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A Topology of Multilevel Inverter for Tolerance against Single and Multiple Faults

Aquib Mehdi Naqvi[1]* Pushkar Tripathi[1] & S P Singh[2]

[1]EED, Institute of Engineering and Technology,Lucknow 226 021, Uttar Pradesh, India

[2]EED, Rajkiya Engineering College, Ambedkar Nagar 224 122, Uttar Pradesh, India

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Multilevel Inverter (MLI) offers numerous advantages, making them suitable for a wider range of application. However, the increased number of switches in MLIs raises the probability of faults. A fault in a switch may interrupt the complete power supply, which is a much-undesired condition for a critical load. In this paper, a fault-tolerant MLI topology is proposed for seven and higher voltage levels, capable of tolerating faults and ensuring the continuity of operation. The proposed MLI exhibits high redundancy in switching states, enabling it to produce all voltage levels even in the event of an open circuit fault in any switch. Fault detection and identification of the faulty switch are accomplished through the analysis of switching signals and measured output voltage. The proposed topology is implemented for 15-levels using the nearest level switching technique, operating under normal conditions as well as during different fault scenarios. Upon detection and identification of a fault by the fault detection unit, the switching sequence is updated to ensure the attainment of rated voltage magnitude and voltage levels. The fault-tolerant capability makes the MLI crucial for critical power supplies and renewable energy systems. The topology and its fault-tolerant operation under various fault cases are tested in the MATLAB Simulink environment and validated in real-time using the OPAL-RT Lab simulator.

Keywords: Detection, Fault-tolerant, Identification, Open-circuit, Switch fault

Introduction

Multilevel Inverters have attracted researchers as well as industries due to their advantages like low THD and low stresses on switches. This inverter provides a good solution for DC-AC conversion. It has a wide range of applications and has been a hot topic of research for the last 4 decades. MLIs, due to their high efficiency and better performance, have widespread applications such as electric drives, active filters, electric vehicles, Flexible AC transmission, custom power devices, and integration with renewable energy resources.[1–4]

Multilevel Inverters consist of a large number of switches that increase cost, size, gate driver, other components, and complexity. The use of a large number of switches in MLIs increases its vulnerability to fault. Commonly occurring faults are Open-Circuit (OC) and Short-Circuit (SC) faults of semiconductor switches. Researchers endeavored to reduce the number of devices and proposed many topologies with reduced device count. Although the MLIs with reduced switches possess many advantages like lesser cost and size, they lose redundancy in switching states. Redundant states /paths available can be used to produce the same voltage-level. Higher redundancy increases reliability which is an essential characteristic of the power system. The redundancy in switching states is an essential characteristic of a Fault-Tolerant (FT) MLI and it is very challenging to achieve it with a lesser number of switches. Researchers suggested many methods and topologies that ensure the reliability of the converter by increasing the redundant paths.[5,6]

Cascaded MLI (CMLI), a classical type of MLI, is made up of modules, each consisting of an H-Bridge of switches and a separate D.C. source. The use of four relays in each module is recommended in relay-based FT CMLI. In a system with seven levels and three modules, consisting of 12 relays to bypass each module in case of a fault, while this setup ensures fault tolerance, a drawback is the operation of the CMLI with reduced voltage levels.[5] Relay-based bypass method is also suggested by Patel *et al.* and Jahan *et al.*[6,7] For a seven-level CMLI, a configuration involving 16 relays is proposed to ensure operational continuity; however, this setup makes the system

*Author for Correspondence
E-mail: aquibmn@gmail.com

uneconomical.[6] Additionally, the discussion does not address the occurrence of two OC faults in different modules. Researchers classified the switches into right and left categories and used relays to bypass the faulty switch.[7] While the additional incorporation of an H-bridge module increases reliability, it also introduces complexity and cost as drawbacks.[7] Current-sensor-based fault detection to bypass the faulty cell is proposed for Cascaded MLI.[8] An ANN-based fault detection and control strategy for a PV-cell-powered CMLI was developed, utilizing a redundant H-bridge to enhance reliability.[9] In these relay-based bypass methods module with the faulty switch is bypassed which reduces the voltage levels hence voltage waveform is get deteriorates. An 11-switch-based 15-level MLI continues its working with a reduced voltage-level in case of a single OC fault in level-generating switches.[10] A five-level MLI, consisting of two H-bridge and two DC sources, is capable of tolerating a single OC fault, however, its voltage-level and magnitude are reduced.[11]

The FT MLI with boosting capability is noteworthy; however, it suffers from a drawback of voltage level loss in case of a fault.[12] A new seven-level MLI topology with 10 switches, possesses high redundancy but a single switching state for both peak values (i.e. $+3V_{DC}$ and $-3V_{DC}$). Hence a fault in one of the involved switch decreases the voltage magnitude and level both.[13]

Neutral Point Clamped (NPC) based topology have been proposed for hybrid five-level applications. These inverters are tolerant against OC and SC faults; however, the number of switches just for the five-level inverter is 14.[14,15] The reliability of the hybrid inverter with NPC and (Flying Capacitor) FC legs is enhanced by the addition of an H-bridge, though it requires a higher number of components to achieve a five-level output.[16] Researcher presents a topology with 12 switches capable of tolerating both OC and SC faults.[17] A fault tolerance approach for diode clamping and switch faults in NPC inverters has been explored to enhance the reliability of grid-connected systems.[18] Back-to-back switching is proposed to mitigate short-circuit faults in NPC.[19] However, in the case of SC faults, quick detection of fault is required, as SC faults could cause severe damage to other components and produce SC conditions on the source side. Further back-to-back switching reduces the intermediate voltage-levels and doubles the switching stress on healthy switches. An asymmetrical 15-level MLI incorporating three unequal DC sources capable of operating in fault-tolerant mode with a modified switching scheme is presented in Roopa *et al.*[20] Asymmetrical MLI of the same level with four DC sources is proposed in Fahad *et al.*[21] Both lose their levels in a single OC fault of a few switches.[20,21]

The topologies possess fault-tolerant features; however, both the nine-switch and 12-switch designs, with the latter including one bidirectional switch, experience rated voltage loss during certain faults.[22]

The Packed E-Cell 13-level inverter, utilizing just eight switches, is capable of operation during faults; however, it operates with reduced voltage-levels.[23] The reliability of the five-level inverter is enhanced by adding four switches, resulting in a total of 12 switches capable of tolerating multiple open-circuit faults.[24] After a single switch fault in the main topology, operation relies on a redundant switch; however, faults in the redundant switches are not considered for subsequent faults.[24]

In the three-phase T-Type inverter reliability is improved using an additional fourth leg and a fault-tolerant bridge.[25] A nine-level Hybrid FC MLI with a redundant leg is proposed that tolerates both SC and OC faults. Despite consisting of 16 switches and the voltage level and magnitude reduced in case of the single OC fault of a few switches.[26] The fault in a DC source of the topology, which consists of two DC sources and two DC capacitors, is considered, and in the healthy state, five switches are in active mode, leading to higher conduction losses.[27] Fault-tolerant operation of MLIs with PV cells is proposed on the by-pass method that has its own drawback like reduced voltage-levels.[9,28]

In this paper, a generalized structure of MLI is proposed that can tolerate single and multiple OC faults and retain its level and magnitude during OC faults. The topology is implemented for 15-level, and a simple fault detection technique has been implemented to identify faults and initiate corrective action. No additional relay is required in the MLI. Its ability to handle switch faults, without compromising performance, directly addresses key challenges in industries such as renewable energy, industrial automation, and aerospace, where reliable power supply is crucial. The next section reveals a broad-ranging topology that is extendable to levels higher than seven. A separate section explains the 15-level topology. In the *Fault-tolerant feature* section, the

available switching patterns of the MLI are discussed. The fault detection and faulty switch identification method are explained in the *Fault Detection and Identification* section. In the *Fault-tolerant operation* section, fault-tolerant operation of the MLI under different fault cases is discussed, along with its real-time results in a later section. The proposed MLI is compared with other fault-tolerant topologies in the second-to-last section, and the last section concludes the paper.

Proposed Generalized Topology

The proposed generalized MLI structure which can be implemented for seven or higher voltage levels is shown in Fig. 1. For a seven-level inverter, three separate DC sources, four unidirectional and eight bidirectional switches are required. For 'n' voltage-levels the number of separate DC Sources required are given by

$$k \text{ (No. of DC Sources)} = \frac{n-1}{2} \quad \ldots (1)$$

where, n is No. of levels of the MLI

For 'n' levels, four unidirectional switches and (n+9)/2 bidirectional switches will be required. The components required to develop the MLI of different levels and respective Total Harmonic Distortion (THD) in output voltage without filters are shown in Table 1.

From the next section 15-level model of the proposed topology will be considered to validate the feasibility of the proposed generalized topology.

Proposed 15-Level Novel MLI

The proposed 15-level MLI shown in Fig. 2 consists of seven separate DC sources, each with an equal voltage of 100 volts (denoted as$1V_{DC}$) and 16 switches (four unidirectional and 12 bidirectional switches).

The topology holds high redundancy for each voltage-level. For any voltage-level either positive or negative there will be only four conducting switches.

A_1 to A_8 are level-generating switches, their appropriate switching will generate voltage-levels of 0 to 7 V_{DC}, and out of them (A_1 to A_8), one switch at a time remains in the ON state. C_1-C_4 are bidirectional switches constructing an H-Bridge that can change the polarity of generated voltage. B_1 and B_2 are bypass switches, these bidirectional switches provide redundant paths in case of a fault in any

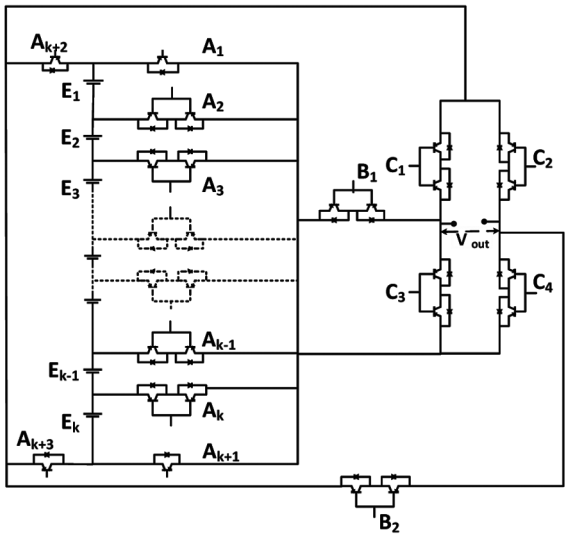

Fig. 1 — The proposed generalized model of fault-tolerant MLI

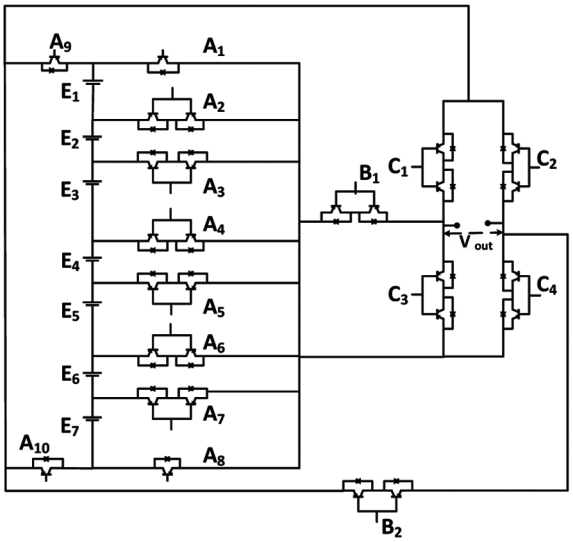

Fig. 2 — Proposed fifteen-level fault-tolerant MLI

Table 1 — Components required for the proposed MLI

Voltage-level	THD in Voltage (in %)*	DC Source	Two Quad Switches	Four Quad Switches	Total Switches
7 Level	12.22	3	4	8	12
9 Level	9.37	4	4	9	13
11 Level	7.58	5	4	10	14
13 Level	6.38	6	4	11	15
15 Level	**5.50**	**7**	**4**	**12**	**16**
….		….	4	….	…
N Level		(N–1) /2	4	(N+9)/2	(N+17)/2

*THD of output-voltage of the MLI without filter

switch of H-Bridge. These redundant bypass switches are incorporated to enhance fault-tolerant capability by increasing the available switching patterns. Although the MLI's performance in a healthy state remains unaffected by removing these switches, it will operate with reduced fault-tolerance capability. A_9-A_{10} are unidirectional essential switches as they are the most involved switches in available switching patterns. Voltage-rating of switches A_4 & A_5 is $4V_{DC}$, A_3 & A_6 is $5V_{DC}$, A_2& A_7 is $6V_{DC}$, rest of switches are $7V_{DC}$. The next section describes the switching combinations available for the 15-level MLI.

Fault-Tolerant Feature

The Proposed topology produces 15 voltage-levels consisting of $\pm7V_{DC}$, $\pm6V_{DC}$, $\pm5V_{DC}$, $\pm4V_{DC}$, $\pm3V_{DC}$, $\pm2V_{DC}$, $\pm1V_{DC}$, and 0. Due to the availability of many switching patterns for each voltage-level, the MLI has high redundancy which leads to high reliability. Five switching patterns for all the voltage-levels are shown in Table 2. Only four switches are used at a time, for example, to produce $+7V_{DC}$ there are five patterns each consisting of four switches, in P_1 switching patterns A_9, C_1, C_4, and A_8 will be in the 'on' state, the rest of 12 switches will remain off. Switching patterns for positive half cycles are denoted by '**P**' and for negative half cycle '**N**'isused. Output-voltage level and path of the current of the MLI with switching pattern P_1 and N_1 (Table 2) is shown in Fig. 3.

The proposed MLI can also be implemented with high frequency switching scheme like PWM, however to minimize the switching losses the MLI is simulated with nearest-level switching technique with fundamental 50 Hz switching frequency. In this method, switching losses significantly reduces due to fewer transitions per cycle.[29] The output voltage and current waveform of the MLI, when operated with an inductive load of 10 ohms and 10.4624 mH is shown in Fig. 4. THD of output-voltage and current without filter is 5.5% and 0.01% respectively. However THD is expected to reduce upon use of appropriate filter. For i^{th} voltage-level switching angle can be given by

$$\theta_i = sin^{-1}\left(\frac{i-0.5}{(n-1)/2}\right) \quad \ldots (2)$$

where, I =1,2,3,4,5,6,7, and n is the number of levels of the MLI

MLI possesses high reliability and capability to operate in case of OC fault in any switch of the MLI. All the voltage-levels are available in case of a fault in any switch, as indicated in Table 3. Considering the fault in A_1, the table shows that all the voltage-levels can be produced using any switching pattern, but for $7V_{DC}$ only P_1 that is $A_9C_1C_4A_8$ is available and for $-7V_{DC}$ any pattern, except N_2 (that is $A_{10}C_1C_4A_1$), can be used.

Fault Detection and Identification

The voltage waveform of N-level MLI can be divided into (N+1) sections according to the level of the waveform. Positive half cycle can be divided into k sections where k = (N+1)/2 and j^{th} voltage-level is considered as $(j+1)^{th}$ section. Similarly, the negative half cycle can also be divided into k sections, and j^{th} voltage-level is considered as $(k+j+1)^{th}$ section. This has been demonstrated in Table 4 and Fig. 5 for 15-level MLI. There are 16 sections in one cycle and eight sections in each half cycle.

In this fault detection and identification method, reference signals are used to predict the output voltage, and it is compared to the voltage waveform observed by the voltage sensor at the output terminals.

Table 2 — Available switching patterns for the proposed fifteen-level MLI

Voltage-level	Switching pattern 1		Switching pattern 2		Switching pattern 3		Switching pattern 4		Switching pattern 5	
$+7V_{DC}$	P_1	$A_9C_1C_4A_8$	P_2	$A_{10}C_2C_3A_1$	P_3	$A_{10}B_2C_3A_1$	P_4	$A_{10}B_2B_1A_1$	P_5	$A_{10}B_1C_2A_1$
$+6V_{DC}$		$A_9C_1C_4A_7$		$A_{10}C_2C_3A_2$		$A_{10}B_2C_3A_2$		$A_{10}B_2B_1A_2$		$A_{10}B_1C_2A_2$
$+5V_{DC}$		$A_9C_1C_4A_6$		$A_{10}C_2C_3A_3$		$A_{10}B_2C_3A_3$		$A_{10}B_2B_1A_3$		$A_{10}B_1C_2A_3$
$+4V_{DC}$		$A_9C_1C_4A_5$		$A_{10}C_2C_3A_4$		$A_{10}B_2C_3A_4$		$A_{10}B_2B_1A_4$		$A_{10}B_1C_2A_4$
$+3V_{DC}$		$A_9C_1C_4A_4$		$A_{10}C_2C_3A_5$		$A_{10}B_2C_3A_5$		$A_{10}B_2B_1A_5$		$A_{10}B_1C_2A_5$
$+2V_{DC}$		$A_9C_1C_4A_3$		$A_{10}C_2C_3A_6$		$A_{10}B_2C_3A_6$		$A_{10}B_2B_1A_6$		$A_{10}B_1C_2A_6$
$+1V_{DC}$		$A_9C_1C_4A_2$		$A_{10}C_2C_3A_7$		$A_{10}B_2C_3A_7$		$A_{10}B_2B_1A_7$		$A_{10}B_1C_2A_7$
0 V_{DC}		$A_9C_1C_4A_1$		$A_{10}C_2C_3$ A_8		$A_{10}B_2C_3A_8$		$A_{10}B_2B_1A_8$		$A_{10}B_1C_2A_8$
$-1V_{DC}$	N_1	$A_9C_2C_3A_2$	N_2	$A_{10}C_1C_4A_7$	N_3	$A_9C_2B_1A$	N_4	$A_9B_2B_1A_2$	N_5	$A_9B_2C_3A_2$
$-2V_{DC}$		$A_9C_2C_3A_3$		$A_{10}C_1C_4A_6$		$A_9C_2B_1A_3$		$A_9B_2B_1A_3$		$A_9B_2C_3A_3$
$-3V_{DC}$		$A_9C_2C_3A_4$		$A_{10}C_1C_4A_5$		$A_9C_2B_1A_4$		$A_9B_2B_1A_4$		$A_9B_2C_3A_4$
$-4V_{DC}$		$A_9C_2C_3A_5$		$A_{10}C_1C_4A_4$		$A_9C_2B_1A_5$		$A_9B_2B_1A_5$		$A_9B_2C_3A_5$
$-5V_{DC}$		$A_9C_2C_3A_6$		$A_{10}C_1C_4A_3$		$A_9C_2B_1A_6$		$A_9B_2B_1A_6$		$A_9B_2C_3A_6$
$-6V_{DC}$		$A_9C_2C_3A_7$		$A_{10}C_1C_4A_2$		$A_9C_2B_1A_7$		$A_9B_2B_1A_7$		$A_9B_2C_3A_7$
$-7V_{DC}$		$A_9C_2C_3$ A_8		$A_{10}C_1C_4A_1$		$A_9C_2B_1A_8$		$A_9B_2B_1A_8$		$A_9B_2C_3A_8$

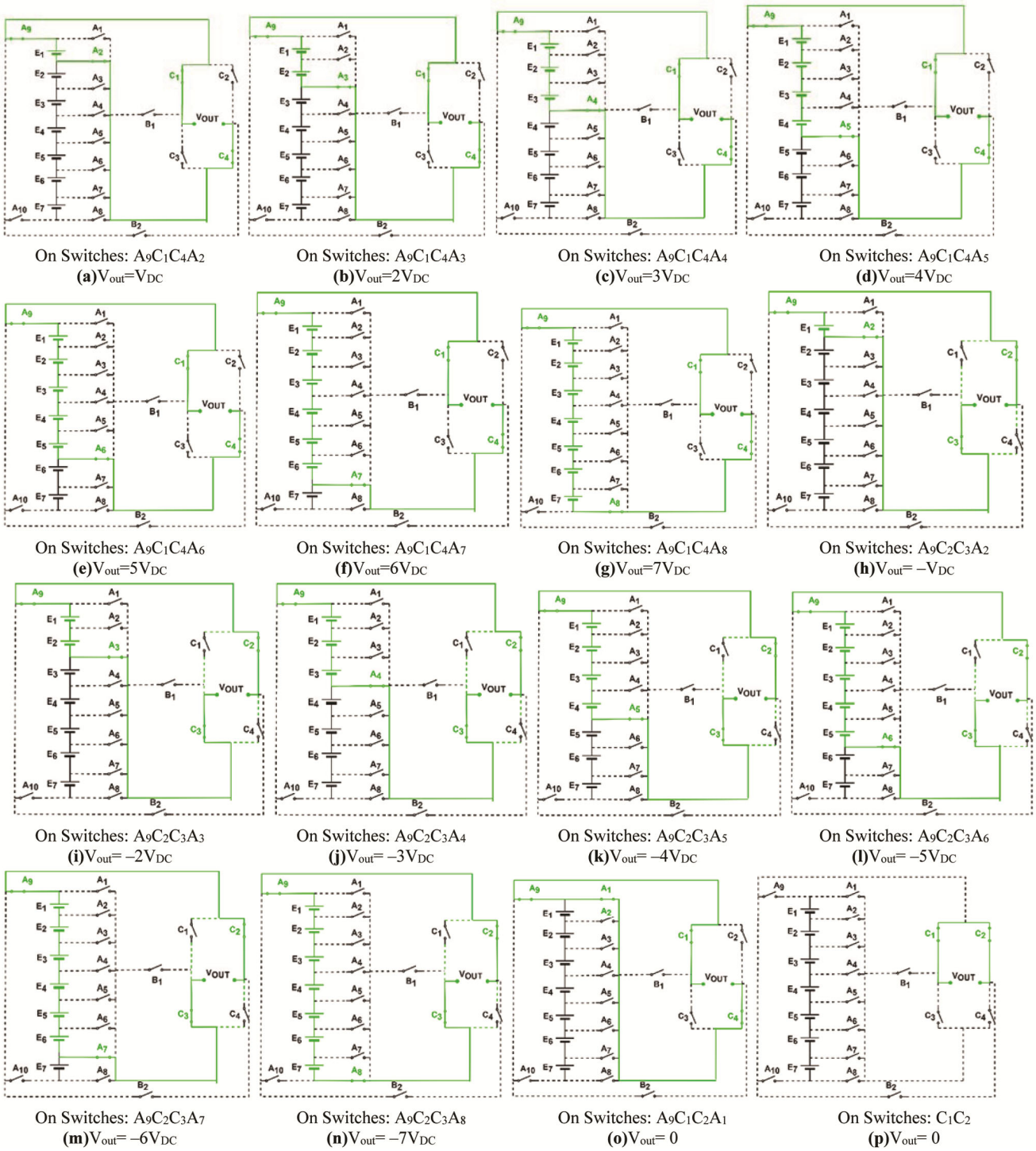

Fig. 3 — Current path and respective voltage in Switching-pattern 1 (as shown in Table 2)

Let the expected voltage be denoted as V_e and the actual output voltage as V_o If the difference $|V_o - V_e|$ remains within a specified threshold, it indicates a healthy condition. When a fault occurs in any switch, it leads to a deviation from the expected output voltage. The information of the switching pattern implemented and the section of the waveform in which deviation has occurred are utilized to identify the faulty switch. Disturbance can be categorized as follows

1. Disturbance in a level
2. Disturbance for half cycle (positive or negative)
3. Disturbance for full cycle

A. Disturbance for full cycle

Combinations of switching patterns for positive and negative half cycles make 25 cases. When the MLI is being operated with any of these 25 combinations, and disturbance for the full cycle of output voltage has occurred, the faulty switch can be identified using Table 5.

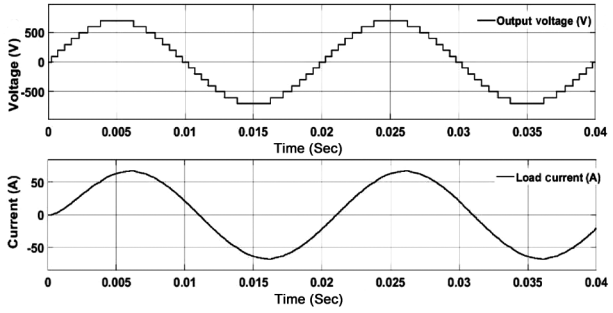

Fig. 4 — Output voltage and current of the MLI with RL (inductive) load

If the fault continues from one half cycle to next half cycle, then this full cycle fault can be observed from very first level of the next half cycle. Therefore to identify a full cycle disturbance in output voltage instead of waiting for full cycle, it can be observed from L_1 of one half cycle to L_1 of the next half cycle.

The error signal which is the difference of the expected voltage and output voltage is shown in Fig. 6. In the case of switching pattern P_1 and N_1 being used for switching the MLI, Fig. 6 shows

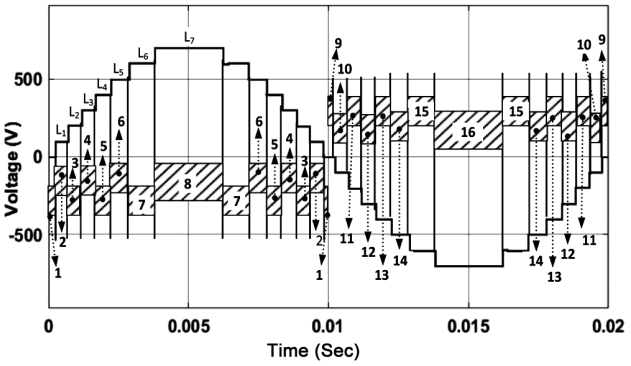

Fig. 5 — Division of sections in a cycle

Table 3 — Available switching pattern in different single OC fault

Fault in Switch↓	Available Pattern														
VL→	7 V_{DC}	6 V_{DC}	5 V_{DC}	4 V_{DC}	3 V_{DC}	2 V_{DC}	1 V_{DC}	0	–1 V_{DC}	–2 V_{DC}	–3 V_{DC}	–4 V_{DC}	–5 V_{DC}	–6 V_{DC}	–7 V_{DC}
A_1	P_1	All	All	All	All	All	All	All	All	All	All	All	All	All	N_1, N_3-N_5
A_2	All	P_1	All	All	All	All	P_2-P_5	All	N_2	All	All	All	All	N_1, N_3-N_5	All
A_3	All	All	P_1	All	All	P_2-P_5	All	All	All	N_2	All	All	N_1, N_3-N_5	All	All
A_4	All	All	All	P_1	P_2-P_5	All	All	All	All	All	N_2	N_1, N_3-N_5	All	All	All
A_5	All	All	All	P_2-P_5	P_1	All	All	All	All	All	N_1, N_3-N_5	N_2	All	All	All
A_6	All	All	P_2-P_5	All	All	P_1	All	All	All	N_1, N_3-N_5	All	All	N_2	All	All
A_7	All	P_2-P_5	All	All	All	All	P_1	All	N_1, N_3-N_5	All	All	All	All	N_2	All
A_8	P_2-P_5	All	All	All	All	All	All	All	All	All	All	All	All	All	N_2
A_9	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	All	N_2	N_2	N_2	N_2	N_2	N_2	N_2
A_{10}	P_1	P_1	P_1	P_1	P_1	P_1	P_1	All	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5
C_1	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	All	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5
C_2	P_1, P_3-P_4	P_1, P_3-P_4	P_1, P_3-P_4	P_1, P_3-P_4	P_1, P_3-P_4	P_1, P_3-P_4	P_1, P_3-P_4	All	N_2, N_4-N_5	N_2, N_4-N_5	N_2, N_4-N_5	N_2, N_4-N_5	N_2, N_4-N_5	N_2, N_4-N_5	N_2, N_4-N_5
C_3	P_1, P_4-P_5	P_1, P_4-P_5	P_1, P_4-P_5	P_1, P_4-P_5	P_1, P_4-P_5	P_1, P_4-P_5	P_1, P_4-P_5	All	N_2-N_4	N_2-N_4	N_2-N_4	N_2-N_4	N_2-N_4	N_2-N_4	N_2-N_4
C_4	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	P_2-P_5	All	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5	N_1, N_3-N_5

Table 4 — Sections for 15-level MLI

	Switching (Positive Half Cycle)								Switching (Negative Half cycle)							
Level	0	1V_{DC}	2V_{DC}	3V_{DC}	4V_{DC}	5V_{DC}	6V_{DC}	7V_{DC}	0	–V_{DC}	–2V_{DC}	–3V_{DC}	–4V_{DC}	–5V_{DC}	–6V_{DC}	–7V_{DC}
Section	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Table 5 — Faulty switch in case of full cycle disturbance

		Switching Pattern (N cycle)				
		N_1	N_2	N_3	N_4	N_5
Switching Pattern (P cycle)	P_1	A_9	C_1 /C_4	A_9	A_9	A_9
	P_2	C_2 /C_3	A_{10}	C_2	x	C_3
	P_3	C_3	A_{10}	x	B_2	B_2 /C_3
	P_4	x	A_{10}	B_1	B_1 /B_2	B_2
	P_5	C_2	A_{10}	B_1/C_2	B_1	A_3

voltage and error waveforms for one healthy cycle and then for a fault that continues in all the sections of the positive half and in the very first level of next (−ve) half cycle. This indicates, it is a full cycle fault and a switch involved in all the levels of the full cycle must be faulty. In P_1 and N_1 switching pattern, A_9 is the only switch that is involved in all levels of the cycle i.e. A_9 switch must be faulty. Similarly, with other combinations of switching patterns, if a full cycle fault occurs, the faulty switch can be identified from Table 5.

B. Disturbance for a Half Cycle

After one cycle a continuous disturbance in all the sections of the positive half occurred when the MLI was implemented with P_1 and N_1 switching pattern as depicted in Fig. 7. In P1, three switches namely A9, C1 and C4 keep conducting during positive half cycle

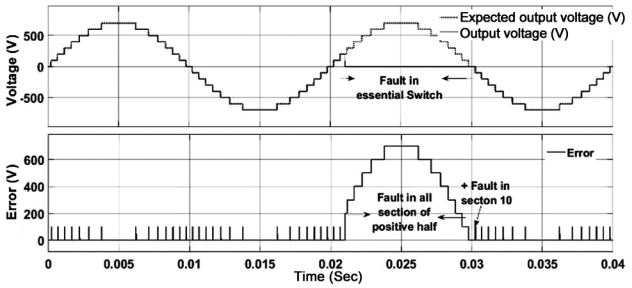

Fig. 6 — Fault in all sections of positive half and section 10

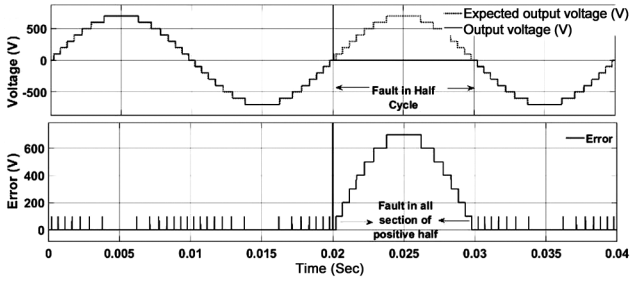

Fig. 7 — Fault in all sections of positive half

whereas switches A9, C2 and C3 keep conducting during negative half cycle.

Switch A_9 conducts in both half cycles, whereas C_1 and C_4 kept on in only a positive half cycle. This indicates, either C_1 or C_4 is faulty. Similarly, with other combinations of switching patterns if a cycle fault occurs, the faulty switch can be identified from Table 6.

C. Disturbance in a Level

If the disturbance in any single level of output voltage is observed, fault can be identified using the information of the section number in which the disturbance has occurred, and the implemented switching pattern during that disturbance. The faulty switch in case of disturbance in different sections with different switching patterns is shown in Table 7.

The output voltage waveform of the MLI with P_1 and N_1 switching pattern is shown in Fig. 8. In positive half of the second cycle the missing $+2V_{DC}$ indicates a fault in section 3. With switching pattern P_1, switches A_9, C_1, C_4 and A_3 are expected to be conducting in section 3. Three switches (namely A_9, C_1 and C_4) are common for other levels, however, A_3 is used for section 3 only, which indicates A_3 is faulty. Similarly, in the case of other switching patterns, the faulty switch of corresponding section can be seen from Table 7.

Table 7 — Faulty switch identification

SI→	Positive half cycle						Negative half cycle				
Sec ↓	P_1	P_2	P_3	P_4	P_5	Sec ↓	N_1	N_2	N_3	N_4	N_5
1	A_1	A_8	A_8	A_8	A_8	9	A_1	A_8	A_1	A_1	A_1
2	A_2	A_7	A_7	A_7	A_7	10	A_2	A_7	A_2	A_2	A_2
3	A_3	A_6	A_6	A_6	A_6	11	A_3	A_6	A_3	A_3	A_3
4	A_4	A_5	A_5	A_5	A_5	12	A_4	A_5	A_4	A_4	A_4
5	A_5	A_4	A_4	A_4	A_4	13	A_5	A_4	A_5	A_5	A_5
6	A_6	A_3	A_3	A_3	A_3	14	A_6	A_3	A_6	A_6	A_6
7	A_7	A_2	A_2	A_2	A_2	15	A_7	A_2	A_7	A_7	A_7
8	A_8	A_1	A_1	A_1	A_1	16	A_8	A_1	A_8	A_8	A_8

SI: Switching Implemented Sec: Section

Table 6 — Faulty switch in case of half cycle disturbance

		Fault in cycle	Switching Pattern (N cycle)				
			N_1	N_2	N_3	N_4	N_5
Switching Pattern (P cycle)	P_1	Positive	C_1 /C_4	A_9	C_1 /C_4	C_1 /C_4	C_1 /C_4
		Negative	C_2 /C_3	A_{10}	C_2 /B_1	B_1 /B_2	B_2 /C_3
	P_2	Positive	A_{10}	C_2 /C_3	A_{10}/C_3	A_{10}/C_2 /C_3	A_{10}/C_2
		Negative	A_9	C_1 /C_4	A_2	A_9/B_1 /B_2	A_9 /B_2
	P_3	Positive	A_{10}/B_2	B_2 /C_3	A_{10}/B_2 /C_3	A_{10} /C_3	A_{10}
		Negative	A_9/C_2	C_1 /C_4	A_9/B_1 /C_2	A_9/B_1	A_9
	P_4	Positive	A_{10}/B_1 /B_2	B_1 /B_2	A_{10} /B_2	A_{10}	A_1
		Negative	A_9/C_2 /C_3	C_1 /C_4	A_9/C_2	A_9	A_2
	P_5	Positive	A_{10}/B_1	B_1/C_2	A_{10}	A_{10}/C_2	A_{10}/B_1 /C_2
		Negative	A_9 /C_3	C_1 /C_4	A_9	A_9/B_2	A_9/B_2 /C_3

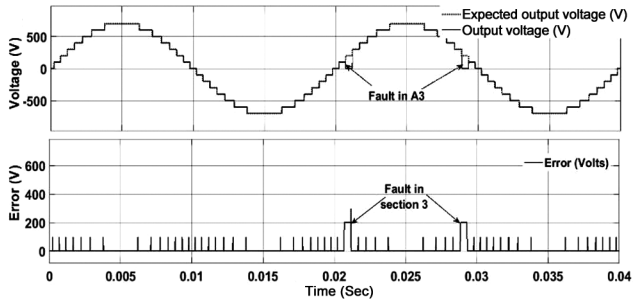

Fig. 8 — Fault in section 3

Fault-Tolerant Operation

Once a fault is identified, corrective action must be taken to keep the MLI working without interruption. Here, corrective action is based on the change of the switching pattern according to type of the faulty switch.

A few fault cases are considered below

A. Fault in a single switch of a level-generating switch
B. Fault in multiple switches of level-generating switches
C. Fault in single switch of H-Bridge switches
D. Fault in A_9 or A_{10}

a) Fault in Single Switch of Level-Generating Switches

Switches A_1 to A_8 are used to generate voltage-levels. In case of a fault in any of these switches, alternate switching patterns are available. For further understanding let us take a few examples of such faults

i. Fault in A_3

The output-voltage of the MLI implemented with P_1 and N_1 switching pattern, the fault in switch A_3 has occurred after one cycle, as shown in Fig. 9(a), and the THD in voltage increases to 10.3%. Fault in A_3affects the $+2V_{DC}$ and $-2V_{DC}$. As Table 3 shows that there is one redundant switching pattern N_2 available for $-2V_{DC}$ though four patterns, P_2- P_5 will be available for $+2V_{DC}$, which do not involve A_3. After fault identification in negative half of second cycle, as corrective action P_2 and N_2 switching pattern is implemented for $+2V_{DC}$ and $-2V_{DC}$, and for rest of the levels P_1 and N_1 is used.

ii. Fault in A_5

In case of fault in switch A_5, as Fig. 9(b) shows that distortion in $+4V_{DC}$ has occurred in second cycle. There are four redundant switching patterns (P_2- P_5) available for $+4V_{DC}$ though one pattern N_2 for $-4V_{DC}$, which don't involve A_5. After fault identification, a redundant switching pattern is implemented to produce $+4V_{DC}$ and $-4V_{DC}$.

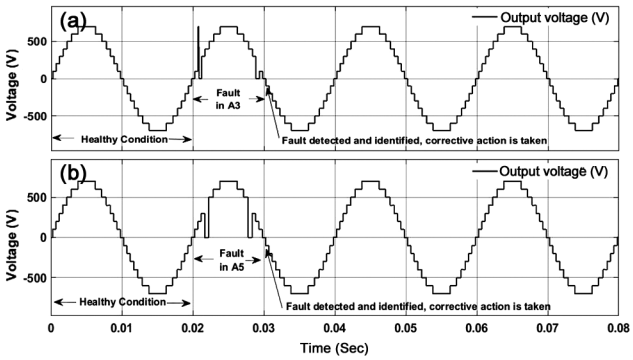

Fig. 9 — Output voltage of the MLI in case of a fault in (a) switchA_3, and (b) switch A_5

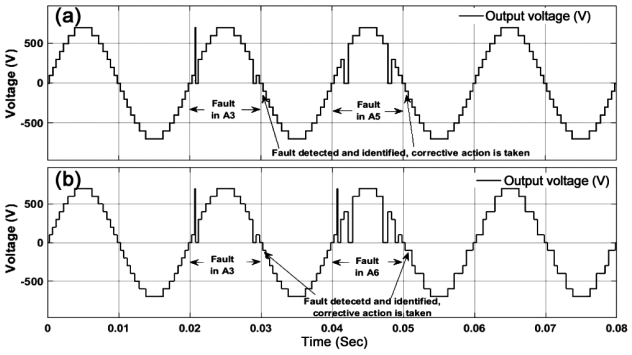

Fig. 10 — Output voltage of the MLI in case of a fault in (a) switches A_3 and $A_5$and (b) switches A_3 and A_6

b) Fault in Multiple Switches of Level-Generating Switches

In the single switch fault of level-generating switch, it can be observed that there is either a positive or negative pattern in which one level has only one redundant pattern. For example, in case of a fault in A_3, only N_2-switching-pattern is available for $-2V_{DC}$. We can categorize a fault in multiple switches into two types.

i. Type I: Fault in Pair of Switches not Involved in Generating Same Voltage-Level

Many pairs of level-generating switches are not responsible for the same voltage-levels. For example, A_3 and A_5, in different switching patterns A_3 is involved for generating $\pm2V_{DC}$ (P_1 and N_1) and $\pm5V_{DC}$ (P_2 and N_2) whereas A_5 is involved in generating $\pm3V_{DC}$ (in P_2 and N_2) and $\pm4V_{DC}$ (in P_1 and N_1). In cases of fault in such pairs of switches, the MLI is capable of producing all the voltage-levels. In the above-discussed pair of switches A_3 and A_5, A_6 can be replace A_3 to produce $\pm2V_{DC}$ and $\pm5V_{DC}$ and A_4 can replace A_5 to produce $\pm3V_{DC}$ and $\pm4V_{DC}$. The output voltage of the MLI with switching patterns P_1 and N_1, for faults in A_3 and A_5, is shown in Fig. 10(a). After

identification of the faulty switch, as corrective action to produce $\pm 2V_{DC}$ and $\pm 5V_{DC}$, P_2 and N_2 is implemented which utilizes A_4 and A_6 in place of A_5 and A_3 respectively, though other voltage-levels are produced using P_1 and N_1 switching patterns.

ii. Type II: Fault in Pair of Switches Involved in Generating Same Voltage-Level

Either A_3 or A_6 is involved in the generation of $\pm 2V_{DC}$ (similarly for $\pm 5V_{DC}$). Therefore, in case of a fault in both of these switches, there is no redundant switching pattern available to generate $\pm 2V_{DC}$ and $\pm 5V_{DC}$. As shown in Fig. 10(b) two voltage-levels for positive as well for negative cycles get distorted. After corrective action THD in voltage is about 11%. Although faults in such a pair of switches will reduce the intermediate voltage-levels, the amplitude of output voltage will remain the same. Such pairs are A_1-A_8, A_2-A_7, A_3-A_6, and A_4-A_5.

c) Fault in a Switch of H-Bridge

H-Bridge is used to change the polarity of output voltage, C_1 and C_4 are switched together whereas C_2 is switched with C_3. In P_1 and N_1 switching pattern C_1 and C_4 generate positive polarity and C_2 and C_3 generate negative polarity.

i. Fault in C_1

If a fault in C_1 or C_4 occurs, it distorts the whole positive cycle. In such cases the other switching pattern not involving the faulty switch can be used for a positive cycle, like P_2 can be used in this case. For the MLI implemented with P_1 and N_1 switching pattern, fault in C_1 has occurred as shown in Fig. 11(a). After identification of the fault, as a corrective action, the switching pattern for positive half is changed to P_2.

ii. Fault in C_2

If a fault in C_2 or C_3 occurs, it distorts the whole negative cycle. In such cases the other switching pattern not involving the faulty switch can be used for a negative cycle, like N_2 can be used in this case. For the MLI implemented with P_1 and N_1 switching pattern, a fault in C_2 has occurred as shown in Fig. 11(b). After identification of the fault, as a corrective action, the switching pattern for the positive half is change to N_2.

In multiple faults of H-bridge, as in case C_1 was already faulty and C_2 became suddenly faulty. In this case, switching patterns consisting of bypass switches can be considered. Switching patterns P_4 and N_4 in Table 2 consist of bypass switches.

A_9 and A_{10} switches are categorized as essential switches as the MLI has high dependency on them. The MLI is capable of operating in case of a fault in one of these two switches. A case of the fault in switch A_9, is shown in Fig. 12, where after fault detection and identification, the available redundant switching patterns, P_2 and N_2, are utilized to produce all the voltage-levels. Similarly, in case of a fault in A_{10}, P_1 and N_1 switching patterns can be used. However, in case of a fault in both $A_9$and A_{10} switches, the MLI does not have redundant switching pattern. To overcome this issue a relay can be added in parallel to A_{10}, to enable MLI to operate at the rated magnitude while retaining all its voltage-levels.

THD in the output voltage of the MLI during fault and after corrective action is shown in Table 8. The last two columns show a sample of faults in multiple switches concurrently.

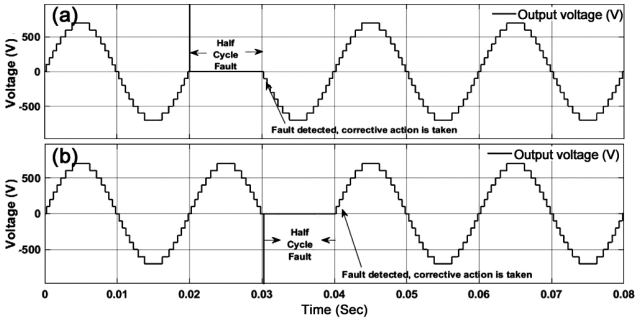

Fig. 11 —Output voltage of the MLI in case of a fault in (a) switch C_1 and (b) switch C_2Fault in A_9 or A_{10}

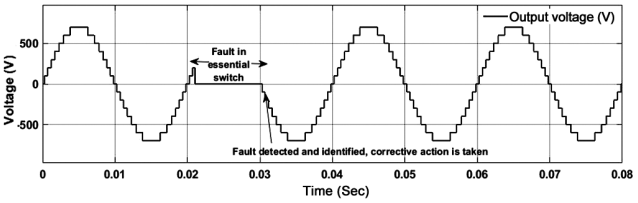

Fig. 12 —Output voltage of the MLI in case of a fault in A_9

Table 8 — THD and rms of the output voltage during fault and post-fault condition

Fault in switch→		A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	C_1	C_2	C_3	C_4	A_3& A_5	A_3& A_6
During fault	V_{rms}(V)	498.4	497.5	494.6	489.3	480.2	464.7	427.8	359.9	352.5	352.5	352.5	352.5	476.1	460.6
	THD_v(%)	5.5	8.2	13.8	20.4	28.8	39.7	61.36	93.3	44.6	44.6	44.6	44.6	31.9	42.4
Post fault	V_{rms}(V)	498.4	498.4	498.4	498.4	498.4	498.4	498.4	498.4	498.4	498.4	498.4	498.4	483.6	498.4
	THD_v(%)	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	11.1	5.5

THD_v and V_{rms} is total harmonic distortion and the rms of fundamental component of the output voltage without filter respectively

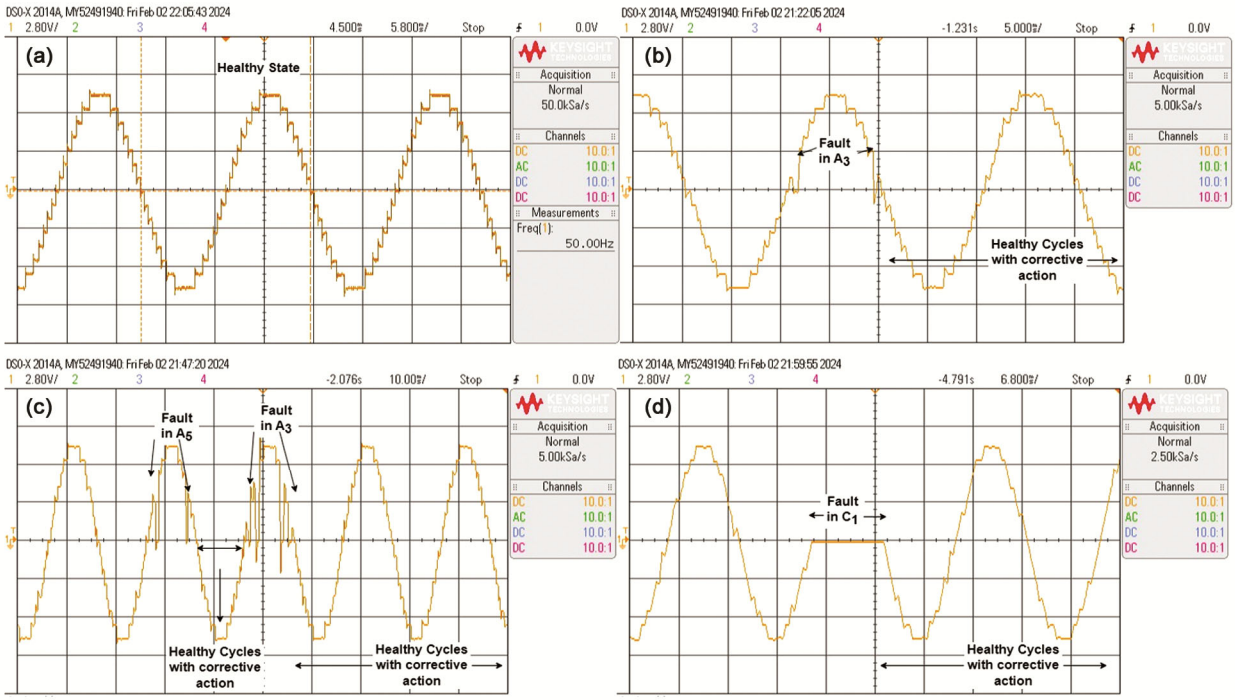

Fig. 13 —Real-time result: Output voltage of the MLI in (a) Healthy state (b) Fault in switch A_3 (c) Fault in switches A_3 and A_5, and (d) Fault in switch C_1

Table 9 — Comparison of different fault tolerant MLIs

Reference	Voltage-levels	Number of DC sources	Number of switches used	Number of IGBTs required	Number of gate drivers	Number of relays used	All levels retained in all single OC faults	Magnitude retained in all single OC faults	All levels retained in all multiple OC faults	Magnitude retained in all multiple OC faults
[5]	15	7	28	28	28	28	Yes	Yes	No	Yes
[6]	15	7	28	28	28	35+	Yes	Yes	No	Yes
[7]	15	7	32	32	32	2	No	Yes	No	No
[10]	15	7	11	18	11	0	No	No	No	No
[13]	15	7	14	20	14	0	No	No	No	No
[11]	13	6	27	27	27	0	No	No	No	No
[20]	15	3A	10	14	10	0	No	No	No	No
[21]	15	4A	11	12	11	0	No	No	No	No
Proposed	15	7	16	28	16	0	Yes	Yes	Yes*	Yes

*except a few pairs discussed in b(ii) of section Fault-tolerant operation

Real-Time Result

The proposed topology is tested and validated within the real-time environment, utilizing the OPAL-RT simulator lab OP4512. The output voltage waveform is scaled down by factor 100 and observed using the Keysight DSOX2014a. The output voltage of the MLI in a healthy state is displayed in Fig. 13(a), whereas Fig. 13(b) illustrates a single OC switch fault occurring in A_3. Upon completion of the half cycle with the fault, it is detected, and corrective action is promptly taken to maintain the magnitude and all voltage levels intact. Fig. 13(c) illustrates the occurrence of multiple OC faults simultaneously in both A_3 and A_5, whereas Fig. 13(d) shows a fault happening in an H-bridge switch C_1.

Comparison with other Fault-Tolerant Structures

In Table 9, the proposed topology is compared with other fault-tolerant MLI topologies. Requirements of components like separate DC sources, IGBTs, diodes, and gate drivers are important to compare as they determine the cost, size, space required, etc. in few topologies a large number of gate drivers are required.[5–7,11] An additional 6 diodes are required in

the MLI.[21] However, the feature of a fault-tolerant MLI can be determined on the basis of its ability to tolerate single and multiple OC faults. In addition to maintaining the continuity of operation in such fault-conditions, MLI should maintain the voltage-level and magnitude. For a single OC fault, all the voltage-levels and magnitude scan be retained.[5,6] A module of four switches is bypassed in case of just a single switch fault and switches will be subjected to a higher voltage in case of fault.[5,6] A single switch fault in either left or right category bypasses all the switches of the respective category. Fault in the redundant bridge is not considered.[7] A single OC fault in a bidirectional level generating switch will reduce the two intermediate voltage-levels whereas a single fault in H-bridge will affect either the positive or negative half-cycle.[10] Single switch faults in either S_1 or S_5 will reduce the voltage-level[13]. Single switch fault will reduce the voltage-level and magnitude.[11,20,21] The proposed topology can retain all the voltage-levels and maintain the rated voltage in not only single OC faults but also in multiple OC faults except the multiple faults in a few switch pairs discussed in b(ii) of section '*Fault-tolerant operation'*.

Conclusions

A generalized fault-tolerant topology of MLI capable of handling single and multiple open-circuit faults, is presented in this paper. The proposed topology is demonstrated for fifteen voltage levels using the nearest-level switching technique and tested under various fault cases, including single and multiple open-circuit faults in level-generating and H-bridge switches. Fault detection is achieved through a simple voltage comparison, and an algorithm modifies the switching pattern to exclude faulty switches using inherent redundant configurations. This ensures continuous operation while maintaining rated voltage magnitude and voltage levels under fault conditions, thereby enhancing MLI reliability. Despite the MLI's high total blocking voltage, its exceptional reliability makes it suitable for critical loads and renewable energy systems. Future work could involve integrating the fault-tolerant MLI with solar PV systems to improve PV system reliability. The results of MATLAB simulations and real-time OPAL-RT testing verify the fault-tolerant operation of the MLI.

Declaration

The first Author is a research scholar under AICTE doctoral fellowship scheme of AICTE, which operates under the Department of Higher Education, Ministry of Education, Government of India.

Conflict of Interest

There is no conflict of interest to declare.

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