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Heavy-ion Radiation Strikes on LDD Implanted RingFET using 3D Numerical Device Simulations

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A ringFET is formed on vertically revolving bulk MOSFET with concentrical cylinders acting as the source, gate, and drain areas. By integrating lightly doped regions into conventional ringFET structures, three distinct types of LDD implanted ringFETs can be designed, with the implantation location defining each type. If LDD is implanted merely on the source side, it creates an SLDD ringFET, and if LDD is implanted only on the drain side, it results in a DLDD ringFET. Lastly, upon implanting LDD on both the drain and source sides, it forms an LDD ringFET structure. The effects of heavy ion radiation on three different types of LDD ringFET structures are assessed using 3D TCAD simulations and compared to the effects on a conventional ringFET structure under normal incidence. The ion strike's position, angle of incidence, and the resulting transient current and charge collected all affect the device's sensitivity and can be used to identify its vulnerable area. It has been found that the ringFET structure with LDD implanted on both the source and drain sides is more resilient to radiation-induced damage, as it exhibits a lower collected charge of 98.271 fC compared to conventional ringFET (106.768 fC), SLDD ringFET (101.549 fC), and DLDD ringFET (100.468 fC) for a LET value of 100 MeV/(mg/cm²). Additionally, the LDD-implanted ringFET exhibits a superior I_{ON}/I_{OFF} ratio compared to the other two LDD structures and conventional ringFET structures.

Keywords: Lightly doped drain, Linear energy transfer, RingFET, Single event transient, Technology computer aided design

Introduction

CMOS technology advances as devices become compact and offer the benefit of low power consumption. After decades of device shrinking, MOSFETs experience Short Channel Effects (SCEs) when the device dimensions are further reduced. To increase CMOS scalability, the semiconductor industry has investigated several innovative device architectures. De Lima and Gimenez[1] presented a planar circular-gate architecture with short channel immunity without sacrificing device planarity. RingFETs have better short-channel immunity than conventional MOSFETs because they don't have side interface regions due to the circular gate geometry, which leads to trap-induced leakages. RingFET performs better because of the lower OFF current in the short channel regime. Williams *et al.*[2] performed the 2D Hydrodynamic simulations on ringFET at the nanoscale level and studied the device performance based on various effective gate lengths. De Lima and Gimenez[3] described how ringFETs might be used as power MOSFETs. Kumar *et al.*[4] developed an analytic approach to model the drain current of ringFETs. Similarly, an analytical approach for gate-engineered and channel-engineered ringFETs has been modeled using the Poisson equation by Kumar *et al.*[5] The ringFET architecture for high-frequency ions was evaluated using Technology Computer Aided Design (TCAD) by Kumari *et al.*[6] Kumari *et al.*[7] investigated the ringFET for gas molecule detection using a TCAD-based computational approach. Conventional and Lightly Doped Drain (LDD) short-channel MOSFETs' characteristics were studied by Liu.[8] Shobana *et al.*[9] investigated the performance optimization of ringFETs utilizing LDD implantation. These new device alternatives may replace conventional MOSFETs in the digital circuits used in the radiation-prone environment in the near future.

The devices are subjected to radiation in radiation-prone circumstances, including space applications, which impair their ability to function. A high-energy particle colliding with the silicon substrate of a semiconductor device can produce Single-Event Effects (SEEs), which are unusual and unforeseen electronic phenomena. As a result of these subatomic interactions, charged particles are created. These

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events can be categorized as either hard or soft, with hard errors being destructive and potentially catastrophic, such as single event gate rupture, single event latch-up, and single event burnout, which can damage or destroy the device. In contrast, soft errors are non-destructive and may cause temporary errors, such as Single Event Transient (SET) and single event upset, which subsides after a short period. Baumann[10] and Nicolaidis[11] investigated single-event effects, which result in both short-term and long-term device degradation as well as dependability problems in electronic systems. The study of SEEs is a crucial aspect of device design and operation in the nanoscale regime.[12] Specifically, the study on the effects of irradiation in space on satellite operations near the Earth has been investigated.[13] Numerous resources on SEE are accessible for MOSFETs[14] and MOSFET-based circuits.[15] Experimental studies have assessed the performance of N-Channel MOSFETs under gamma radiation[16] and X-ray photon beams.[17] There have been discussions in the literature about SEEs on gate-all-around devices, FinFETs, and multi-gate devices.[18–23] Also, the effects of heavy-ion-induced transients on bulk and SOI FinFETs[24] have been performed experimentally. The effects of radiation on LDD MOS devices were examined by Woodruff and Adams.[25] The impact of radiation on conventional ringFETs[26] at the nanoscale regime has been explored, whereas the impact of radiation on LDD implanted ringFETs remains an unexplored area of research.

Materials and Methods

Design of RingFET Structures and analysis of I_d-V_g Characteristics using 3D TCAD Simulations

A conventional ringFET's DC performance has already been reported.[26] The 3D view of a conventional ringFET (n-type) is given in Fig. 1(a). The top perspective of a conventional ringFET is given in Fig. 1(b). The 2D perspective of a conventional ringFET is given in Fig. 1(c).

This study utilizes the Sentaurus 3D TCAD device simulator, which consists of two primary components: Sentaurus Structure Editor (SDE) and Sentaurus Device Simulator (SDEVICE). The SDE tool is employed to create the device structure by specifying impurities, and contacts, and generating a mesh. Subsequently, the SDEVICE tool is used to execute DC simulations. Shobana *et al.*[9] have already reported on the DC performance of SLDD (upon implanting LDD merely on the source side), DLDD (upon implanting LDD merely on the drain side), and LDD

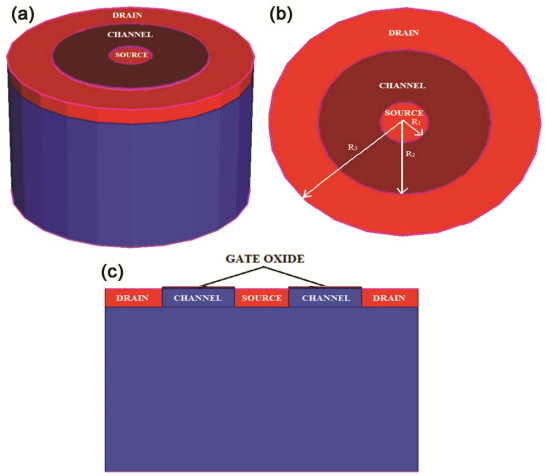

Fig. 1 — Representation of ringFET: (a) 3-dimensional view, (b) Top angle view, (c) 2D perspective

Table 1 — ringFET Dimensions

Parameter	Value
Radius of source (R_1)	12 nm
Length of gate (R_2–R_1)	32 nm
Length of drain (R_3–R_2)	25 nm
Thickness of gate oxide	1 nm
Height of substrate	90 nm
Gate work function	4.35 eV
Doping of source / drain	1×10^{20} / cm^3
Doping of substrate	2×10^{18} /cm^3
Extension of LDD	10 nm
Doping of the LDD region	1×10^{19} / cm^3

(upon implanting LDD on both the drain and source sides) ringFETs utilizing the device parameters listed in Table 1.

For calibration purposes, identical structures are built again and their I_d-V_g characteristics are replicated using TCAD. A 3D visual representation of the LDD ringFET generated through TCAD is provided in Fig. 2(a), with a top perspective of the device shown in Fig. 2(b). Fig. 2(c) illustrates the 2D layout of the LDD ringFET. The addition of LDD on both the source and the drain side increases the drain area, resulting in increased ON current, and it enhances the control of the drain potential on the source barrier, resulting in less OFF current and an improved I_{ON}/I_{OFF} ratio of the ringFET.

The operation of the device can be effectively illustrated using the band diagram depicted in Fig. 3, which is obtained by performing a Z-cut on 2D representations of both conventional ringFET and LDD ringFET images.

A barrier separates the drain and the source in the channel area of the Conduction Band (CB) and

Valence Band (VB) once the device is turned off as shown in Fig. 3(a) and 3(b). As a result, there isn't any transfer of electrons from the source to the drain. But once a gate voltage is provided, the channel area's band structure alters as shown in Fig. 3(c) and 3(d), making it possible for electrons to travel from the source to the drain and aiding current flow. The device simulation employs several physics models, including the field-dependent[27] and concentration-dependent[27] mobility models, the Lombardi model[27], the Shockley-Read-Hall recombination model[27], and the drift-diffusion model.[27] To take quantum effects into account, the eQuantum Potential model[27] is used.

The I_d-V_g characteristics of the conventional ringFET (Conv), the SLDD ringFET upon implanting LDD merely on the source side (SLDD), the DLDD ringFET upon implanting LDD merely on the drain side (DLDD), and the LDD ringFET upon implanting LDD on both the drain and source sides (LDD) are depicted in Fig. 4.

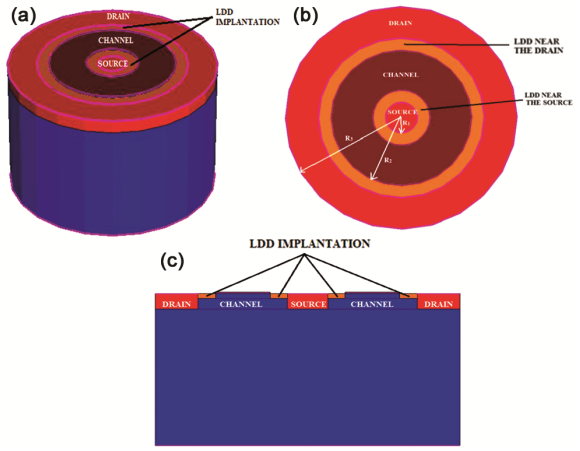

Fig. 2 — Representation of LDD ringFET: (a) 3-dimensional view, (b) Top angle view, (c) 2D perspective

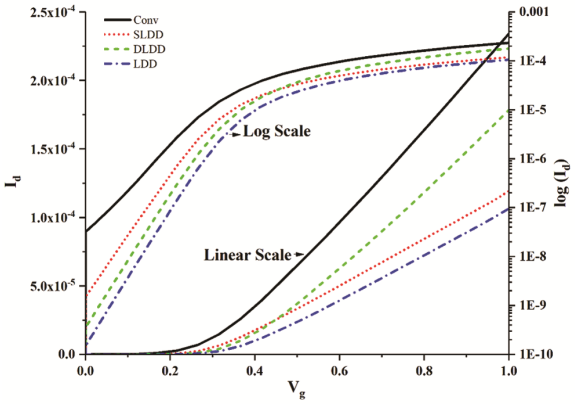

Fig. 4 — I_d-V_g characteristics of ringFET structures

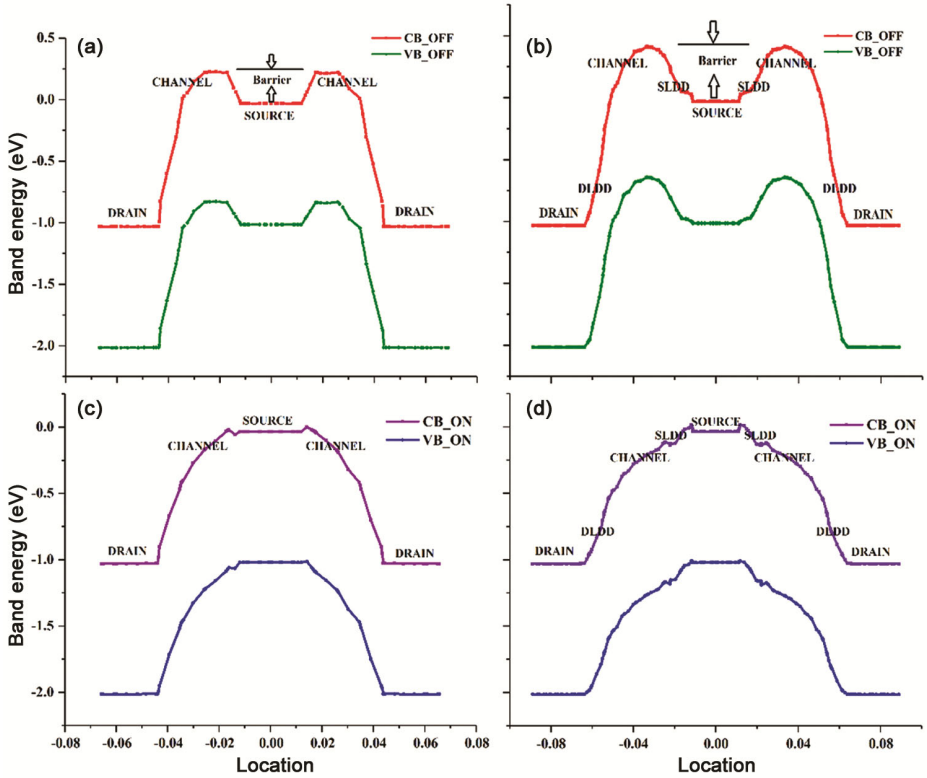

Fig. 3 — Band Diagram: (a) OFF State - conventional ringFET, (b) OFF State - LDD ringFET, (c) ON State - conventional ringFET, (d) ON State - LDD ringFET

The DC performance metrics like I_{ON}, I_{OFF}, SS, V_{th}, and G_m for SLDD ringFET, DLDD ringFET, and LDD ringFET are extracted and listed in Table 2. All these ringFETs have been calibrated against the published results[9]. The DC parameters of a conventional ringFET device with the same device dimensions are also tabulated in Table 2 for comparison.

From Table 2, it is clear that the ringFET structure with LDD implanted on both the source and drain sides has a higher I_{ON}/I_{OFF} ratio than the other two LDD structures and conventional ringFET structures.

Single Event Transient Analysis

Single Event Transients are created by the interaction of ionizing heavy ions with semiconductors, which results in mobile charge carriers. SETs are transient voltage excursions (voltage spikes) caused by the electric field separation of an ion's charge when it travels through a device at the node of an integrated circuit. SETs are non-destructive errors and can be cleared by refreshing the electronics. The heavy-ion model utilized by the device simulator tool (SDEVICE) to simulate irradiation effects in TCAD devices employs the Gaussian radial distribution with a characteristic radius of 20 nm, a characteristic time of 2 ps, and a Gaussian distribution of time centered around 20 ps, to characterize the column of electrons and holes that generate the ion's impact in the device using normal incidence. Several charge carriers are created per unit of time and area as the device interacts with heavy ions. The rate at which these carriers are generated is calculated using the formula,

$$G\,(l,w,t) = G_{\,LET}(l)R(w,l)T(t) \quad \ldots (1)$$

where, $G_{LET}(l)$ is the linear energy transfer generation rate density and the rate of generation varies over time and space, denoted by T(t) and R(w,l), respectively.

In this work, these models have been invoked under transient mode at V_{GS} = 0V and V_{DD} = 1V, and the drain current is plotted versus time. Several key factors are considered when a heavy ion interacts with a device during SET analysis. These factors include the point of radiation ion impact, the direction of ion incidence, the timing of ion arrival, the radial distance of the ion from the device's centre, and the radiation dosage value expressed in picocoulombs per micrometer. This dosage value can be alternatively represented as Linear Energy Transfer (LET), which is typically measured in pC/μm or MeV/(mg/cm²).

The bipolar amplification of heavy-ion irradiation is analogous to the amplification of the deposited charge. According to Castellani[(14)], the bipolar gain is provided by the equation, where the bipolar gain can be described as the proportion of charge collected over charge deposited acquired from drain current transients.

$$\beta = \frac{Q_{collect}}{Q_{deposit}} \quad \ldots (2)$$

where, $Q_{collect}$ is the charge collected and $Q_{deposit}$ is the charge deposited. The following expressions are used to obtain $Q_{collect}$ and $Q_{deposit.}$

$$Q_{collect} = \int_0^{t1} I_d\,(t)dt \quad \ldots (3)$$

$$Q_{deposit} = 10.3 \times LET(\text{MeV}/\,(\text{mg/cm}^2)) \times \text{T}_{\text{Si}}\,(\mu\text{m}) \quad \ldots (4)$$

where, t_1 is the transient time, T_{Si} is the silicon film thickness, and $I_d(t)$ is the altered drain current.

When radiation hits the device, electron-hole pairs are created. Depending on the position of the radiation impact, electron-hole pairs recombine at varying rates, and the amount of charge collected is dependent on this recombination. The vulnerable area of the device is found to be the area with the highest collected charge.

To assess the sensitivity of an LDD ringFET to heavy ion radiation, the SET analysis is conducted in

Table 2 — Calibrated results of ringFET

Type of ringFET		Parameters					
		I_{ON}(A)	I_{OFF}(A)	I_{ON}/I_{OFF}	SS(mV/ decade)	V_{th}(V)	G_m(A/V)
SLDD ringFET	Simulated	1.19×10^{-4}	1.52×10^{-9}	7.83×10^{4}	79.16	0.14	1.75×10^{-4}
	Reported[9]	1.17×10^{-4}	6.12×10^{-9}	1.92×10^{4}	79.01	0.25	2.20×10^{-4}
DLDD ringFET	Simulated	1.79×10^{-4}	3.61×10^{-10}	4.96×10^{5}	73.62	0.18	3.14×10^{-4}
	Reported[9]	1.92×10^{-4}	9.33×10^{-10}	2.05×10^{5}	78.51	0.35	3.10×10^{-4}
LDD ringFET	Simulated	1.06×10^{-4}	1.51×10^{-10}	7.02×10^{5}	70.2	0.2	1.74×10^{-4}
	Reported[9]	1.00×10^{-4}	3.73×10^{-10}	2.69×10^{5}	89.98	0.32	1.90×10^{-4}
Conventional ringFET	Reported[26]	2.34×10^{-4}	3.23×10^{-8}	7.24×10^{3}	93.82	0.27	3.62×10^{-4}

seven different regions, as illustrated in Fig. 5. These regions include the drain region (CD), LDD near the drain (CDL), channel near the drain (CND), channel centre (CC), channel near the source (CNS), LDD near the source (CSL), and the source region (CS) as illustrated in Fig. 5.

Similarly, SET analysis is performed on six distinct regions of SLDD ringFET: the drain region (CD), channel near the drain (CND), channel centre (CC), channel near the source (CNS), LDD near the source (CSL), the source region (CS), and six distinct regions of DLDD ringFET: the drain region (CD), LDD near the drain (CDL), channel near the drain (CND), channel centre (CC), channel near the source (CNS), the source region (CS). In this work, the SET analysis is performed at a normal angle of incidence and the time at which radiation strikes the device is 20 ps.

Results and Discussion

The device generates an alteration in the drain current when subjected to irradiation at 20 ps and the amplitude of alteration in the drain current is different at different strike locations. This altered drain current of the SLDD ringFET, DLDD ringFET, and LDD ringFET at various locations, with a LET value of 100 MeV/(mg/cm²) are depicted using Figs. 6(a–c). The total collected charge can be computed by integrating the SET current pulse. This procedure is then repeated for different LET values to analyze the device's response to heavy ion radiation.

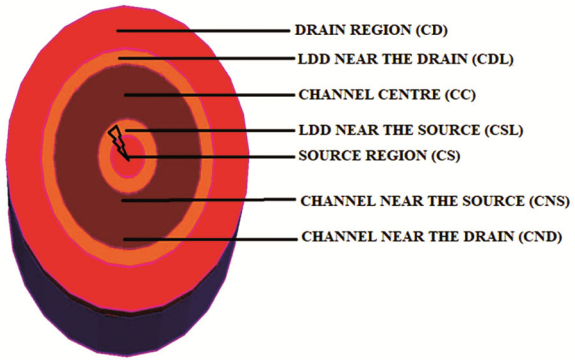

Fig. 5 — Radiation locations on LDD ringFET

For different dosage values, Table 3 displays the collected charge ($Q_{collect}$) for SLDD, DLDD, and LDD ringFET structures at various device locations. The $Q_{collect}$ is compared to the $Q_{collect}$ of conventional ringFET.[26]

From Table 3, it is clear that the collected charge grows in direct proportion to the LET value because a higher dose generates an increased SET current. From Table 3, it is evident that the vulnerable area in a conventional ringFET[26] is the channel near the drain (CND) since this location has the highest $Q_{collect}$. The next vulnerable area is the drain (CD), then the channel centre (CC), then the channel near the source (CNS), and finally the source (CS) since the source region has the lowest $Q_{collect}$. Similarly, in SLDD ringFETs, the channel near the drain (CND) is the most vulnerable area to radiation-induced damage, followed by the drain (CD), and the source (CS) is the least vulnerable. In DLDD and LDD ringFETs, the LDD near the drain (CDL) is the most vulnerable area, followed by the channel near the drain (CND), and the source (CS) remains the least susceptible region.

For various LET values for conventional ringFET (Conv), SLDD ringFET (SLDD), DLDD ringFET (DLDD), and LDD ringFET (LDD), respectively, Figs. 7(a–d) show the $Q_{collect}$ at four distinct regions: the channel centre (CC), channel near the drain (CND), LDD region near the drain (CDL), and the drain region (CD).

Analysis of Table 3 and Fig. 7 indicates that the LDD ringFET architecture outperforms the others in terms of radiation hardness, as its $Q_{collect}$ values are consistently lower than those of the conventional ringFET, SLDD ringFET, and DLDD ringFET across different LETs. The $Q_{deposit}$ for various LET values are summarized in Table 4.

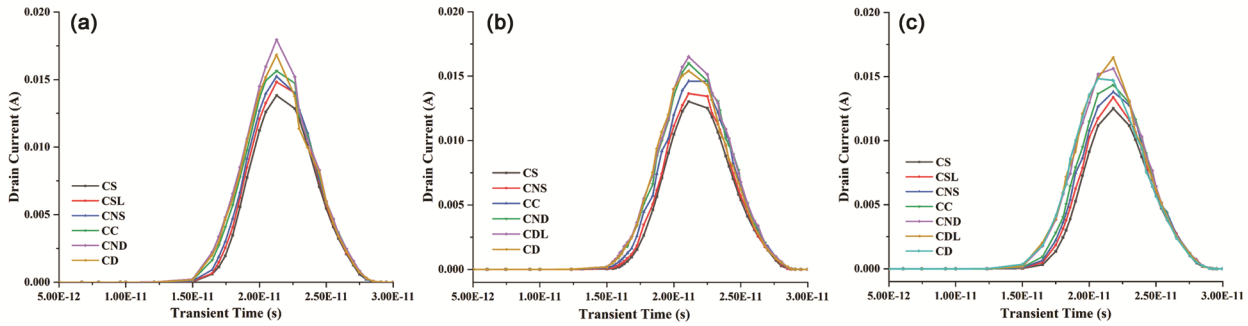

Fig. 6 —Drain Current: (a) SLDD ringFET, (b) DLDD ringFET, (c) LDD ringFET

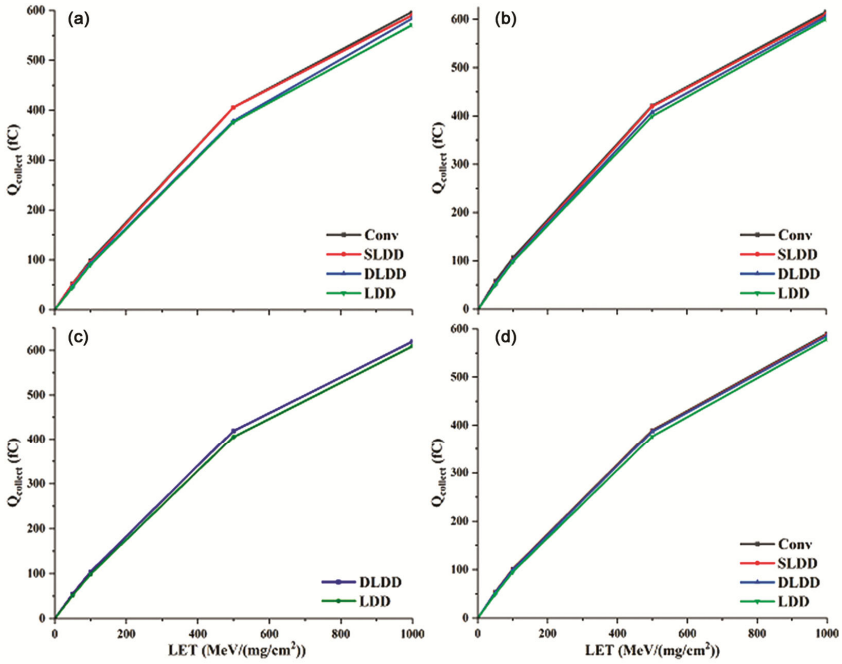

Fig. 7 — $Q_{collect}$ for different dose values: (a) at CC, (b) at CND, (c) at CDL, (d) at CD

Table 3 — $Q_{collect}$ at various locations for different dose values

LET (MeV/(mg/cm^2))	Type	$Q_{collect}$ (fC)						
		CS	CSL	CNS	CC	CND	CDL	CD
1	Conventional	0.31	—	0.50	0.75	0.89	—	0.84
	SLDD	0.25	0.34	0.44	0.72	0.85	—	0.81
	DLDD	0.24	—	0.39	0.60	0.84	0.86	0.81
	LDD	0.20	0.28	0.36	0.59	0.82	0.85	0.79
50	Conventional	42.98	—	45.74	51.94	58.44	—	53.62
	SLDD	39.84	43.58	44.23	50.85	53.11	—	51.15
	DLDD	38.16	—	40.96	45.77	52.16	54.40	51.08
	LDD	34.30	37.91	40.75	44.50	50.25	51.51	49.17
100	Conventional	86.64	—	90.48	98.31	106.80	—	101.30
	SLDD	81.69	88.14	89.45	95.08	101.55	—	99.62
	DLDD	78.09	—	84.67	92.18	100.47	104.16	98.94
	LDD	73.25	79.73	83.61	89.92	98.27	98.84	94.90
500	Conventional	360.37	—	377.49	405.57	421.11	—	389.60
	SLDD	350.12	370.49	372.13	405.28	419.46	—	387.47
	DLDD	344.22	—	361.60	378.09	407.85	419.38	386.66
	LDD	330.09	345.99	356.57	375.94	399.34	405.54	376.32
1000	Conventional	571.05	—	583.73	597.32	615.67	—	590.28
	SLDD	559.53	573.70	578.06	590.27	610.85	—	587.21
	DLDD	545.43	—	571.73	584.10	605.97	619.71	585.35
	LDD	536.71	558.49	565.47	571.20	600.33	609.23	578.56

Table 4 — $Q_{deposit}$ for several dose values

LET (MeV/(mg/cm^2))	$Q_{deposit}$ (fC)
1	0.18025
50	9.0125
100	18.025
500	90.125
1000	180.25

The bipolar amplification factor (β) for conventional, SLDD, DLDD, and LDD ringFETs is shown in Table 5 for a range of dosage values and device locations.

According to Table 5, conventional ringFETs and SLDD ringFETs exhibit maximum β in the channel near the drain (CND) and minimal β in the source region (CS). In contrast, DLDD ringFETs and LDD

Table 5 — β for different dose values

LET (MeV/(mg/cm^2))	Type	β						
		CS	CSL	CNS	CC	CND	CDL	CD
1	Conventional	1.71	—	2.75	4.18	4.96	—	4.67
	SLDD	1.4	1.86	2.41	3.98	4.7	—	4.52
	DLDD	1.32	—	2.15	3.34	4.67	4.78	4.49
	LDD	1.12	1.54	2	3.27	4.52	4.73	4.41
50	Conventional	4.77	—	5.08	5.76	6.48	—	5.95
	SLDD	4.42	4.84	4.91	5.64	5.89	—	5.68
	DLDD	4.23	—	4.55	5.08	5.79	6.04	5.67
	LDD	3.81	4.21	4.52	4.94	5.58	5.72	5.46
100	Conventional	4.81	—	5.02	5.45	5.93	—	5.62
	SLDD	4.53	4.89	4.96	5.28	5.63	—	5.53
	DLDD	4.33	—	4.7	5.11	5.57	5.78	5.49
	LDD	4.06	4.42	4.64	4.99	5.45	5.48	5.27
500	Conventional	4	—	4.19	4.5	4.67	—	4.32
	SLDD	3.89	4.11	4.13	4.5	4.65	—	4.3
	DLDD	3.82	—	4.01	4.2	4.53	4.65	4.29
	LDD	3.66	3.84	3.96	4.17	4.43	4.5	4.18
1000	Conventional	3.17	—	3.24	3.31	3.42	—	3.28
	SLDD	3.1	3.18	3.21	3.28	3.39	—	3.26
	DLDD	3.03	—	3.17	3.24	3.36	3.44	3.25
	LDD	2.98	3.1	3.14	3.17	3.33	3.38	3.21

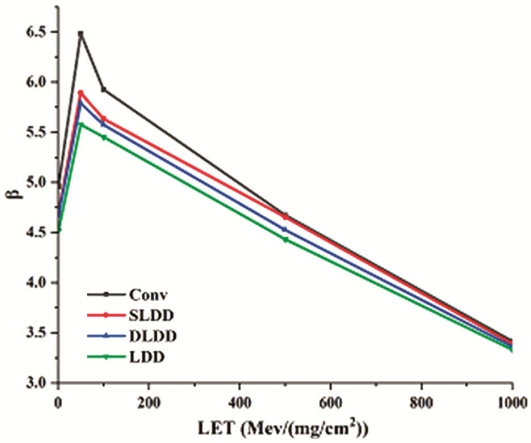

Fig. 8 — β at CND region

ringFETs show maximum β in the LDD near the drain (CDL), followed by the channel near the drain (CD), and minimal β in the source region (CS).

The bipolar amplification at the channel near the drain region (CND) for different LET values is shown in Fig. 8. From Fig. 8, it is evident that the bipolar amplification of the LDD ringFET is consistently lesser than the conventional ringFET, SLDD ringFET, and DLDD ringFET.

Conclusions

Using 3D TCAD simulations, this study compared the SET response of conventional ringFET, SLDD ringFET, DLDD ringFET, and LDD ringFET structures. The channel near the drain (CND) is identified to be the most vulnerable area in conventional and SLDD ringFET. The LDD region near the drain (CDL) is identified to be the most vulnerable area in DLDD and LDD ringFET. In all 4 cases, the source region is identified to be the least vulnerable. The findings suggest that the LDD ringFET structure stands out in terms of radiation resistance, as it shows a significantly lower collected charge ($Q_{collect}$) compared to conventional ringFET and other LDD-implanted structures, indicating a reduced vulnerability to radiation-induced damage. Our analysis has been limited to normal angles of incidence. However, it is crucial to extend the study to include both positive and negative angles of incidence to gain a more comprehensive understanding of the impact of radiation on the device.

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