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High-Performance On-Chip Inductor Design using Hilbert Fractal Geometry with Split Ring Array

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This paper focuses on enhancing the on-chip inductor's performance by improving the inductance (L), Quality factor (Q-factor), and Self-Resonant Frequency (SRF), which are crucial in the design of high-performance Radio Frequency Integrated Circuits (RFICs) and Monolithic Microwave Integrated Circuits (MMICs). This work proposes a new approach by incorporating a geometry variation of the traditional on-chip inductor using the Hilbert fractal geometry with a Split Ring Array (SRA) configuration. This approach leverages the superior attributes of Hilbert-based fractals in designing on-chip inductors. Simulation results have shown an inductance of 1.249 nH, a Q-factor of 13, and an SRF of 55 GHz, marking three times higher Figure of Merit (FoM) compared with conventional on-chip inductor designs, illustrating the potential that this geometry offers to push forward the performance benchmarks in integrated circuit applications. These results demonstrate the feasibility of fractal geometries to achieve superior performance metrics. The proposed design will become highly prospective for future RFIC and MMIC applications in terms of high-efficiency inductors.

Keywords: Figure of merit, Integrated circuit, MMIC, Quality factor, RFIC

Introduction

There has been an increased need for high-performance on-chip inductors because of their crucial application in RFICs and MMICs. The on-chip inductor's performance has been characterized using parameters such as L, Q-factor, and SRF. Improvement in inductance and quality factor are always preferable in an area-efficient high-efficiency mm-wave transceiver.[1] Nevertheless, it has been very difficult to optimize these parameters at higher frequencies because of increased losses and parasitic effects. Together with the advances in operating frequency and integration density, the demand for on-chip inductors with higher electrical performance, like a higher Q-factor with a better Figure of Merit (FoM), has become a requirement. The Q-factor and FoM are important since they affect the efficiency, linearity, as well as the noise of the RF and microwave circuits, including filters, amplifiers, and oscillators. The problem with the present on-chip inductor design, like the coplanar spiral inductor in Fig. 1(2), involves the low Q-factor, inductance density, and other parasitic effects.

Earlier research has investigated approaches like patterned ground shields[3] and multi-layer stacking[4]; however, balancing size and performance continues to present a significant challenge. To overcome such challenges, novel design methodologies aiming to optimize inductor geometries have been pursued aggressively. Of such geometries, the fractal geometry has also been prominently highlighted for its distinctive space-filling characters and self-similarity features, which are potentially beneficial for the increase of inductance and suppression of the resistive loss in the inductor. In particular, the fractal geometry of the Hilbert fractal, which possesses an efficient and compact structural property, also shows promising prospects for on-chip inductor design and improvement.[5]

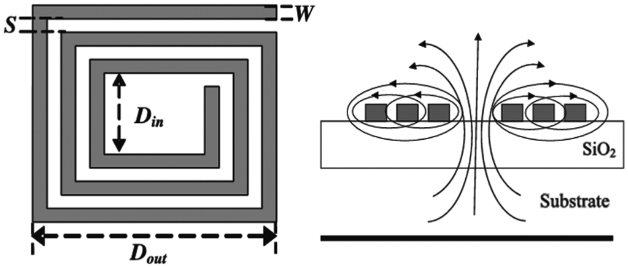

Fig. 1 — Planar Spiral Inductor with cross sectional view indicating magnetic field lines

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In this work, a novel design approach that leverages Hilbert fractal geometry integrated with a split ring array configuration is proposed. This geometry variation enables significant improvements in the Q-factor and FoM of the inductor by minimizing energy losses and enhancing the electromagnetic characteristics. Through detailed simulations, the performance of the Hilbert fractal inductor with SRA is compared with conventional on-chip inductors, demonstrating its superior efficiency and applicability in RFIC and MMIC applications.

The following sections of the paper are structured as follows: review of prior research on fractal geometries for on-chip inductors, methodology and design principles of the proposed inductor, results and discussion highlighting key performance improvements. Finally, concludes with insights into the implications of this work and potential directions for future research.

Literature Review

Recent works have been carried out to enhance on-chip inductors at high frequency using fractal patterns. Fractals, specifically Hilbert curves, provide improved area reduction and higher performance compared to traditional inductors.[6] A novel parallel stacked[7] inductor based on an improved Hilbert fractal increased its Q-value by 50% compared to traditional fractal inductors.[8] Stacked inductors using modified Hilbert patterns have been revealed to provide more than 90% area improvement and increased Q-value with higher inductance.[8,9] MEMS methods have also been utilized to design fractal inductors with a Hilbert curve structure on a silicon substrate, increasing inductance by 50% compared to planar spiral-wound inductors.[10,11] There are various reports in the literature that feature high-performance integrated inductors on a microchip, incorporating fractal geometry with a Hilbert pattern, featuring Split Ring, that describe substantial progress made in terms of improved performance in RFIC and MMIC technology to overcome limitations associated with device minimization.

The recursive nature of the Hilbert curve helps in designing compact layouts with improved inductance value and Q factor.[9] As compared to the conventional structures, fractal inductors presented better performance, but the introduction of SRA into fractal structures has shown further improvements in the value of L, Q-factor, and SRF.[12] A split ring resonator for microwave sensor applications was developed with a sensitivity of 12.03%.[13] Inclusion of SRA within the geometry of an inductor increases the resonating characteristic by manifold, hence making this highly suitable for applications in high-frequency analog front-ends.[6]

Although the improvements brought about by the fractal inductor are promising, there are still some challenges associated with the design, especially about the integration of the design within existing systems. Further studies are required to improve the design for practical applications.

Design Methodology

Hilbert Fractal Geometry

The Hilbert curves depicted in Fig. 2 are space-filling curves with self-similar patterns at different orders.[14] They have many applications in various engineering design processes, like antenna design and circuit design.[15] Regarding the application of on-chip inductors, the fractal geometry of Hilbert has some distinct advantages, such as the increased length and decreased inter-winding capacitance.[16]

SRA in Fig. 3 is a periodic metal ring array with unique electromagnetic properties, such as negative permeability at certain frequencies.[17] When SRA is employed in inductor designs, it has the potential to increase inductance (L) and the quality factor (Q-factor) of inductors by reducing parasitic capacitances and increasing the concentration of magnetic fields.

The proposed design involves the following steps:

Fractal Generation

Generation of Hilbert Curve: A Hilbert curve of desired order is created using software tool such as Microwave Office.

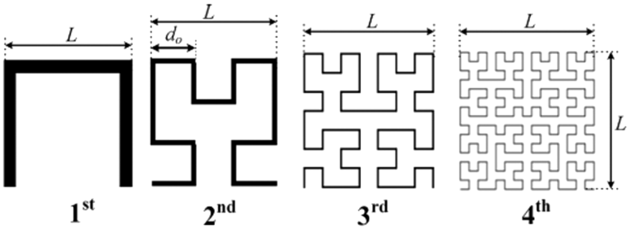

Fig. 2 — Hilbert curve-based Fractals

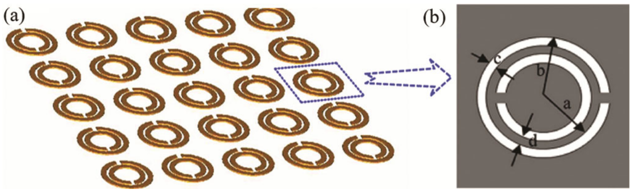

Fig. 3 — SRA: (a) with repeating distance, (b) Single unit cell

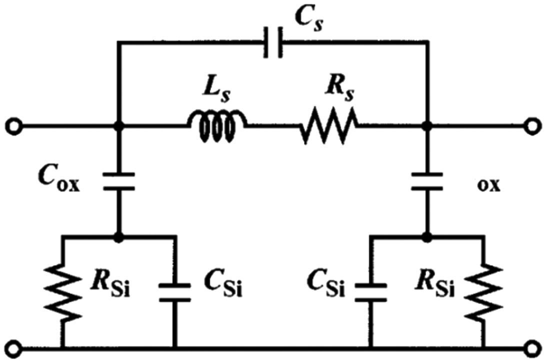

Fig. 4 — Physical model of on-chip spiral inductor

Conductor Pattern Definition: The Hilbert curve is converted to a conductor pattern based on the conductor width, distance, and thickness.[18]

SRA Integration

SRA Design: The SRAs are designed with proper dimensional spacing so that the resonant frequencies are below the desired operating range of the inductor.[19]

SRA Placement: The SRA structures can be placed effectively in the Hilbert fractal pattern either as discrete features or as part of the conductive lines.

Electromagnetic Simulation

Simulation Tool: A full-wave electromagnetic simulator such as Microwave Office is employed to examine the performance of the inductor.

Simulation Setup: Simulation setup involves a 3D environment, taking into account the substrate material properties, along with the feedline configuration.

Simulation Parameters: The crucial simulation parameters, such as inductance (L), quality factor (Q-factor), and Self-Resonant Frequency (SRF), are derived from the simulation.

The physical model of an on-chip spiral inductor is shown in Fig. 4.(20) This model represents a series inductance (L_s) and series resistance (R_s) which are the inductance and resistance of the inductor respectively. The series capacitance is modeled as C_s. Capacitance of the oxide (C_{ox}) is used to model the capacitance between spiral and the silicon substrate.[21] The silicon substrate's capacitance is modeled as C_{si} and resistance is modelled as R_{si}.

The performance metrics to be examined during the design and development process of on-chip inductors are:[6]

Inductance: Hilbert fractal geometry causes the effective length of the inductor to increase, thereby enhancing its inductance properties as compared to the conventional spiral inductor.[22] Integrating SRA increases the overall inductance as it traps the magnetic flux inside the on-chip inductor. A general expression for the on-chip inductor is given by Eq. (1).

$$L_T = \frac{\mu_0 n^2 A}{L} \qquad \dots (1)$$

μ_0 represents the permeability of free space, n denotes the iteration count, A signifies the effective enclosed area, and L indicates the length of the segment.[6]

Quality Factor (Q): The SRA helps to suppress parasitic capacitances, resulting in improved Q-factor.[17] The fractal geometry also contributes to reduced parasitic capacitances, leading to higher Q-factors. The general expression for quality factor of an on-chip inductor is given in Eq. (2).

$$Q = \frac{\omega L_T}{R_s}\frac{R_p}{[(\omega L_T/R_s)^2+1]R_s}\left[1-\frac{R_s^2(C_s+C_p)}{L_T}-\omega^2 L_T\left(C_s+C_p\right)\right] \qquad \dots (2)$$

$$R_p = \frac{1}{\omega^2 C_{ox} R_{Si}} + \frac{R_{Si}(C_{ox}+C_{Si})^2}{C_{ox}^2} \qquad \dots (3)$$

$$C_p = C_{ox} \cdot \frac{1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2}{1+\omega^2(C_{ox}+C_{Si})^2 R_{Si}^2} \qquad \dots (4)$$

ω is referred to as the angular frequency, R_s represents the series resistance, L_T gives the total inductance; and C_s denotes the capacitance between the adjacent layers.

In Eq. (3) R_p and (4), R_p represent the overall parasitic resistance and C_p is the overall parasitic capacitance, derived from oxide parasitic capacitance (C_{ox}), capacitance of the substrate (C_{Si}), and resistance of the substrate (R_{Si}).[22]

Self-Resonant Frequency (SRF): The SRA can be designed to resonate at frequencies above the desired operating range of the inductor, effectively increasing the SRF and it is given by Eq. (5).

$$f_{SR} = \frac{1}{2\pi\sqrt{L_T C_P}} \qquad \dots (5)$$

C_P is the parasitic capacitance.

Figure of Merit (FoM): FoM is a distinct metric provided by Eq. (6) that assesses the proposed inductor's performance with the existing inductors.[22]

$$\mathrm{FOM} = \frac{(\mathrm{Inductance} \times \mathrm{Qualityfactor} \times f_{SR})}{\sqrt{\mathrm{Area}}} \quad \dots (6)$$

Impact of Fractal Order: Increasing the fractal order leads to higher inductance density and lower Q-factor. However, the optimal fractal order depends on the trade-off between inductance density and Q-factor for RFIC and MMIC application requirements.

Impact of SRA Configuration: The number, size, and spacing of SRAs can significantly affect the inductor performance. A careful optimization of these parameters is crucial to achieve the desired performance metrics.

The design process has started with 2nd order and 3rd order Hilbert fractal inductors of area 170 × 170 µm^2 as shown in Fig. 5. It is observed that as the order of the fractal geometry is increased, the inductor's Q-factor is reduced. To overcome this above problem a 3rd order Hilbert fractal inductor with a split ring array is proposed and shown in Fig. 6.

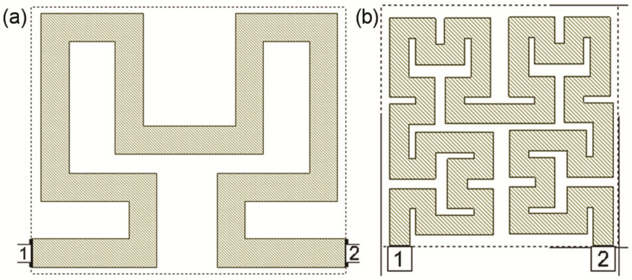

Fig. 5 — Hilbert fractal inductor: (a) 2nd order (b) 3rd order

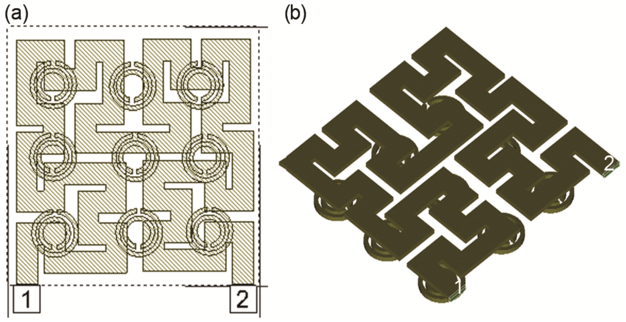

Fig. 6 — 3rd order Hilbert fractal inductor with split ring array: (a) 2D view (b) 3D View

Results and Discussion

Simulated Results

To evaluate the performance of the proposed Hilbert fractal inductor with split ring arrays, a comprehensive simulation study was conducted using a full-wave electromagnetic simulator, Microwave Office. The inductor was developed on a silicon substrate with a thickness of 500 µm. The copper thickness was assumed to be 2 µm with a trace width of 5 µm.

The frequency response of 2nd order and 3rd order Hilbert fractal inductors is shown in Fig. 7 and it is observed that the Q-factor and SRF of 3rd order Hilbert fractal was reduced by 40% and 50% respectively. The frequency response of the proposed Hilbert fractal inductor with Split Ring Array (SRA) is represented in Fig. 8.

The proposed Hilbert fractal inductor with split ring array has resulted in an inductance of 1.249 nH which is three times the existing inductance in the literature, a quality factor of 13 and a Self-Resonant Frequency (SRF) of 55 GHz.

Comparison with Conventional Inductors

The proposed Hilbert fractal inductor with SRA was compared with a conventional spiral inductor of a relevant size. The results show that the proposed inductor exhibits significantly higher inductance density, Q-factor, and SRF. The improved performance is attributed to the combined effects of the Hilbert fractal geometry and the SRA. The performance metrics of the proposed Hilbert fractal inductor with split ring array are compared with state-

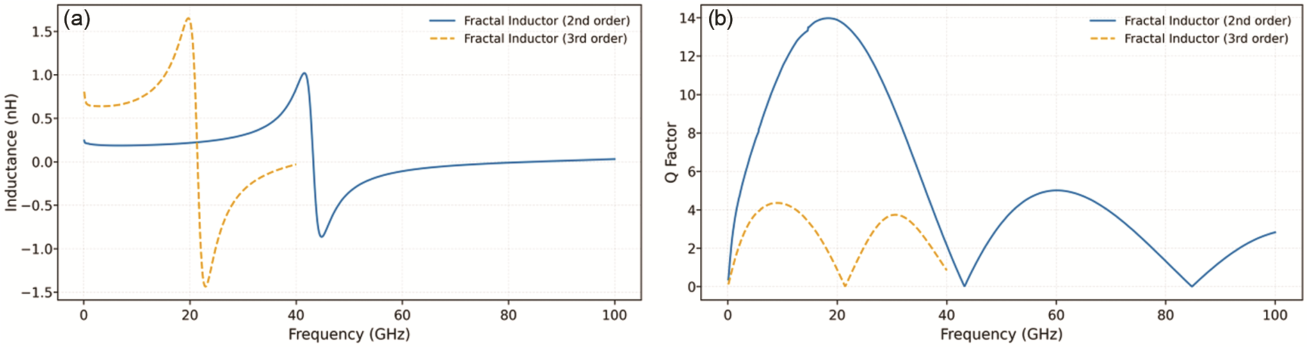

Fig. 7 — Frequency response of 2nd order and 3rd order Hilbert fractal inductors: (a) Inductance (b) Q-factor

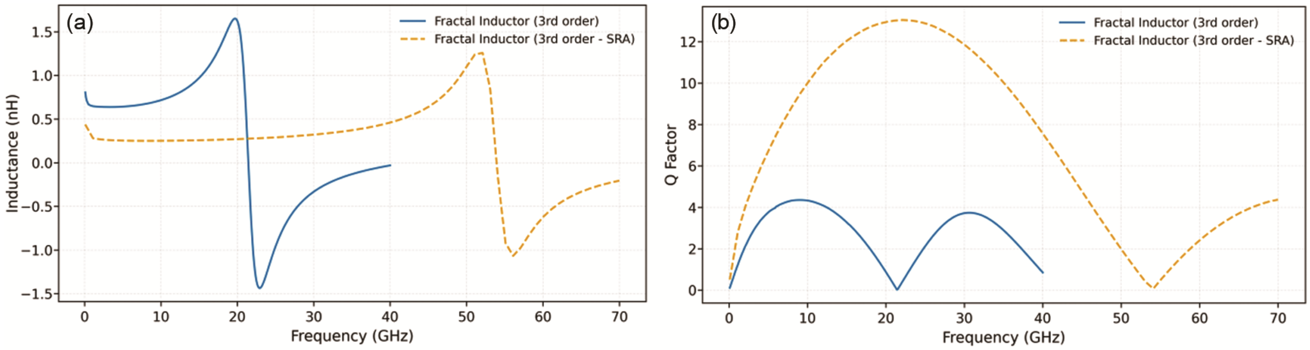

Fig. 8 — Frequency response of 3rd order Hilbert fractal inductor with and without split ring array: (a) Inductance (b) Q-factor

Table 1 — Comparative analysis of the proposed on-chip inductor

	L, nH	Q	f_{SR}, GHz	Chip area, μm^2	FoM
Maric *et al.*[23]	0.3	12	10	200 × 200	0.18
Wang *et al.*[10]	0.9	8.67	10	200 × 200	0.39
Jair *et al.*[24]	0.5	7.06	5	117 × 117	0.15
Proposed (without SRA)	0.5	13	75	170 × 170	2.86
Proposed (with SRA) – 3rd order	1.249	13	55	170 × 170	5.25

of-the-art inductors in the literature and presented in Table 1.

Conclusions

This work has proposed and analysed a novel design of a high-performance on-chip inductor using split ring array (SRA) and Hilbert fractal geometry. Higher inductance density results from the integration of Hilbert fractal geometry, which increases the inductor's effective length. By concentrating the magnetic field and reducing parasitic capacitances, the addition of SRA enhances the inductor's performance even more. To maximize the inductor performance, the effects of several design parameters, including substrate thickness, SRA configuration, and fractal order, were examined. Electromagnetic simulations show that the proposed inductor achieves an inductance of 1.249 nH, a Q-factor of 13, and an SRF of 55 GHz, outperforming the conventional fractal inductor in terms of FoM and inductance for an equivalent on-chip area.

Although the suggested design has a lot of potential for high-performance RFIC and MMIC applications, there are still issues with process variations and fabrication complexity. To fully realize the potential of the suggested design, future research efforts can focus on exploring simplified fabrication techniques. Further performance improvements may result from investigating various fractal geometries and SRA configurations.

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