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Improving On-state current and Ambipolarity of TFET using Gate-Drain and Gate Dielectric Engineering

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This article presents the Gate Overlap on Drain with Hetero Gate Dielectric TFET (GDHD-TFET), a novel tunnel FET structure aimed at addressing the low ON current and ambipolar leakage observed in traditional TFETs. By investigating the combined effects of hetero gate dielectric and gate-drain overlapping, the GDHD-TFET offers a significant improvement in design compared with conventional TFET design. Unlike traditional approaches that focus solely on regulating the tunnel barrier widths at the channel-source junction, the GDHD-TFET simultaneously improves the tunnel barrier widths at both channel-source and channel-drain junctions. As a result, the GDHD-TFET achieves remarkable improvements in ON current and ambipolar conduction, surpassing traditional TFET performance by factors of 10^2 and 10^4, respectively. Furthermore, it maintains low subthreshold swing (SS) of 29.3 mV/dec indicating its potential for low-power applications.

Keywords: Ambipolarity; Gate overlapping; TFET; Tunnelling barrier width

1 Introduction

The MOSFET has faithfully served us for many years, with the majority of integrated circuits built using MOS technology. However, as further scaling becomes increasingly complex, achieving greater performance from MOS technology becomes more challenging. Due to the numerous drawbacks of MOSFET when scaled down to deep sub-micron regimes, the growing demand for low-power devices prompts us to explore alternatives to MOSFETs.

As technology has advanced, scaling of MOS devices has led to poor subthreshold swing (SS) and various second-order effects, such as mobility reduction, the hot carrier effect, and a substantial increase in leakage currents[1-4]. As a prospective low-power device for future technology, the TFET stands out as one of the most interesting and prominent devices. Unlike traditional MOSFETs, where current conduction occurs through a thermionic emission mechanism, with carriers injecting from the source to the channel region across an energy barrier, TFETs utilize the band-to-band tunnelling (BTBT) concept. TFETs are gated p-i-n FETs, with 'p' and 'n' representing the types of semiconductor materials used for the source and drain regions, while 'i' represents the intrinsic (undoped) channel region. TFETs are preferred over MOSFETs due to their improved subthreshold swing, which is less than 60 mV/dec, and small leakage current[5-11]. The lower subthreshold swing helps minimize power requirements and improves voltage headroom at lower supply voltages.

The significant challenges encountered by TFET are (i) low ON-state current (I_{ON}) and (ii) ambipolar leakage. Low I_{ON} results from inadequate electron tunnelling from the source to the channel, limiting the potential use of TFETs in high-performance applications[12-16]. Ambipolar conduction is a unique property that allows current flow at high negative gate voltages, restricting the usage of TFETs in digital circuit applications[6,17].

Several approaches have been made to improve the ON-state current, such as using double gate architectures[8,18] and introducing high-k dielectric and low bandgap materials[19-22]. High-k dielectric materials increase the lateral electric field, thereby boosting the I_{ON}. Introducing pockets of small bandgap material near the tunnelling region decreases the tunnelling width, resulting in increased I_{ON}[23]. For reducing ambipolar leakage, several approaches have been reported, including (i) using heterogeneous gate dielectrics to decrease the drain-side electric field[24], and (ii) employing gate overlapping on drain

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techniques to control the tunnelling barrier width for different gate voltage polarities[25]. The above-mentioned techniques are useful for improving either ON-state current or ambipolar leakage. The aim of this effort is to enhance the speed performance of TFET along with improved ambipolarity. Therefore, it must have a low SS_{avg}, a high I_{ON}/I_{OFF} ratio, and a low I_{amb} to be suitable for low-power applications. In this paper, a systematic investigation is conducted to understand the effect of hetero gate dielectric and gate overlapping on the drain. This study explores various device-level engineering solutions to address the aforementioned challenges of TFET structures. The proposed structure is named GDHD-TFET, which improves the ON-state current and ambipolar leakage simultaneously.

The paper is organized into subsequent sections. Section II describes the device design flow. Section III presents comparative results along with their explanation. Section IV provides an explanation of the optimized structures. Finally, Section V presents the overall conclusion of this paper.

2 Device Geometry and Simulation Methods

Figure 1 illustrates the structural view of the Traditional TFET (T-TFET), the Gate overlapping on drain TFET (GD-TFET) with an overlapping length (L_{OV}=30nm)[25], the Hetero gate dielectric TFET (HD-TFET), and the Gate overlap on the drain with Hetero gate dielectric TFET (GDHD-TFET)

Figure 2 shows the block diagram of the potentially feasible fabrication stages for the proposed GDHD-TFET, along with the flow chart in Fig. 3. The fabrication process carried out as in[26-28]. The p-i-n layers can be formed using an epitaxial technique as shown in Fig. 2(a). Fig. 2(b) shows deposition of SiO_2 layer and Fig. 2(c) shows selective etching for extended source drain regions. In the next step ion implementation is taking place as shown in Fig. 2(d). Fig 2(e) shows the deposition of HfO_2 by masking SiO_2 layer. Lastly, to develop the contacts of the source and drain region metallization and patterning for the front gate and back gate shown in Fig. 2(f), Fig. 2(e).

The simulation is performed by calibrating the data reported in[8] using Sentaurus TCAD simulator[29], as depicted in Fig. 4. To analyse Band-to-Band Tunnelling (BTBT), the simulation method utilizes the non-local BTBT model. Here, we consider the effect of phonon-assisted tunnelling, taking into account the parameter values (A = 2.2×10^{17} $cm^{-3}\cdot s^{-1}$ and B = 8.2×10^{6} MV cm−1). Additionally, tunnelling generation rates are examined during the tunnelling length of this device using this model Table 1. At lower dimensions, quantum confinement causes the continuous conduction and valence bands to split into discrete energy subbands, increasing the effective bandgap and reducing carrier mobility[30]. This modification results in higher tunnelling widths, significantly diminishing tunnelling currents. Consequently, the ON-state current levels are reduced, affecting the overall device performance in nanoscale transistors. For smaller dimensions (less than 10 nm), the effect of quantum confinement must be considered. In this work, the quantum potential model is incorporated to account for these quantum confinement effects.

3 Results and Discussion

In the T-TFET, the gate voltage plays a critical role in deciding the tunnelling width at either the source-channel or drain-channel junction, which in turn influences the device behaviour. By applying a

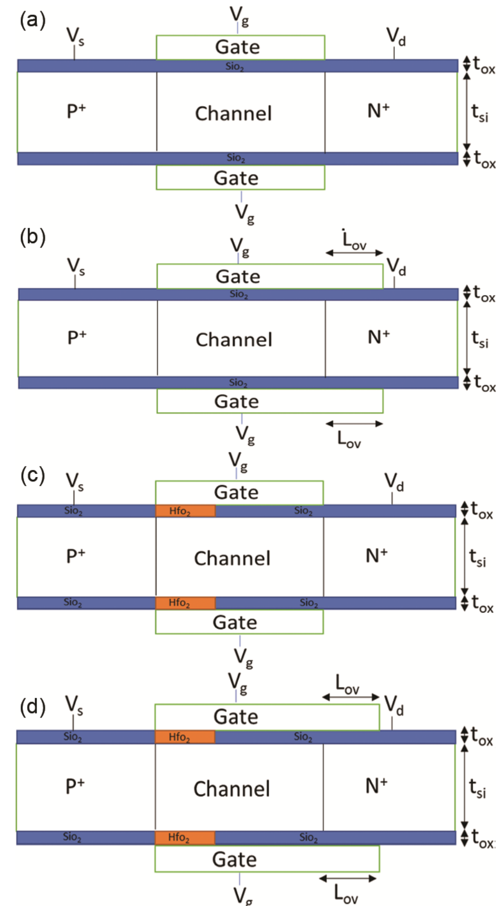

Fig. 1 — Structural images of (a) T-TFET, (b) GD-TFET (c) HD-TFET (d) GDHD-TFET (proposed device)

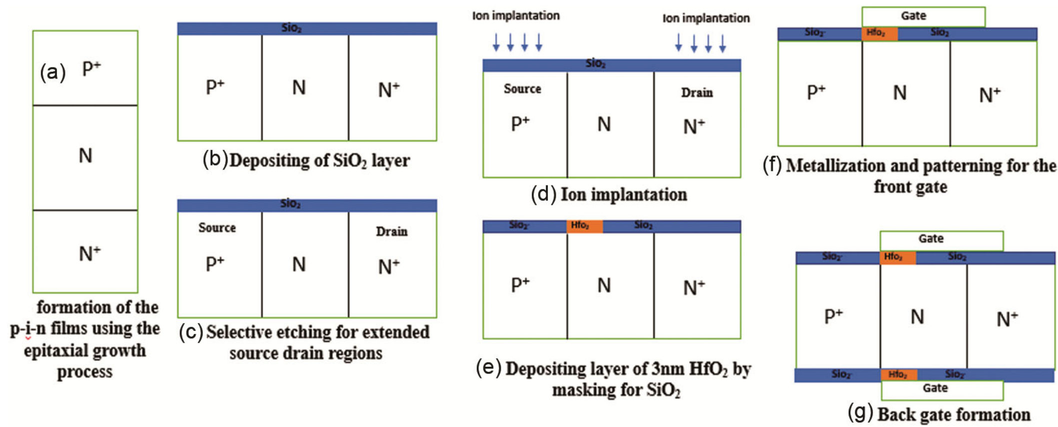

Fig. 2 — The manufacturing process block diagrams of the GDHD-TFET device

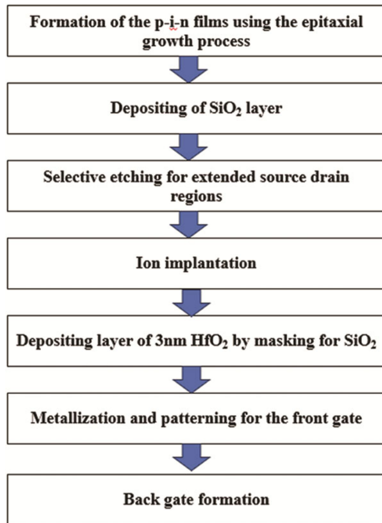

Fig. 3 — Flow chart of the GDHD-TFET device

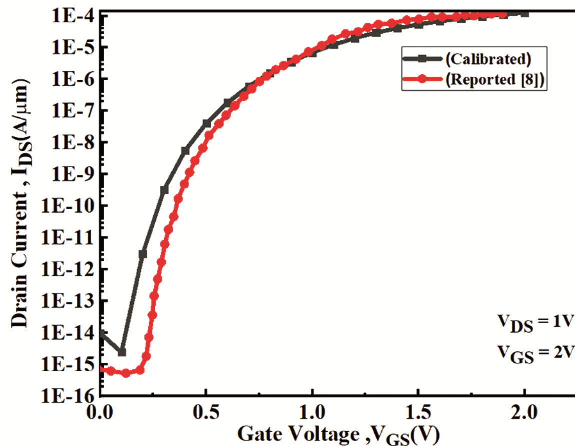

Fig. 4 — I_D VS V_{GS} Calibrated from the results described in[8]

positive gate bias, the conduction band energy at the source-channel junction is lowered. As a result, the effective width of the tunnelling barrier at the channel-source interface is reduced. This reduction in barrier width enhances the tunnelling probability of

Table 1 — Design Parameters for Device Simulation

Parameters	T-TFET	GD-TFET	HD-TFET	GDHD-TFET
Silicon film thickness (t_{si})	10nm	10nm	10nm	10nm
Oxide thickness (t_{ox})	3nm	3nm	3nm	3nm
Length of channel (L)	50nm	50nm	50nm	50nm
Gate length	50nm	80nm	50nm	80nm
Work function	4.5eV	4.5eV	4.5eV	4.5eV
Source doping(N_A)	$10^{20}/cm^3$	$10^{20}/cm^3$	$10^{20}/cm^3$	$10^{20}/cm^3$
Channel doping(N_D)	$10^{17}/cm^3$	$10^{17}/cm^3$	$10^{17}/cm^3$	$10^{17}/cm^3$
Drain doping(N_D)	$10^{19}/cm^3$	$10^{19}/cm^3$	$10^{19}/cm^3$	$10^{19}/cm^3$

carriers, leading to increased current flow. An ON-state current is produced as a result of charge carriers tunnelling from the source to the channel due to the narrowing of the barrier. On the other hand, negative gate bias leads to an onset of ambipolar behaviour of TFET because it reduces the tunnelling barrier of the drain-channel interface. The use of TFET is limited for complementary digital circuit applications because of the ambipolar current conduction.

To effectively suppress ambipolar current, the OFF-state tunnelling barrier should remain sufficiently wide to prevent the undesired flow of carriers from the drain to the channel, regardless of the polarity of the gate voltage. Maintaining an adequate OFF-state current and tunnelling barrier width at the drain-channel junction is crucial to minimize ambipolar conduction and achieve proper FET functionality. When a negative gate voltage is applied to a TFET, and if the gate is overlapped on the drain, it creates a depletion region at the drain-channel interface. By depleting the charge carriers in the drain-channel interface, the width of the tunnelling barrier at that junction is increased, preventing the flow of charge carriers from the drain to the channel. The corresponding structure that helps minimize ambipolar conduction is shown in Fig. 1(b), named GD-TFET. The use of high-k gate oxide at the

source side (see Fig. 1(c)) results in a higher ON-state current. Investigation of the proposed device (GDHD-TFET) is conducted to explore the cause of improvement in ON current and ambipolar conduction.

Figure 5 depicts the transfer characteristics of all structures for VDS = VGS = 1.0V. Without any bias voltage at the gate terminal, the device transitions into the OFF state due to a large energy gap between the source-channel regions. When a positive gate voltage is applied, the electric field across the source-channel

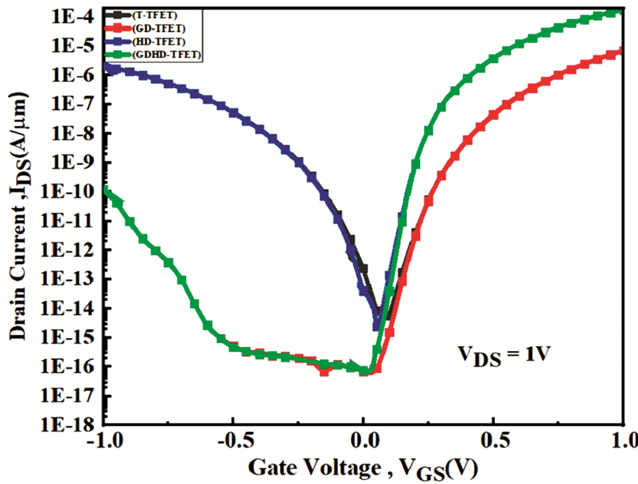

Fig. 5 — I_{DS}-V_{GS} characteristics of (a) T-TFET, (b) GD-TFET (c) HD-TFET (d) GDHD-TFET (proposed device)

junction increases in the proposed device (GDHD-TFET). This results in 10^2times increase in ON current compared to T-TFET. The carriers across the drain-channel interface deplete due to gate-drain overlap with negative gate bias. In the proposed device, the tunnelling width across the drain-channel interface increases, leading to a reduction of ambipolar current by 10^4 times compared to T-TFET.

Figure 6 describes the band diagrams for the T-TFET, GD-TFET, HD-TFET, and GDHD-TFET at different bias conditions. The tunnel barrier width of the channel-source interface and channel-drain interface is found to be 6.6 nm and 10.7 nm for positive and negative gate bias, respectively (see Table 2). As shown in Fig. 6(b), when the positive gate bias is applied to GD-TFET, the tunnelling width of the source-channel interface is close to the T-TFET case. However, the charge carriers across the drain-channel interface are depleted for negative gate voltage due to gate overlapping on the drain. Interestingly, the ambipolar conduction is suppressed because of an increase in the tunnelling width of the drain-channel junction by 183% (10.7 nm to 30.3 nm) as shown in Fig. 5.

Figure 6(c) shows the band diagram of HD-TFET. The tunnel barrier width of HD-TFET is 4.7 nm at the source-channel interface, which is lower than that of

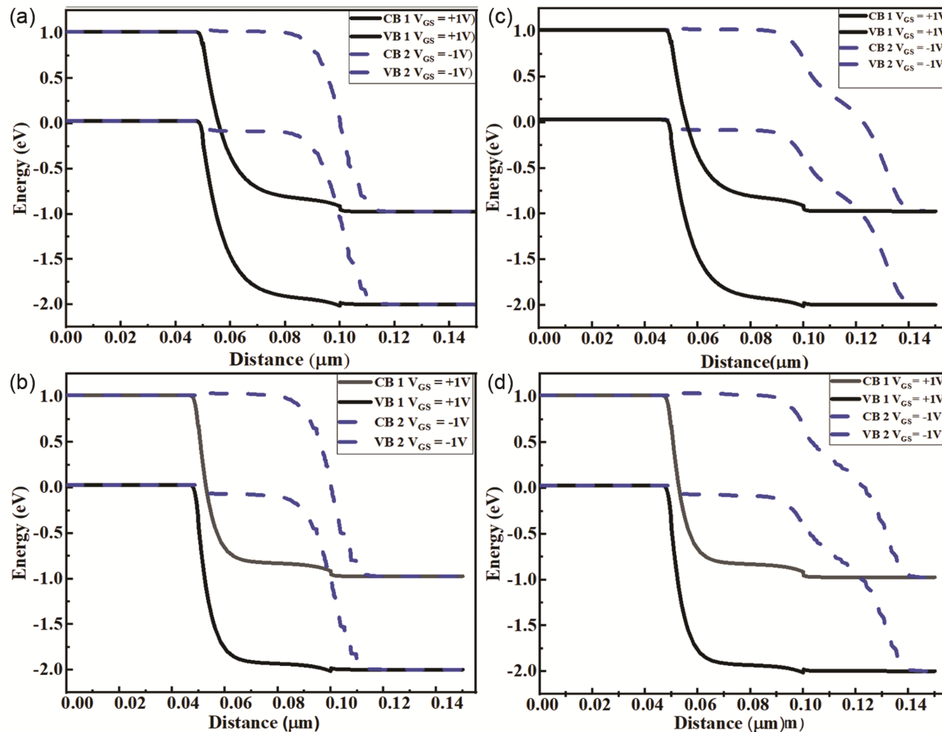

Fig. 6 — Energy-band diagrams of (a) T-TFET (b) GD-TFET (c) HD-TFET (d) GDHD-TFET with L_{ov} = 30 nm

GD-TFET and T-TFET. In HD-TFET, the screening of the electric field improves because of the high-k dielectric near the channel-source junction, resulting in improved ON-state current as shown in Fig. 5. In the case of HD-TFET, the tunnelling barrier width is reduced by 28% (6.6 nm to 4.7 nm) compared to T-TFET as shown in Table 2. For negative gate voltages, the tunnelling barrier width of the channel-drain junction is 12.3 nm, close to the drain-channel barrier width (10.7 nm) of T-TFET. Due to this, the ambipolar current characteristics of HD-TFET and T-TFET overlapped, as shown in Fig. 5. Fig. 6(d) shows the energy band diagram of GDHD-TFET. For positive gate bias, the source-channel junction's barrier width is reduced by 28% compared to T-TFET. Interestingly for negative gate voltages, the tunnelling barrier width at the channel-drain junction is increased by 178% (10.7 nm to 29.8 nm) compared to T-TFET. As a consequence, there is an increase in ON-state current by a factor of 10^2 and a reduction in ambipolarcurrent by a factor of 10^4.

Figure 7 represents the electric field diagram of T-TFET and GDHD-TFET. In T-TFET, for positive gate bias, the peak electric field across the source-channel interface is 1.99 MV/cm. However, in the GDHD-TFET case, the high-k dielectric near the channel-source interface increases the peak electric field by 42% (1.99 MV/cm to 2.83 MV/cm) as shown in Fig. 7. Due to this, the tunnelling barrier width is reduced by 1.8 nm (see Table 2), and the ON current is increased by a factor of 100 (see Table 3).

Table 2 — Tunnel barrier widths in ON and OFF states

Structure	Tunnel Barrier width (source–channel) ON-state	Tunnel Barrier width (drain–channel) OFF state
T-TFET	6.6nm	10.7nm
GD-TTFET	6.7nm	30.3nm
HD-TFET	4.7nm	12.3nm
GDHD-TFET	4.8nm	29.8nm

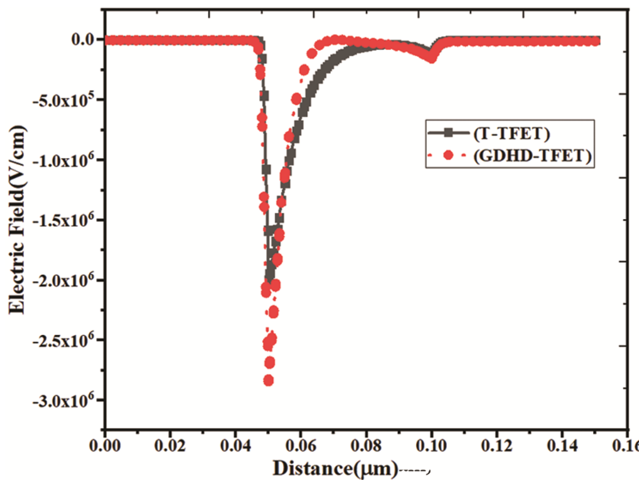

Fig. 7 — Electric field representation of T-TFET, GDHD-TFET in ON-state

The band-to-band (BTBT) tunnelling profiles in the ON and ambipolar states of T-TFET and GDHD-TFET structures are shown in Figs 8 & 9. During the ON state, the maximum BTBT rate in T-TFET is 5.6×10^{30} $cm^{-3}s^{-1}$ (see Fig. 8(a)). However, in the case of GDHD-TFET, we can observe a stronger tunnelling profile with an enhanced BTBT rate by 10^2 times (5.6×10^{30} $cm^{-3}s^{-1}$ to 1.3×10^{32} $cm^{-3}s^{-1}$) due to the high-k gate dielectric, as shown in Fig. 8(b). In the ambipolar state, the maximum BTBT rate at the drain-channel junction in T-TFET is 4.2×10^{29} $cm^{-3}s^{-1}$ (see Fig. 9(a)). Nevertheless, in the case of GDHD-TFET, the BTBT rate across the drain channel is reduced by 10^{11} times (4.2×10^{29} $cm^{-3}s^{-1}$ to 4.8×10^{18} $cm^{-3}s^{-1}$) due to gate-drain overlap, as shown in Fig. 9(b).

The performance characteristics of T-TFET, GD-TFET, HD-TFET, and GDHD-TFET structures are shown in Table 3. When compared to T-TFET, HD-TFET shows a 100 times improvement in ON-state current, and the SS decreased by 46% while maintaining a good I_{ON}/I_{OFF} ratio of 10^{14}. Similarly, when compared with T-TFET, GD-TFET shows a 10^4 times decrement in ambipolar leakage, and the SS decreased by 36%. The proposed device (GDHD-TFET) shows better results compared to T-TFET with a 100 times improvement in ON current and a reduction in ambipolar leakage by 10^4 times, maintaining a low SS and a high I_{ON}/I_{OFF} ratio of 29.3 mV/dec and 10^{13}, respectively. By comparing all the performance characteristics, GDHD-TFET shows a better improvement in ON current, OFF current, ambipolar leakage, and SS.

4 Optimization

In this section, Table 4 represents the variation of ON current (I_{ON}) with the change in ratio of dielectric lengths HfO_2, and SiO_2 with fixed overlapping lengths (L_{ov}) as 10nm, 20nm, and 30nm. For the overlapping length of 10nm, the corresponding ON current for the dielectric length ratios 0.25, 0.66, 1.5, and 4 are 1.62×10^{-4}, 1.73×10^{-4}, 1.73×10^{-4}, 1.72×10^{-4} A/µm. For the overlapping length of 20nm, the corresponding ON current for the dielectric length's ratios 0.25, 0.66, 1.5, and 4 are 1.62×10^{-4}, 1.73×10^{-4},1.73×10^{-4}, 1.72×10^{-4} A/µm. In a similar manner for the overlapping length of 30nm, the corresponding ON

Table 3 — Shows the comparison between T-TFET, GD-TFET, HD-TFET, GDHD-TFET

Structure	I_{ON} (A/µm)	I_{OFF} (A/µm)	Sub Threshold Swing (S.S) ($\frac{mV}{decade}$)	$I_{Ambipolar}$ (A/µm)
T-TFET	7×10^{-06}	2.01×10^{-18}	49.2	2.1×10^{-06}
GD-TFET [25]	7×10^{-06}	7.26×10^{-17}	31.2	1.23×10^{-10}
HD-TFET [24]	1.73×10^{-04}	1.95×10^{-18}	26.5	2.1×10^{-06}
GDHD-TFET (proposed)	1.73×10^{-4}	6.94×10^{-17}	29.3	1.23×10^{-10}

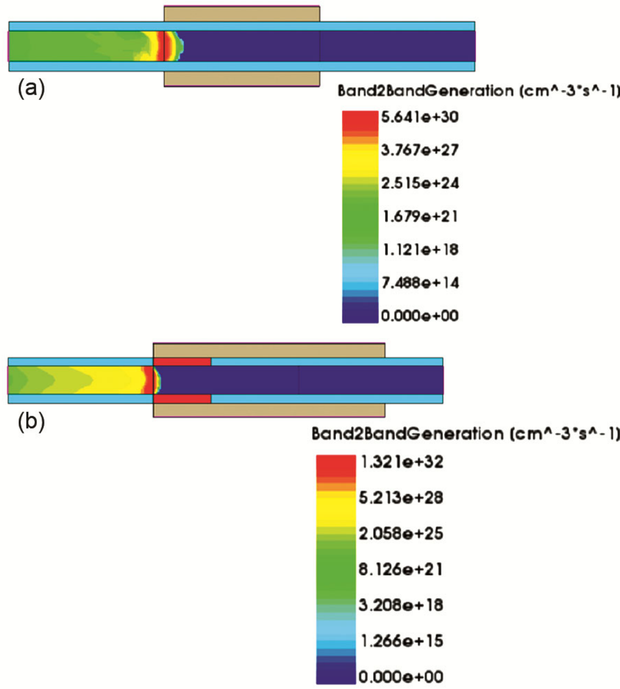

Fig. 8 — Electron band-to-band generation rate in ON-state for (a) T-TFET (b) GDHD-TFET

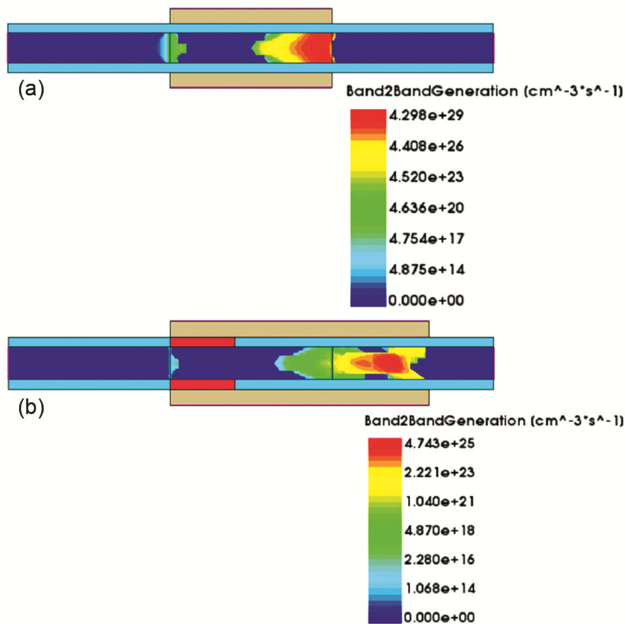

Fig. 9 — Electron band-to-band generation rate in ambipolar-state for (a) T-TFET (b) GDHD-TFET

Table 4 — I_{ON} with respect to change in ratio of dielectric lengths with fixed overlapping length (L_{ov})

Ratio of dielectric lengths	I_{ON} (A/µm) (L_{ov} = 10nm)	I_{ON} (A/µm) (L_{ov} = 20nm)	I_{ON} (A/µm) (L_{ov} = 30nm)
0.25	1.62×10^{-4}	1.62×10^{-4}	1.62×10^{-4}
0.66	1.73×10^{-4}	1.73×10^{-4}	1.73×10^{-4}
1.5	1.73×10^{-4}	1.73×10^{-4}	1.73×10^{-4}
4	1.72×10^{-4}	1.72×10^{-4}	1.72×10^{-4}

current for the dielectric length's ratios 0.25, 0.66, 1.5, and 4 are 1.62×10^{-4}, 1.73×10^{-4}, 1.73×10^{-4}, 1.72×10^{-4} A/µm. By varying the ratio of dielectric lengths from 0.25 to 4, the ON-state current is increased from $1.62\times10^{-4}$to 1.73×10^{-4}. By employing the technique of Hetero gate dielectric to reduce the tunnel barrier width at the source-channel interface in ON state, a better ON current of 1.7×10^{-4} was observed at the ratio of 0.66 (with the length of HfO_2 and SiO_2 as 20nm and 30nm).

Figure 10 represents the variation of ambipolar current (I_{Amb}) with the change in ratio of dielectric lengths HfO_2, and SiO_2 with fixed overlapping lengths (L_{ov}) as 10nm, 20nm, and 30nm. For the overlapping length of 10nm, the ambipolarconduction is reduced from 2.1×10^{-06} to 1.7×10^{-07} A/µm (10 times) in comparison with T-TFET. For the overlapping length of 20nm, the ambipolar current is reduced from 2.1×10^{-06} to 5.1×10^{-10} A/µm (10^4 times). In a similar way, for the overlapping length of 30nm, the ambipolar current is reducedfrom 2.1×10^{-06} to 1.23×10^{-10} A/µm (10^4 times). Ambipolar current is optimally reduced from 10^{-7} to 10^{-10} A/µm with a change in overlapping lengths from 10nm to 30nm. It is observed in Fig. 10, that the ambipolar current is improved at overlapping lengths of 30nm. By employing the technique of Gate overlap on drain to increase the tunnel barrier width at the drain-channel interface in OFF state, a better Ambipolar current of 1.23×10^{-10} was observed with the length of HfO_2 and SiO_2 chosen to be 20nm and 30nm, respectively, at overlapping lengths of 30nm.

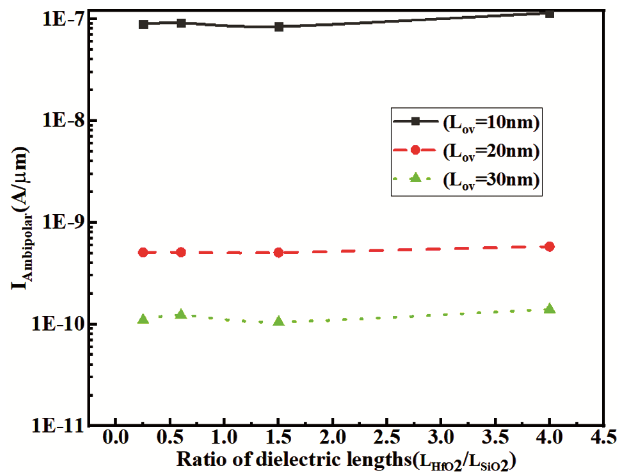

Fig. 10 — $I_{Ambipolar}$ with respect to change in ratio of dielectric lengths with fixed overlapping length (L_{ov})

5 Conclusion

In conclusion, this study presents the GDHD-TFET structure as a significant advancement in TFET technology, offering substantial improvements in ON-state current and ambipolarity. Through a comprehensive investigation of gate overlapping on the drain with hetero-gate dielectric, present research demonstrates unprecedented enhancements in device performance compared to conventional TFET designs. By achieving a 10^2times increase in ON current and a 10^4 times reduction in ambipolar current, alongside maintaining favourable SS and I_{ON}/I_{OFF} ratios, the GDHD-TFET presents a promising solution for addressing the challenges of TFET devices for low-power applications. Furthermore, the exploration of design optimization parameters, such as overlapping length and dielectric length ratio, provides valuable insights for future advancements in TFET technology, particularly for emerging technology nodes.

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