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Performance Comparison of Junctionless FinFET with Nanosheet FET and Device Design Guidelines

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In this paper, the junctionless Fin Field Effect Transistor (FinFET) and nanosheet Field Effect Transistor (NSFET) with a gate length of 12 nm are implemented using the Sentaurus Technology Computer-Aided Design (TCAD) tool. To compare the junctionless FinFET and NSFET, simulations are done at constant threshold voltage. The NSFET outperformed FinFET in terms of current driving capabilities, Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), and intrinsic voltage gain (A_V). Further, the device design guidelines are presented for FinFET and NSFET in terms of geometrical parameters. The simulation indicates that downscaling the gate length from 16 to 8 nm leads to an increase in SS and DIBL by 21 and 68.49 % in FinFET whereas 19 and 70.14 % in nanosheet FET. The height variation of FinFET seems to make the least impact on short channel effects (SCEs) while scaling the thickness of NSFET from 9 to 5 nm improves the DIBL and SS by 61.9 % and 15.54 % respectively. In the case of scaling the width of FinFET from 10 to 5 nm, DIBL and SS increase by 55.4 % and 14 % whereas scaling of nanosheet width from 24 to 12 nm gives 19.44 % and 1.37 % improvement in DIBL and SS, respectively.

Keywords: FinFET; Gate all around (GAA); Junctionless; Nanosheet; Short channel effects (SCE)

1 Introduction

These days devices with minimum power requirements, small in size, and having high speed are in demand. It can only be realized by reducing the device dimensions which could become possible with the advent of junctionless transistors[1]. Also, the short channel effects in the devices degrade the device features and limit further downscaling of the channel length, so JLTs may be utilized to overcome these issues. The junctionless devices have the potential to operate fast and may be utilized to work for ultra-low power applications[2].

In the case of FinFET, the channel between source and drain is the shape of a fin, this fin supports the fin wrapping from three sides. In comparison to the planar MOSFET, FinFET started to take a place in the semiconductor industry due to its performance improvement in terms of area and power for SOC (System on Chip) applications. However, some technical dreads need to be considered. Fins with reduced heights are required to achieve better electrostatics but at the cost of an increase in threshold voltage (V_{th}). Fin depopulation moved the research in the direction of nanosheet FET.

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The structure of the nanosheet may be understood by the concept of Gate All Around (GAA) transistors[3,4,5]. Under the concept of nanosheet technology, the gate covers the channel region from all four sides. This wrapping of the channel by the gate in all four directions provides more and better control as compared to FinFET. In nanosheet FET, the current driving capability can be enhanced by increasing the channel effective width (W_{eff}) under the same footprint. The relatively wider width of the nanosheet provides an edge to drive more current. So it could be a promising device for upcoming electronics applications. Gate all-around (GAA) field effect transistors offer better device performance, low power consumption, and low leakage current.

In the case of FinFET and nanosheet FET, the performance of the device can be enhanced by adding more fins and sheets to the basic FinFET and nanosheet unit. It is observed that with the increase in the number of sheets every time the ON-to-OFF current ratio (I_{ON}/I_{OFF}) increases and the short channel effect improves. The nanosheet has the advantage of delivering better control over short channel effects[6-10,14]. Moreover, the dimension optimization of fins and nanosheets like the length of the gate, width, channel thickness, or fins height plays an important role in

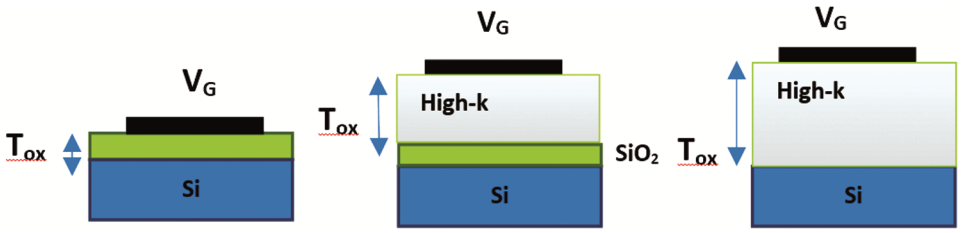

Fig. 1 — Structures depicting the same EOT with (a) SiO_2(b) a thin layer of SiO_2 followed by a layer of High-k oxide (c) a thick layer of high-koxide[15]

determining the analog /RF performance of the device[11,12,13]. The short channel effects restrict the further reduction of the channel length, so multigatejunctionless FinFET or nanosheet FET offers an advantage to mitigate these concerns.

To the best of our knowledge, many Comparative studies on FinFET and nanosheet FETs[12,13,18,28] exist. However, their device dimensional analysis based on geometrical parameter variation under a single frame still needs to be covered. This comparison is very important to get better device design insight to bring the technology to the next futuristic node.

This paper targets, the junctionless multi-fin FinFET comparison with multi-channel nanosheet FET at a specific gate length of 12 nm. These results demonstrate the supremacy of multi-channel nanosheet FET over multi-fin FinFET. Further to enhance the performance of junctionless transistors, the device design guidelines are given that help to determine how the geometrical parameters of the device make an impact on the electrical characteristics. The paper is organized in the following way. The device structure used for the comparison of FinFET and multi-channel nanosheet FET, simulation set-up, and result analysis are presented in section 2. Section 3 covers the device design guidelines that include the impact of the variation of geometrical parameters. Under section-4 the conclusion is drawn.

2 Device structure, Simulation Set-Up, and Result Analysis

2.1 Device Structure and Simulation Set-up

The designed structures of nanosheet FET and FinFET are simulated using Sentaurus TCAD[14] with a gate length of 12 nm. In the proposed structure, a thin layer of SiO_2 (having thickness T_{SiO2}=0.5 nm) followed by a layer of high-k dielectric material (having thickness T_{HfO2}=1.5 nm) is deposited to obtain an EOT of 0.76 nm. This layer of high-k dielectric over the SiO_2 changes its effective oxide thickness

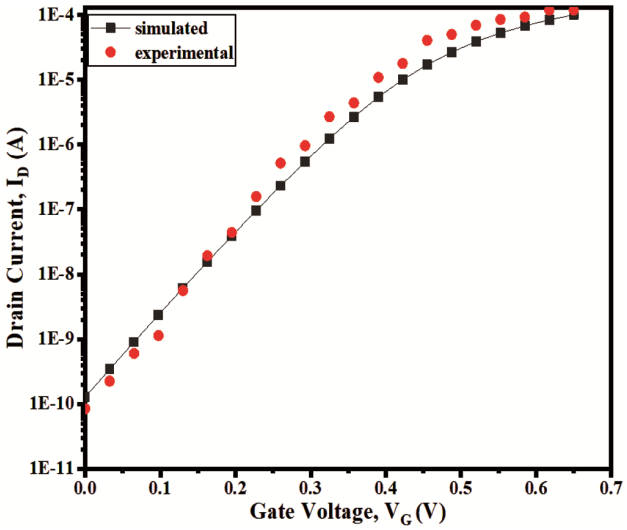

Fig. 2 — Calibration of the simulated structure with experimental data[7]

(EOT). The usage of high-k dielectric provides the same EOT with a thick physical layer as provided by SiO_2 (Fig. 1) alone. Though the use of a thin oxide layer increases the gate leakage current, the use of a thick oxide layer diminishes the control of the gate over the channel[15]. So, to achieve enhanced performance, the thickness of the gate stack should be adjusted and a layer of thin deposited SiO_2 followed by high-k dielectric may be used to get the worthy results. The thickness of the high-k dielectric layer may be evaluated by the relation given by Eq. 1[15].The simulation setup is well calibrated with the experimental results[7] and is presented in Fig. 2.

The 3-D view of both the FETs are shown in Figs. 3 & 4. At the base of both the structures a layer of buried oxide is used which helps to minimize the leakage current.

$$T_{high-k} = (EOT - T_{SiO2}) \times \frac{K_{high-K}}{K_{SiO2}} \quad \ldots (1)$$

For the simulations of the stated structures the models that are included are as fermi dirac and slotboom bandgap narrowing model to account for

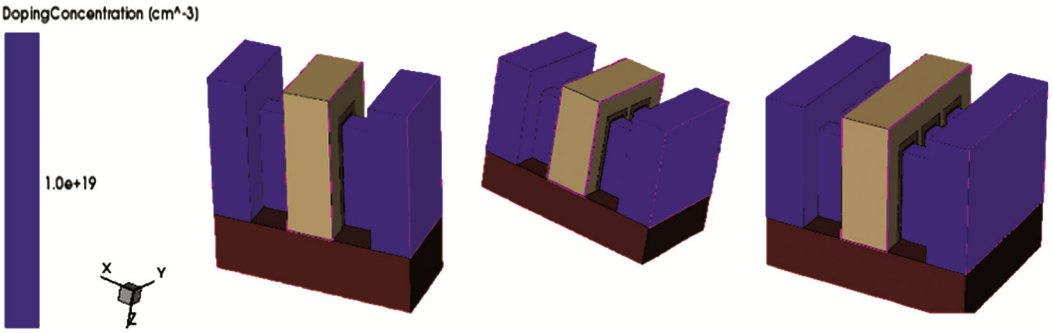

Fig. 3 — FinFET structures with (a) one-fin (1fin), (b) two-fin (2fin), and (c) three-fin (3fin) respectively

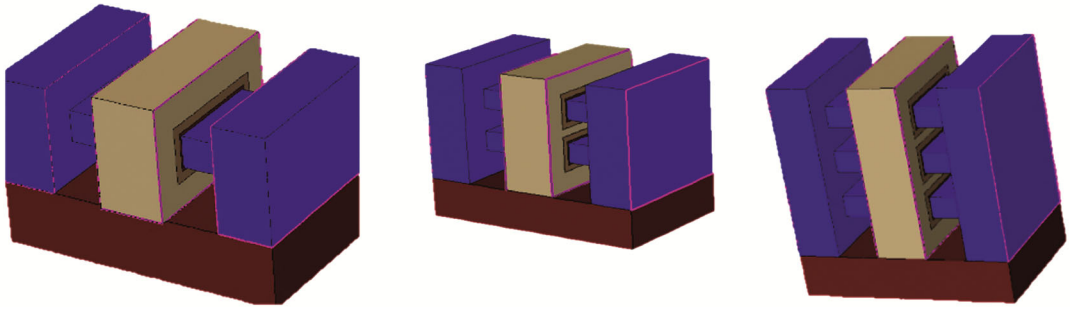

Fig. 4 — Nanosheet FET structures with (a) one-channel (1ns), (b) two-channel (2ns), and (c) three-channel (3ns)

heavy doping in junctionless transistors, the SRH model to account for the recombination effects, the density gradient model is used to consider the influence of quantum effects, Lombardi mobility model is incorporated to add the impact of various scattering phenomenon in the device. The effective width (W_{eff}) of multi-fin FinFET and multi-channel nanosheet FET are also evaluated. This W_{eff} is used to get the effective drain current value (I_{Deff}). Also, the electrical characteristics of multi-fin FinFET with multi-channel nanosheet FET are analyzed at a gate length of 12 nm. The detailed geometrical parameters used in the simulation are enumerated in Table 1.

Table 1 — Geometrical parameters used for the simulation

S. No.	Parameters	Values
1.	Gate length (L_{gns})	12 nm
	Gate length (L_{gfin})	12 nm
2.	Source-Drain doping concentration	1×10^{19}(n-type)
3.	Channel doping concentration	1×10^{19}(n-type)
4.	nanosheet thickness (T_{ns})	5 nm
	nanosheet width (W_{ns})	18 nm
5.	fin height (H_{fin})	18 nm
	fin width (W_{fin})	5 nm
6.	Nanosheet spacing or fin spacing[32, 33]	6 nm
7.	SiO_2 thickness (T_{SiO2})	0.5 nm
	HfO_2 thickness (T_{HfO2})	1.5 nm
8.	Dielectric constant of SiO_2 and HfO_2	3.9 and 22
9.	Gate metal work function(ϕm)	4.9 eV

2.2 Result Analysis

In this section, the analysis of comparison between single, double, and three-fin FinFET with respective single, double, and three-channel nanosheet FET is done using the specified dimensions as mentioned in Table 1. The drain current (I_D) versus gate voltage (V_G) and drain current (I_D) versus drain voltage (V_D) curves are presented in Fig. 5. It confirms that the drain current rises each time, as we add the fins in the FinFET structure. The same trend is observed with the addition of each channel to the nanosheet FET. However, the value of drain current in a nanosheet is on the higher side concerning its value in a FinFET. The percentage increase in current in the case of single nanosheet FET with respect to single FinFET is 3.63 %, in double nanosheet FET with respect to double fins it is 2.21 %. In the case of three-channel nanosheet FET with respect to three-fins FinFET, this percentage increase in current is 2.27 %. The reason for this incremental change in current is due to the large width of nanosheet FET in comparison to FinFET which has the better control over the channel[16,17].The curves in Figs. 6(a & b) depict the behavior of the transconductance (g_m) and output conductance (g_{ds}) versus the effective drain current(I_{Deff}). The transconductance (g_m)[31] of the device is an important analog figure of merit and is expressed as

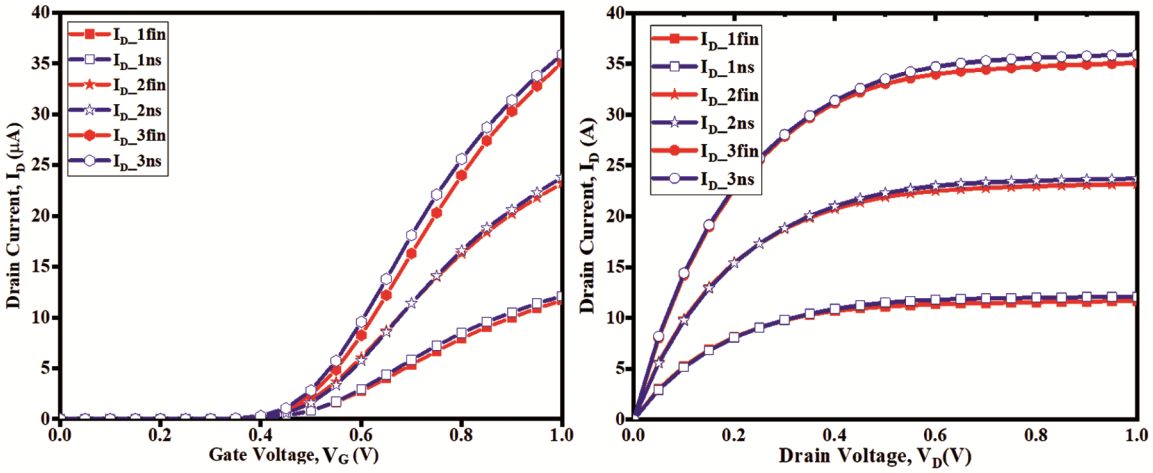

Fig. 5 — (a) Drain current (I_D) versus gate voltage (V_G) and (b) Drain current (I_D) vs drain voltage (V_D) curve of multi-fin FinFET and multichannel nanosheet FET

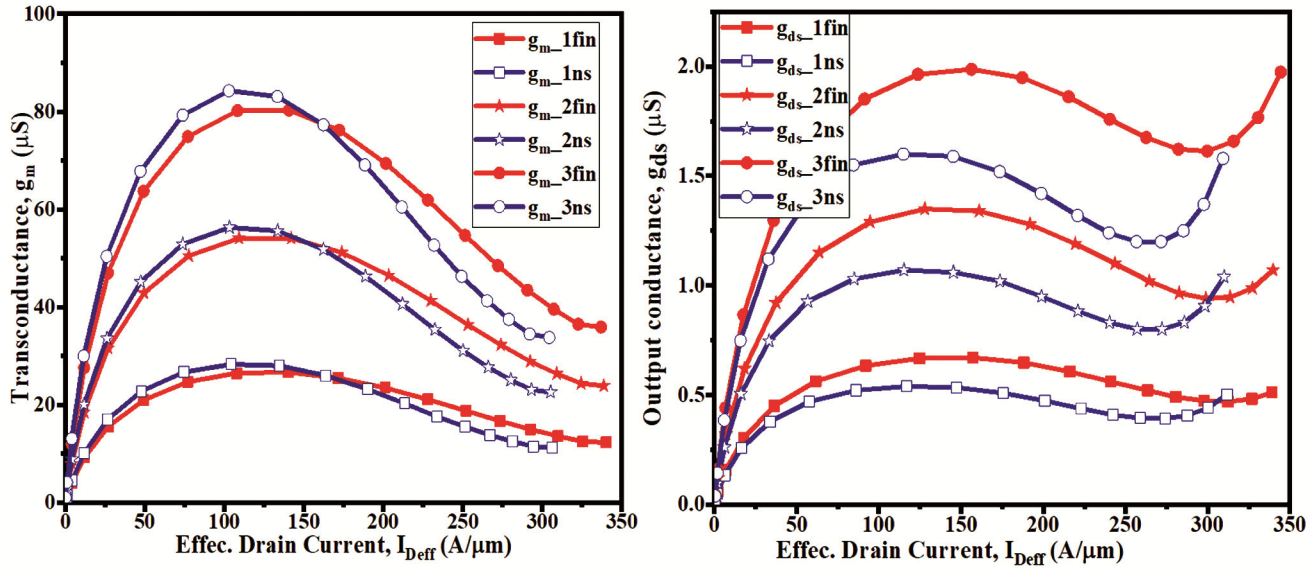

Fig. 6 — (a) Transconductance (g_m) and (b) output conductance (g_{ds}) curve versus effective drain current (I_{Deff}) of multi-fin FinFET and multi-channel nanosheet FET

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \quad \ldots (2)$$

It gives a relation between variations obtained in the drain current with the change of gate voltage. The higher value of transconductance of the devices is always desirable making it suitable for high-speed applications. The g_{ds} is expressed as the derivative of the I_D- V_D curve and Out of all the implemented structures of nanosheet, the structure having three nanosheet possesses the highest g_m. This is due to the high current driving capability of nanosheets with three channels. The g_{ds} of FinFET is more as compared to nanosheet and it increases each time, fins or nanosheet are added to the structure as shown in Fig. 6(b). The increase in g_{ds} hitch the gain of FinFET and hence FinFET has less gain compared to nanosheet FET. The low value of g_{ds} of nanosheet FET than FinFET decreases the output resistance and ensures the delivery of higher drain current[17].

The gate capacitance (C_{gg}) of the nanosheet with respect to I_{Deff} is shown in Fig. 7(a), it can be observed from the curve that the value of gate capacitances in nanosheet FET are attaining a higher peak in comparison to FinFET. The curves of single and three-fin FinFET are in close proximity with single and three-channel nanosheet FET respectively. Figure 7(b) shows the gain variations with respect to I_{Deff}. The curve indicates the high intrinsic voltage

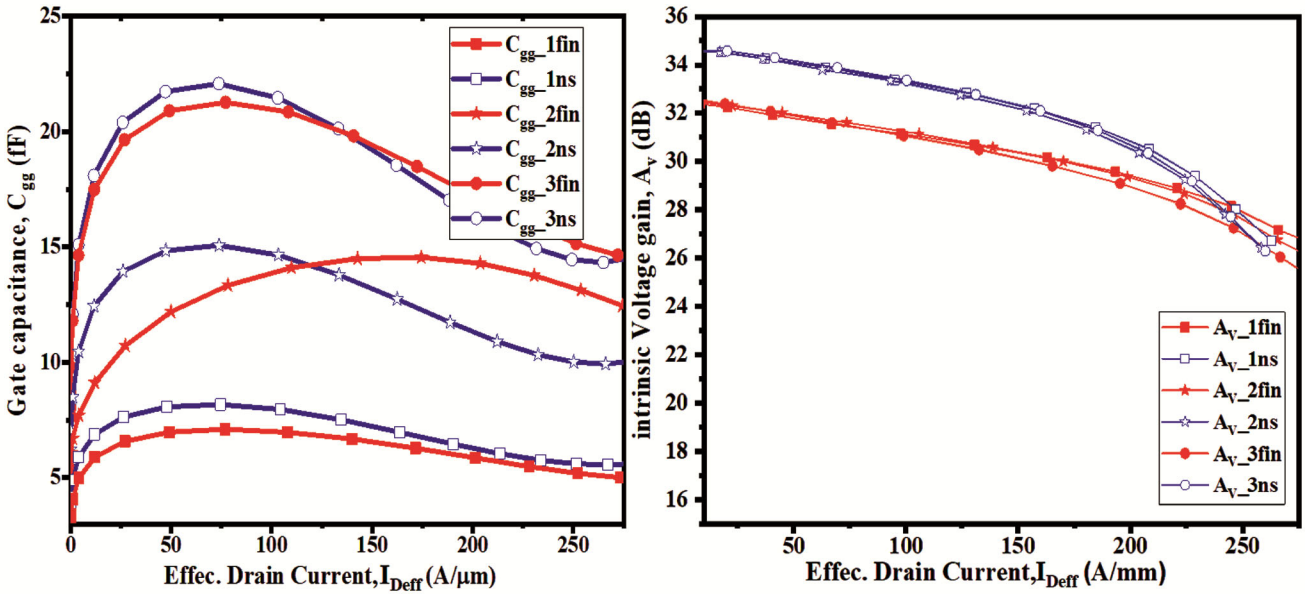

Fig. 7 — (a) Total Gate capacitance (C_{gg}) and (b) Intrinsic voltage gain (A_V) versus effective drain current (I_{Deff}) of multi-fin FinFET and multi-channels nanosheet FETs

gain of multi-channel nanosheet FET in comparison to multi-fin FinFET. The lower value of intrinsic voltage gain in FinFET is due to the high value of g_{ds}[18]. Fig. 8 shows the detailed analysis of SS and DIBL for single, double, and three-fins FinFET with single, double, and three-channel nanosheet FETs. The Subthreshold Swing and DIBL are evaluated using the Eqs. (3) and (4)

$$SS = \left(\frac{\delta \log_{10} I_D}{\delta V_{GS}}\right)^{-1} \quad \ldots (3)$$

$$DIBL = \frac{V_{tlin} - V_{tsat}}{V_{Dsat} - V_{Dlin}} \quad \ldots (4)$$

Both these values are less for the single, double, and three-layered nanosheet FET than the corresponding FinFET structures. The percentage improvement in SS and DIBL of single nanosheet FET with respect to single fin FinFET is 2.87 % and 16.32 % respectively. For double-channel nanosheet FET with respect to double-fin FinFET, this improvement is 0.39 % and 9.75 %. For three-channel nanosheet FET and three-fins FinFET, the percentage improvement of SS and DIBL is 2.89 % and 18.6%. After analyzing the results of single, double, and three-fins FinFET[19] with the corresponding one, two, and three-channel nanosheet FET, it is observed that nanosheet FET has much-improved performance parameters over the FinFET. Since the percentage variation in SS and DIBL of double-fins FinFET and double-channel nanosheet FETs are the least, so further investigation in terms of device design guidelines is done concerning these structures only.

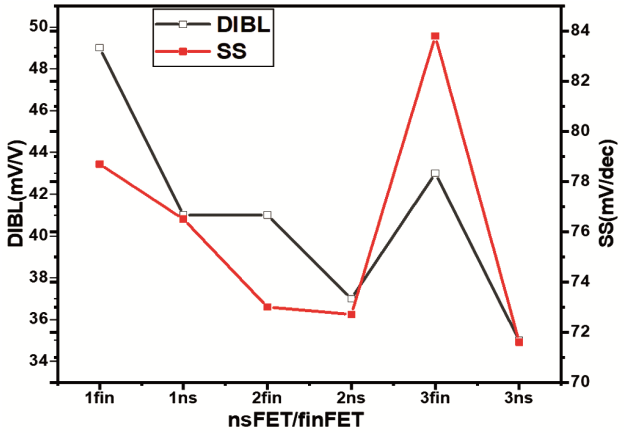

Fig. 8 — SS and DIBL of multi-fin FinFET and multi-channel nanosheet FET

3 Device design guidelines for multi-FinFET and multi-channel nanosheet FET

To define the optimized device guidelines for FinFET and nanosheet FET, the analysis proceeds with the variation in gate length from 16 nm to 8 nm.

All other dimensions are as per the Table 1. The individual analysis of double-channel nanosheet FET and double-fin FinFET has been shown to get a more significant insight into device design guidelines.

Under the first parameter "gate length", fin height and fin width are fixed at 18 nm and 5 nm while the width and thickness of the nanosheet are kept at

18 nm and 5 nm respectively. The effect of gate length variation on drain current (I_D), transconductance (g_m), gate capacitance (C_{gg}), and the cut-off frequency (f_T) are shown in Figs. 9-12 respectively. In the case of FinFET it is observed that under the analyzed gate length range, with a decrease in gate length, the OFF-state current increases. This increase in OFF-state current is 99.3 % at L_g= 8 nm with respect to its value at L_g=16 nm, this is due to the less resistance offered by the substrate region to the flow of current. With scaling down the gate length of the two-channel nanosheet, from L_{gns}=16 nm to 8 nm, the OFF-state current increases by large amount. This degrades the I_{ON}/I_{OFF} at reduced gate length of 8 nm. The increase in OFF–state current is significant from its value 9.03×10^{-15}A at L_{gns}=16 nm to 3.05×10^{-12} A at L_{gns}=8 nm. The threshold voltage (V_{th}) decreases with downscaling the gate length. The transconductance of FinFET and nanosheet FETs are shown in Fig. 10. In Fig. 10(b) the transconductance is highest corresponding to L_g=16 nm. This is due to the partial depletion of the channel. The gate length upscaling of both devices leads to a decrease in transconductance to a voltage of 0.7 V for FinFET and 0.63 V for

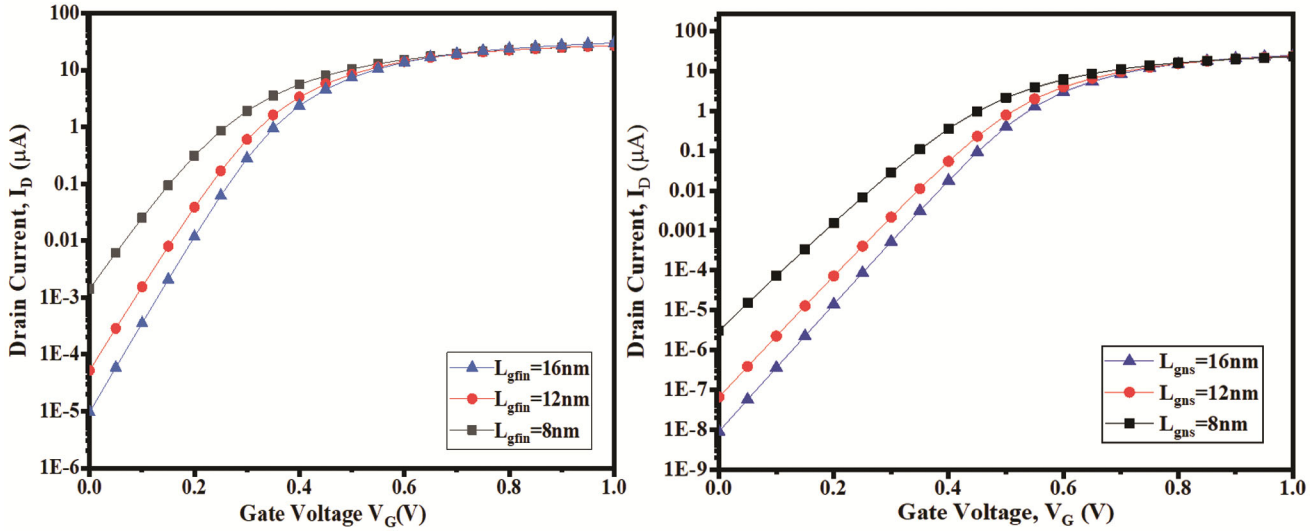

Fig. 9 — Drain Current (I_D) versus Gate Voltage (V_G) characteristics of (a) double-fin FinFET and (b) double channel nanosheet FET with variation in gate length

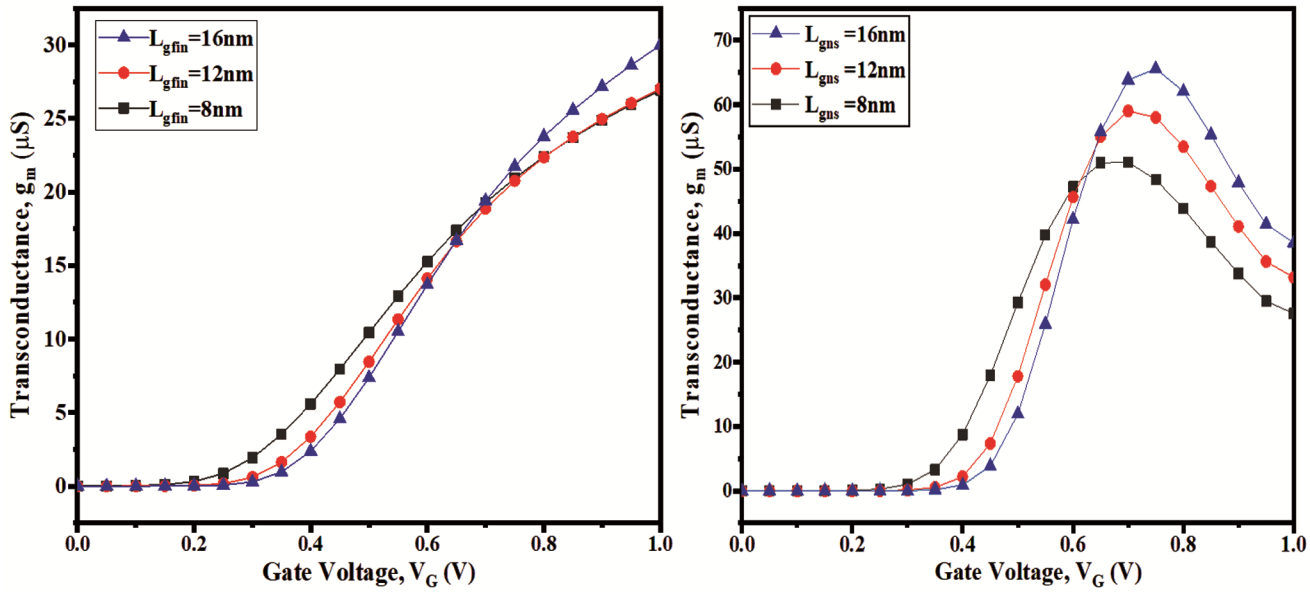

Fig. 10 — Transconductance (g_m) versus Gate Voltage (V_G) characteristics of (a) double-fin FinFET and (b) double-channel nanosheet with variation in gate length

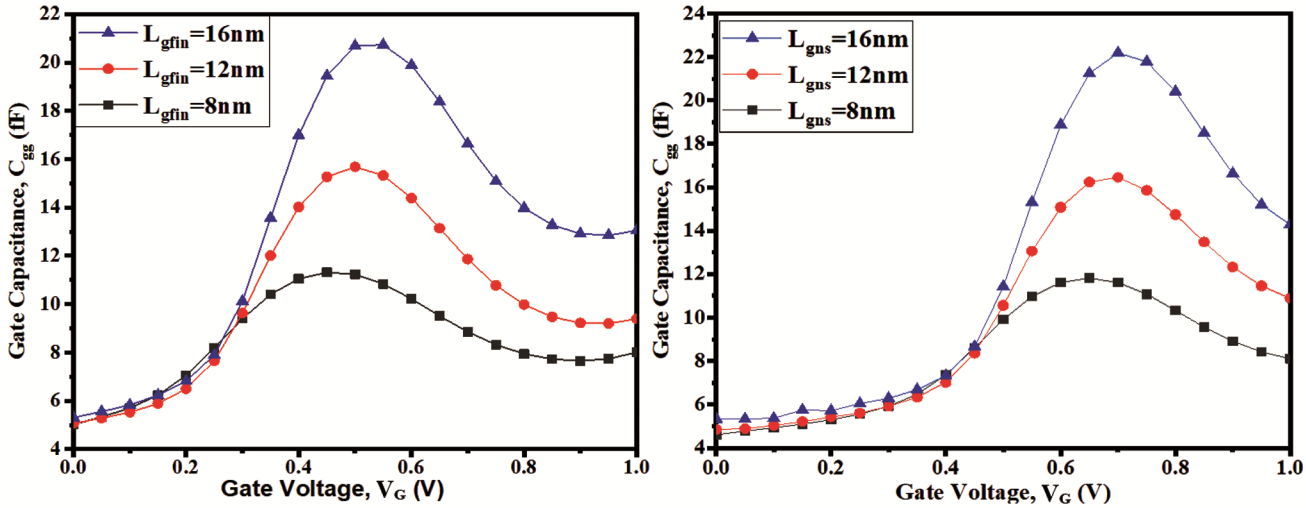

Fig. 11 — Gate Capacitance (C_{gg}) versus Gate Voltage (V_G) characteristics of (a) double-fin FinFET and (b) double-channel nanosheet with variation in gate length

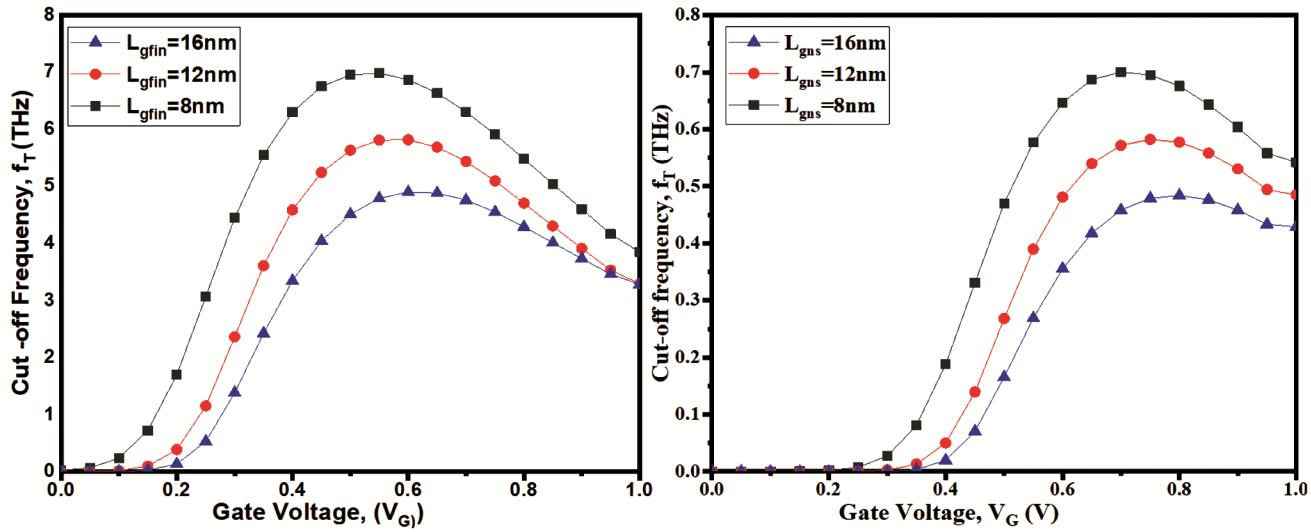

Fig. 12 — Cut-off frequency (f_T) versus gate voltage (V_G) characteristics of (a) double-fin FinFET and (b) double-channel nanosheet with variation in gate length

nanosheet. Thereafter the effect of coupling capacitance (Fig. 11) plays its role and leads to an increase in g_m corresponding to an increase in gate length.

The maximum increase in C_{gg} is observed for L_g=16 nm in both cases (Fig. 11). This increase in C_{gg} is due to the decreased depletion at high gate voltage. But after a particular point, there is a drop in C_{gg}[20]. The cut-off frequency (f_T) is a main constraint for analyzing the behavior of the device for high-frequency applications. The cut-off frequency (f_T) has a direct and inverse dependency on transconductance (g_m) and the gate capacitance (C_{gg}) given by the Eq. (5):[34]

$$f_T = \frac{g_m}{2*\prod*C_{gg}} \quad \ldots (5)$$

The cut-off frequency versus gate voltage curve is shown in Fig. 12. For the gate length of 8 nm, the cut-off frequency is the maximum among the gate lengths under analysis due to the reduced value of C_{gg}. With the increase in the gate length of FinFET and nanosheet FET, the DIBL and SS reduce significantly. This reduction is due to the decrease in subthreshold current.

Therefore, the variation in the SS and DIBL is such that corresponding to a gate length of 16 nm both the parameters improves, indicating the fast switching, and minimum SCEs at this channel length. With the downscaling of the gate length (L_g), the short channel effects increase. In the case of nanosheet, the increase

in DIBL and SS with a decrease in gate length from 16 nm to 8 nm is 70.14 % and 19 % respectivelyas shown in Fig. 13. For FinFET this increase in DIBL and SS is 68.49% and 21% respectively

The above discussion concludes that the devices having the large channel length are good in terms of getting good OFF-state current but the ON-state current variation is minute under the range from 16 nm to 8 nm. So an optimum gate length must be chosen. Drain current versus gate voltage curves specify that the OFF-state current in the nanosheet are much lower than the FinFET with little variation in ON current at workfunction of 4.62 eV. Also, the subthreshold swing and DIBL of nanosheet are better with respect to FinFET but with the downscaling in length both these characteristics deteriorate due to reduced barrier heightthat leads to reduced value of threshold voltage[21]. This helps the drain to make an impact over the channel. Therefore, a trade-off exists between the gate length chosen and the performance metric. At a gate length of 16 nm, though the OFF–state current, DIBL, and SS are favourable (improving) but at the cost of an increase in C_{gg} and reduced f_T. So, the gate length of 12 nm is fit to get the comparatively reduced OFF-state current, DIBL, SS, $C_{gg,}$ and f_T. To mark the device guidelines for the fin width and fin height, variation of fin width is analyzed over a range of 5-10 nm keeping gate length as 12 nm and fin height as 18 nm. The fin height range is analyzed from 12-24 nm, keeping the width at 5 nm and length at 12 nm. The response of the width variation to the drain current and the transconductance is shown in Fig. 14. This rise in drain current is owing to an increase in the effective

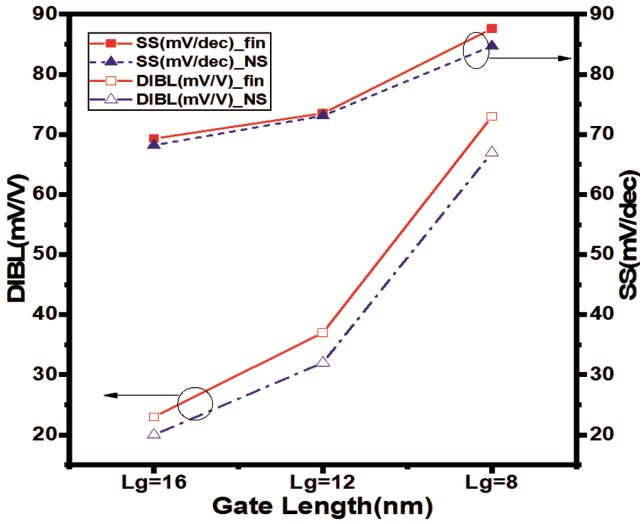

Fig. 13 — SS and DIBL with variation of gate length of finFET and nanosheet FET

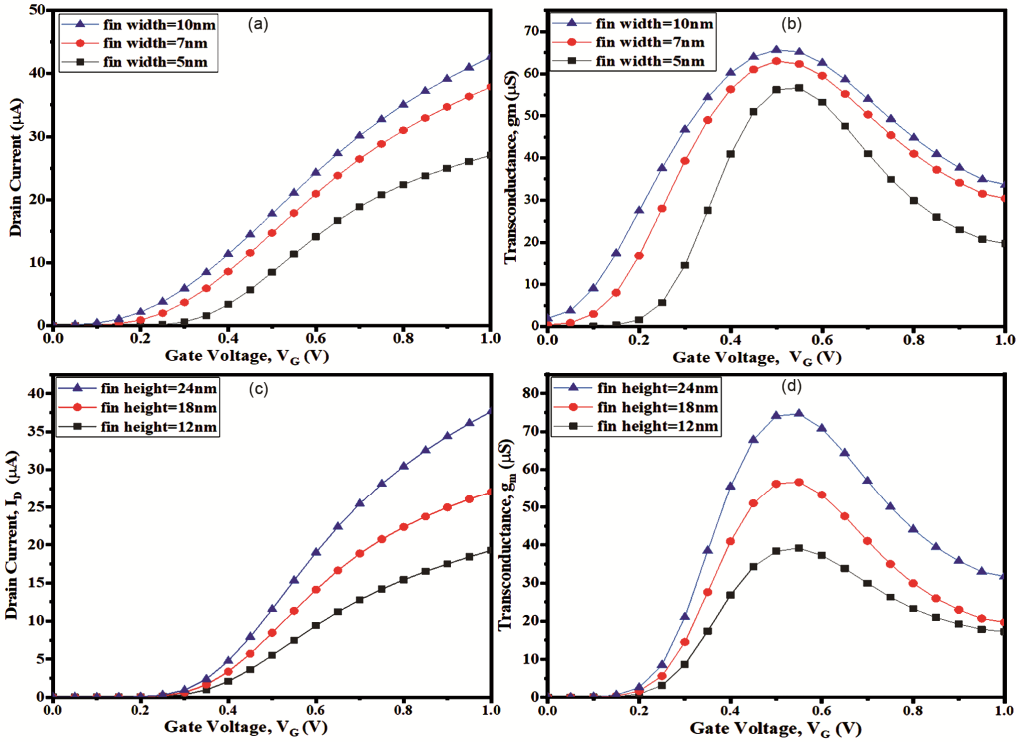

Fig. 14 — (a), (c) Drain Current (I_D) and (b), (d) Transconductance (g_m) versus gate voltage (V_G) curve with variation in fin width and fin height of the FinFET

gate width that leads to a rise in transconductance (g_m)[22,23]. The increase in the value of drain current is maximum at a width of 10 nm among the values analyzed. This increase is due to the direct dependency of it on the width of the fin. This can be understood by the relation of drain current (I_D) for the junctionless transistor given by Eq. (6)[1].

$$I_D \cong q\mu N_D T_{NS} W_{NS} \frac{V_{DD}}{L} \quad \ldots (6)$$

Variation in any geometrical parameter of the structure plays an important part in determining the behavior of the device towards short-channel effects. The fin height variation impact on drain current is shown in Figs 14(c &d). It is analyzed that with the rise in the height of the fin, the ON-state current increases 94% at a height of 24 nm concerning its value at a height of 12 nm.

At a fixed width of 5 nm the OFF-state current rises with an increase in fin height. The ON to OFF ratio is also analyzed and is found that among the heights taken at a width of 5 nm, the ON to OFF ratio is maximum at a height of 12 nm. Also, the scaling down of the width leads to an increase in threshold voltage due to an increase in short-channel effects. The transconductance of the FinFET increases with an increase in fin width and Fin height This is due to an increase in effective gate width. As the fin height increases it increases the effective width of the device.

Figure 15(a) shows the variation of gate capacitance (C_{gg}) with respect to gate voltage (V_G) at variable fin widths of 5 nm, 7 nm, and 10 nm. The gate capacitance is maximum corresponding to the width of 10 nm. This is because of the increase in effective gate width. The peak f_T is observed at a gate voltage of 0.5V with V_{DS} at 1V for a device with a

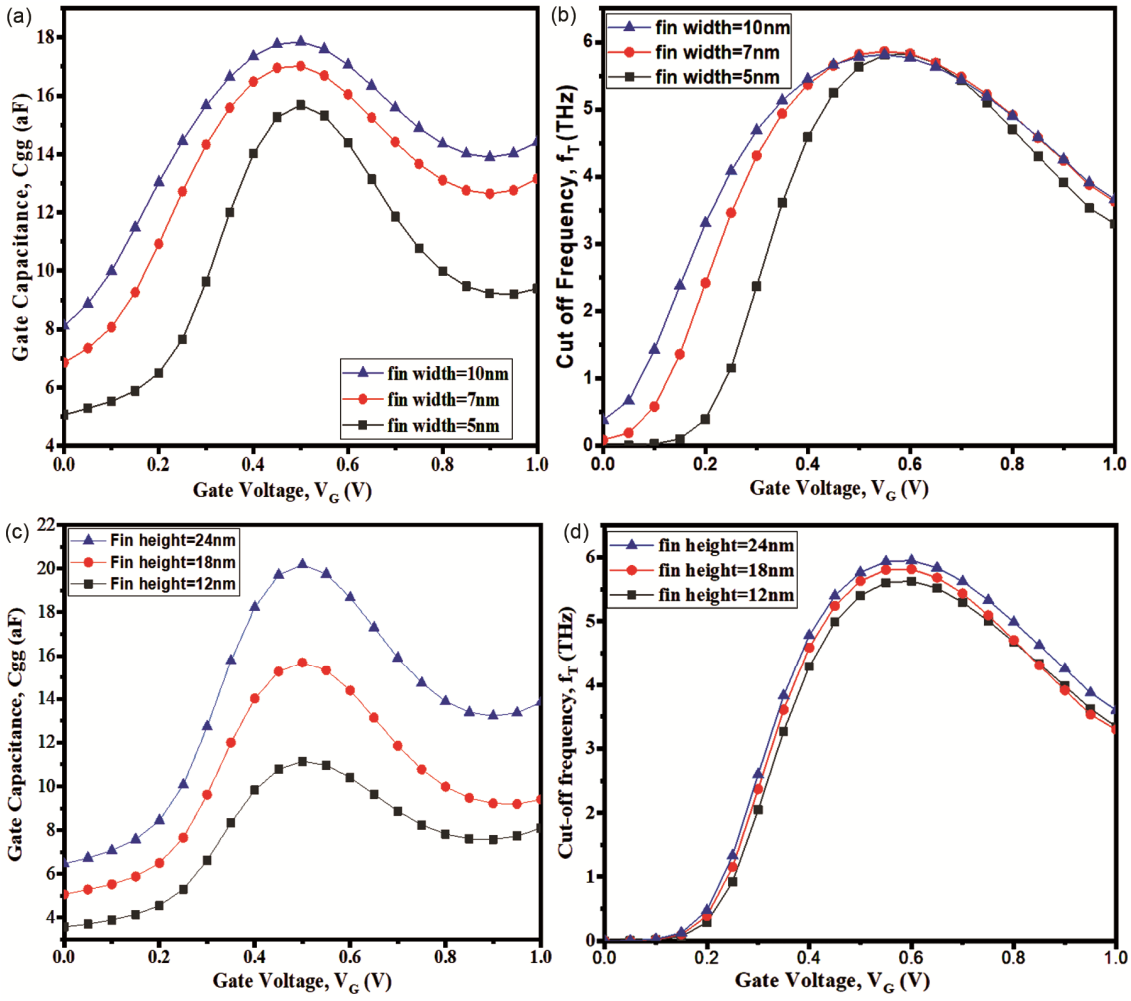

Fig. 15 — (a), (c) Gate capacitance (C_{gg}) vs gate voltage(V) (b), (d) cut-off frequency (f_T) vs gate voltage (V)characteristics of double fins FinFET with variation in fin width and fin height

width of 7 nm as shown in Fig. 15(b). For the variable fin widths of 5 nm, 7 nm, and 10 nm and variable fin heights of 12 nm, 18 nm, and 24 nm under analysis, the DIBL and SS are shown in Fig. 16. Though the line graph shows that the reduction in the fin width provides an edge to control the short channel effect by lowering DIBL and SS however with fin height little variation in SS and DIBL are observed. After the analysis, it may be concluded that with an increase in the fin width, the drain driving current increases, also there is an increase in OFF-state current, transconductance, and total gate capacitance. With the increase in fin height, threshold voltage decreases while ON-state current, transconductance, and total gate capacitance increases. Therefore, one optimized fin width and height should be chosen so that there is not much compromise in one performance metric at the cost of another.

As per the results observed, fin width of 7 nm and fin height of 18 nm are apt. As far as device design guidelines for nanosheet are concerned, the variation in the nanosheet width is observed from 24 nm to 12 nm at a fixed gate length of 12 nm and thickness of 5 nm.

Also, the nanosheet thickness variation from 9 nm to 5 nm with a fixed width of 18 nm and gate length of 12 nm are kept for observation. Various analyses have been carried out to get optimized dimensional parameters. The I_D versus V_G and g_m versus V_G characteristics with varying width and thickness of nanosheet are shown in Fig. 17.

With scaling down the width, the ON-state current decreases from 3.13×10^{-5} A to 1.56×10^{5} A (by 50%). But the OFF-state current improves from 1.42×10^{-13} A to 1.61×10^{-14} A (improves by 89%). The decrease in ON-state current is due to a decrease in mobility which in turn depends on W_{eff}. The overall mobility[8] of the structure depends on the top/bottom and sidewalls. In the case of an n-type device, the mobility decreases with decreasing nanosheet width. The decrease in the drain current with a decrease in the width of the nanosheet further degrades the transconductance of the structure. The scaling down of the thickness from 9 nm to 5 nm leads to a 75.31 % decrease in drain current at a drain voltage of 1V. This reduction in the drain current (I_{ON}) is due to the effect of reduced effective width, W_{eff}, which in turn depends on the width and the thickness parameter of nanosheet[9]. The decrease in the drain current with a decrease in the width of the nanosheet, further degrades the transconductance of the structure. The scaling down of the thickness from 9 nm to 5 nm leads to a 75.31 % decrease in drain current at a drain voltage of 1V. This reduction in the drain current (I_{ON}) is due to the effect of reduced effective width, W_{eff}, which in turn depends on the width and the thickness parameters of nanosheet[9]. The I_{OFF} current reduced to 99% with the decrease in nanosheet thickness (9 nm to 5 nm), which is due to the quantum confinement effect that becomes prominent with reduced dimensions. This effect leads to an increase in the gap between the conduction band and valence band and hence barrier potential increases. The improved I_{OFF} at a nanosheet thickness of 5 nm gives rise to the highest I_{ON}/I_{OFF}.

The variation of the C_{gg} and f_T curves versus V_G for varying nanosheet width and thickness are shown in Fig. 18. The curve in Figs. 17(b & d) reflects the decrease in transconductance with a decrease in nanosheet thickness because of the decrease in drain

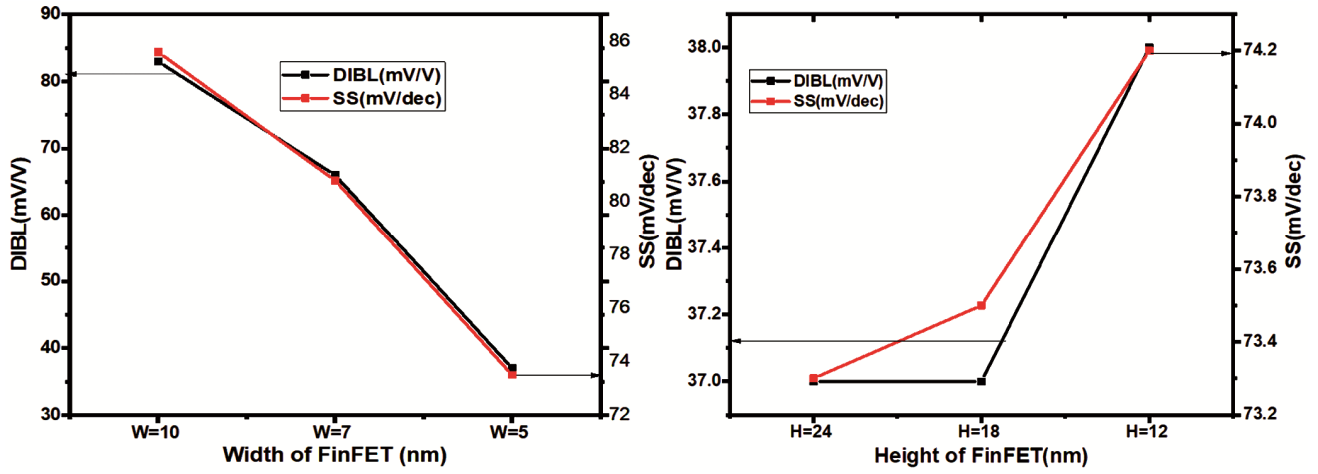

Fig. 16 — SS and DIBL with variation of (a) fin width and (b) fin height of FinFET

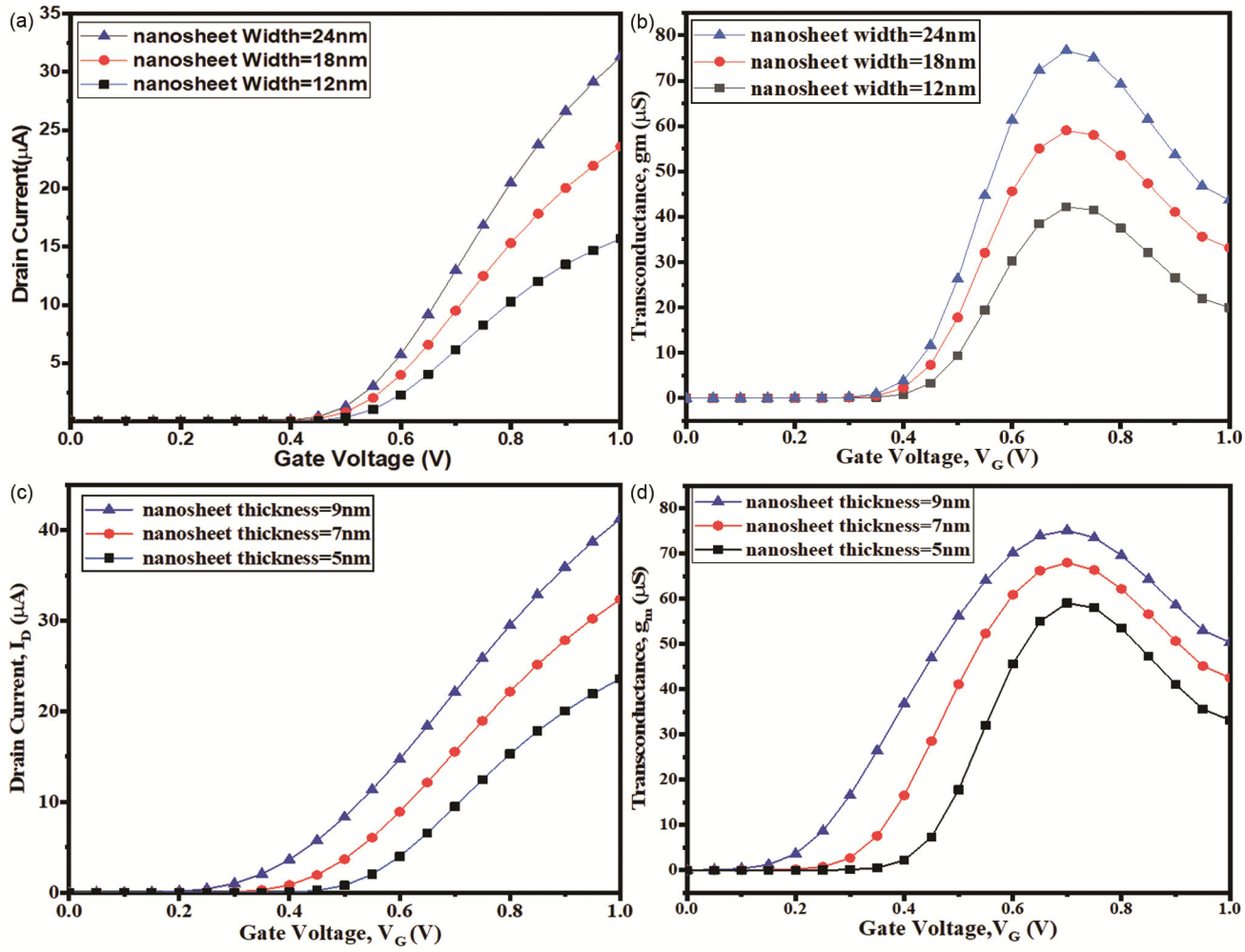

Fig. 17 — (a), (c) Drain Current (I_D) and (b), (d) Transconductance (gm) versus gate voltage (V_G) curve with variation in the width and thickness of the double-channel nanosheet FET

current value. The downscaling of the width and thickness of the nanosheet leads to a decrease in effective gate width and hence control over the channel decreases. As the nanosheet thickness is reduced from 9 nm to 5 nm, f_T also reduces, it is due to a reduction in g_m. The C_{gg} versus V_G curve is shown in Figs. 18(a & d) follow the downtrends with the downscaling of nanosheet width. The cut-off frequency has a direct dependence on transconductance and inverse on C_{gg} by the relation in Eq. (5). Therefore f_T is observed highest for a maximum width of 24 nm.

To analyze the behavior of the structure for RF applications, AC analysis is done. It is observed that the gate capacitance reduces (Fig. 18(c)) with a decrease in nanosheet thickness due to a reduction in W_{eff} and an increase in the quantum confinement effect[24-25]. The DIBL is found least with the reduced width of 12 nm. The SS also gives improved results with a width of 12 nm among the widths analyzed. The cut-off frequency at this width is less than the width of 24 and 18 nm. Therefore, a slightly higher width of 18 nm may be chosen to have the improved DIBL and SS at ample cut-off frequency. It is perceived that the threshold voltage of the structure with two-channel nanosheets increases[13,14] with a decrease in width because of the increase in the bandgap between the conduction and valence band. Also, the width of 18 nm provides an intermediate value of V_{th}.

The subthreshold swing and DIBL improved significantly at a reduced nanosheet thickness of 5 nm as shown in Fig. 19.Therefore, the thickness of the nanosheets contributes towards an important feature in deciding the optimum dimensions[26]. Among the analyzed thicknesses of 9 nm, 7 nm, and 5 nm, it is observed that with the reduced thickness of 5 nm, the

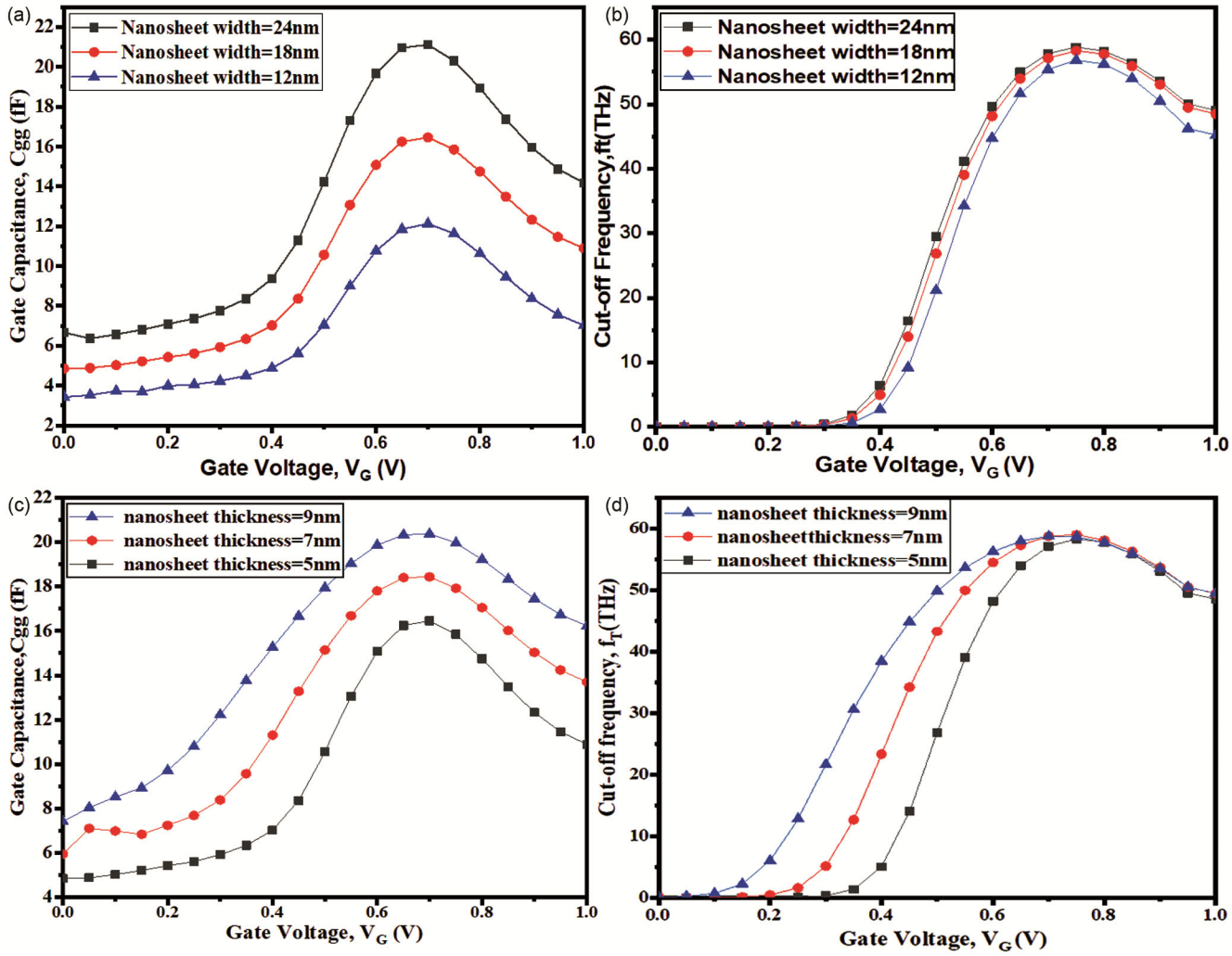

Fig. 18 — (a), (c) Gate Capacitance C_{gg} (b), (d) Cut-off Frequency, $f_T$vs gate voltage (V) with varying nanosheet width and thickness

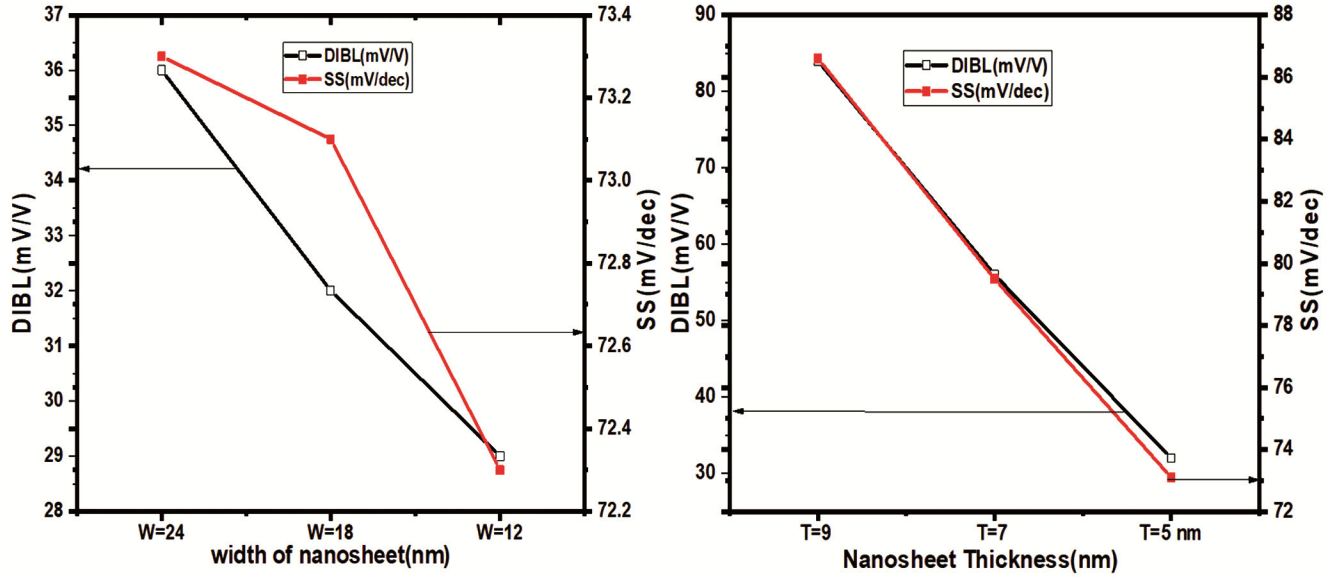

Fig. 19 — DIBL and SS with variation of nanosheet width and thickness

short channel effects are the least and I_{ON}/I_{OFF} is maximum[27,28,29,30]. Also, the nanosheet width of 18 nm is apt to get nearly the same f_T as is obtained at a higher width of 24 nm with improved OFF-state current and total gate capacitance.

4 Conclusion

This work analyzed the performance comparison between junctionless multi-fin FinFET and multi-channel nanosheet FET. It is observed that under the same gate length and comparable width/height and thickness, the nanosheets are the much better alternative structure for making the semiconductor devices in terms of improved I_{ON}, I_{OFF}, g_m, g_{ds}, SS, DIBL, and intrinsic gain (A_V). The addition of fins or channels each time to FinFET or nanosheet boosts the device in terms of current driving capabilities and hence, high transconductance is obtained. But each time with the addition of a fin or sheet, C_{gg} also rises to degrade the analog performance. Further, for the first time, the device design guidelines are elaborated concurrently, for the junctionless FinFET and nanosheet FET covering the impact of scaling the geometrical parameters on the electrical characteristics. With scaling down the gate length, the OFF-state current increases sharply.

In FinFET, working with a high width (10 nm in this case) of fin introduced much increased DIBL and SS but in the case of nanosheet high width provides a quite low value of DIBL and SS. It is observed that the height variation of the fin under the range considered in the paper makes the least impact on SCE of the device However the downscaling of thickness in the nanosheet gives the improved DIBL and SS. For FinFET, the optimized dimensions analyzed are as fin gate length =12 nm, fin width=7 nm, and fin height as 18 nm and of nanosheet is 12 nm as gate length, 18 nm as nanosheet width and thickness of 5 nm. This study is beneficial to get the optimized device performance of FinFET and nanosheet FET. However, a trade-off exists between scaling the dimensions and the performance/application required.

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References

1 Colinge J P, Lee C. W, Afzalian A, Akhavan N D, Yan R, Ferain I, Razavi P, Neill B O, Blake A, White M, Kelleher A M, McCarthy B & Murphy R, *Nature Nanotechnol*, 5 (2010) 225.
2 Sahay S & Mamidala J K, *Wiley-IEEE Press, NJ, USA*, ISBN: 978-1-119-52353-6, (2019) 496.
3 Colinge J P, Parihar M S, Ghosh D & Kranti A, *IEEE Trans Electron Dev*, 60 (2013) 1540.
4 Su C, Tsai T, Liou Y, Lin Z & Chao T, *IEEE Electron Dev Lett*, 32 (2011) 521.
5 Lee C W, Afzalian A, Akhavan N D, Yan R, Ferain I & Colinge J P, *Appl Phys Lett,* 94 (2009) 053511.
6 Dasgupta A, Parihar S S, Agarwal H, Kushwaha P, Chauhan Y S & Hu C*, IEEE Electron Dev Lett*, 41 (2020) 313.
7 Loubet *N, 2017 Symposium on VLSI Technology*, Kyoto, Japan, (2017) T230.
8 Tayal S, Ajayan J & Joseph L M I L, *Silicon,* 14 (2022) 3543.
9 Lee C W, Nazarov A N, Ferain I, Akhavan N D, Yan R, Razavi P & Colinge J P, *Appl Phys Lett,* 96 (2010) 102106.
10 Nagy D, Espiñeira G, Indalecio G, García-Loureiro A J, Kalna K & Seoane N, *IEEE Access*, 8 (2020) 53196.
11 Ajayan J, Nirmal D, Tayal S, Bhattacharya S, Arivazhagan L, Augustine Fletcher A S & Ajitha D, *Microelectron J,* 114 (2021) 105141.
12 Valasa, Tayal S & Thoutam L R, *Silicon,* 14 (2022)10347.
13 Yadav N, Jadav S & Saini G, *Silicon*, 14 (2022) 10681.
14 Sentaurus Device User Guide, Version-A2016, Synopsys Inc, 2020.
15 Salmani-Jelodar M, Ilatikhameneh H, Kim S, Ng K, Sarangapani P & Klimeck G, *IEEE Trans Nanotechnol*, 15 (2016) 904.
16 Yeap K H, Lee J Y, Yeo W L, Nisar H & Loh S H, *Mal J Fund Appl Sci*, 15 (2019) 609.
17 Sreenivasulu V B & Narendar V, *Silicon*, 14 (2022)3823.
18 Yoon J S & Baek R H, *IEEE Access,* 8 (2020)189395.
19 Mohapatra E, Dash T P & Jena J, *SN Appl Sci,* 3 (2021) 540.
20 Garg A & Yadav B S, *AEU - Int J Electron Commun,* 118 (2020) 153140.
21 Rassekh A & Fathipour M A, *J Comput Electron*, 19(2020)631.
22 Boukortt N E I, Lenka T R, Patane S & Crupi G, *Electronics,* 11 (2021).
23 Dargar S K & Srivastava V M, 2*019 Int Conf Automat, Comput Technol Manag (ICACTM)*, London, UK, (2019) 1.
24 Li O W & Wang C Y, *Silicon,* 15 (2023) 2765.
25 Kumari N A & Prithavi P, *Silicon* 14 (2022) 9821.
26 Gundu A K & Kursun V, *IEEE Trans Electron Dev*, 69 (2022) 922.
27 Ajayan J, Nirma Dl, Tayal S, Bhattacharya S, Arivazhagan L & Fletcher A, *Microelectron J,* 114 (2021) 105141.
28 Roy D & Biswas A,*Superlatt Microstruct,* 97 (2016) 140.
29 Kumari N A &Prithav P, *Microelectron J*, 125 (2022) 105432.
30 Jang D, *IEEE Trans Electron Dev*, 64 (2017) 2707.
31 Ghosh S, Koley K, Saha S K & K Sarkar C,*IEEE J Electron Dev Soc*, 3 (2015) 410.
32 Tayal S, Ajayan J, Joseph LL, Tarunkumar J, Nirmal D, Jena B & Nandi A, *Silicon*, 4 (2021)1.
33 Valasa S, Tayal S & Thoutam L R, *Silicon*, 14 (2022) 10347.
34 Singh B, Rai T, Gola D, Singh K & Goel E, *Sci Semicond Process*, 71 (2017) 161.
35 Garg A, Singh B & Singh Y, *AEU - Int J Electron Commun,* 118 (2020) 153140.