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Single VDCC Based Memcapacitor Emulator Circuit without Using Passive Elements and Analog Multiplier

Muhammet Oguz Korkmaz[a], Mehmet Sagbas[b], Yunus Babacan[c] & Abdullah Yesil[a*]

[a]Department of Electrical and Electronics Engineering, Bandirma Onyedi Eylul University, Balikesir 10200, Turkey.

[b]Department of Electrical and Electronics Engineering, Izmir Bakircay University, Izmir 35665, Turkey

[c]Department of Electrical and Electronics Engineering, Erzincan Binali Yıldırım University, Erzincan 24002, Turkey

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In this work, a grounded charge-controlled memcapacitor emulator circuit based on a Voltage Difference Current Conveyor (VDCC) is presented. The proposed circuit is constructed with only one VDCC element and four MOSFETs. It has a transistor-based structure without the use of any passive components. The absence of any passive components makes the circuit eliminating the need for complicated analog components. The suggested circuit does away with the necessity for a mutator, which eliminates the need for an additional separate memristor emulator. The analog multiplier circuit is also not used. Additionally, the designed memcapacitor circuit allows for independent electronic control of both the fixed and variable components, adding to its flexibility and adaptability. To demonstrate the accuracy of the suggested circuit, a SPICE simulation was run using a VDCC constructed with 0.18 μm TSMC CMOS transistors.

Keywords: Memcapacitor; Emulator; Tunable; VDCC

1 Introduction

Mem-elements, in addition to the well-known elements like resistors, capacitors, and inductors, are now regarded as fundamental components of electrical circuits. Researchers are paying a lot of attention to mem-elements. Since, mem-elements are frequently used to develop numerous intriguing applications in fields such as chaotic oscillators, sensors, cellular neural networks, cellular architecture modeling, logic gate implementation, Resistive Random-Access Memory (RRAM), and many others[1–4].

Since the introduction of HP's first memristor, numerous mathematical models of mem-elements have been released for real-world use and modeling[5–7]. Mem-elements, however, are unlikely to be widely used in the near future due to the expensive production costs and technological challenges associated with creating nanoscale electronics. An emulator is a component of a circuit that mimics the electrical behavior of a mem-element. Therefore, researchers have developed a plethora of mem-element emulators as alternatives, which have been reported in the extant literature[8]. On the other hand, memcapacitors are bridging decoupling components that connect conventional passive components to contemporary memory devices. The term "memory capacitor," known as a memcapacitor, refers to a fascinating electronic component that combines the properties of a regular capacitor with the capacity to store and remember electrical charge changes over time[9]. The promise for advancements in several areas, including energy storage, programmable analog circuits, bio-inspired applications, neuromorphic computing, and analog signal processing, is provided by this special combination of features[4,8,9].

After the development of memristors, memcapacitors have gained scientific attention. Due to some manufacturing challenges with this new component, many researchers concentrated on developing memcapacitor emulators. Some of the memcapacitor circuits proposed in the literature are implemented using a mutator circuit and a memristor element[10–18]. One of the primary drawbacks of these emulators is that they must use memristors, which can be difficult to come by on the market, or that designing a memristor emulator requires a lot of active components. The review of mutator-based memcapacitor emulator circuits in the literature is given as follows:

In Ref.[10], the authors suggested a mutator-based emulator circuit that operates as a grounded

*Corresponding author: (E-mail: ayesil@bandirma.edu.tr)

memcapacitor and meminductor using an Operational Amplifier (Opamp), one memristor, one floating resistor, and one grounded capacitor. Pershin and Di Ventra in Ref.[11] proposed a floating memcapacitor using a mutator-based approach. It employs four Second-Generation Current Conveyors (CCIIs), one grounded inductor, one floating resistor, and one floating memristor emulator. Wang et al. proposed a grounded memcapacitor emulator using a mutator[12]. The presented circuit uses two CCIIs, one floating capacitor, one floating resistor, and one memristor emulator. In Ref.[14], a floating memcapacitor circuit was given using four commercially available active components namely, AD844. One memristor, two resistors, and one capacitor are also needed. The presented emulator has not electronically tunability property. A grounded memcapacitor was proposed by Romero et al. in Ref.[15]. The presented circuit employs one Opamp, one inverting Voltage Buffer (VB), one floating capacitor, and a resistor. To construct this memcapacitor, a memristor emulator is also required. In Ref.[16], Singh and Rai presented floating memcapacitor and meminductor emulators. The proposed structures employ one VDCC, one grounded capacitor, and one memristor. Since the proposed structure is a mutator-based structure, an additional memristor emulator must be used. For this reason, an extra VDCC, a capacitor, and a resistor are needed to realize a memcapacitor. In Ref.[17], Taskiran et al. suggested a memcapacitor circuit using one Current Backward Transconductance Amplifier (CBTA), one memristor, and one capacitor. Since the authors used a CBTA-based mutator circuit, the extra memristor emulator circuit is required. Zheng et al. proposed an interface circuit for realizing emulators of mem-elements[18]. Four AD844s, one Opamp, four resistors, three capacitors, and one Varactor Diode (VrD) are needed to construct a memcapacitor emulator.

Apart from the above-mentioned mutator-based memcapacitor circuits, memcapacitor emulators have also been realized using extra Analog Multiplier (AM) circuit[19–24]. The following is a review of memcapacitor emulator circuits based on using AM circuit found in the literature:

Using the mathematical model of charge-controlled memcapacitance presented by Biolek et al. in[6], Fouda and Radwan proposed a grounded memcapacitor circuit[19]. The presented emulator uses two Opamps, two VBs, one AM, three capacitors and two resistors. To obtain the input charge and perform its integration, the proposed circuit also requires the implementation of a copy of the injected current. In Ref.[20], Sah et al. proposed a memcapacitor circuit without the drawback of needing a copy of the input current in Ref.[19]. The presented emulator circuit employs two Opamps, one AM, one floating resistor, one floating capacitor, and one grounded capacitor. Yesil and Babacan proposed two grounded memcapacitor circuits in 2021[21]. The first one employs one CCII, one operational transconductance amplifier (OTA), three capacitors, and one AM. The second one uses two CCIIs, three capacitors, and one AM. In Ref.[22], a memcapacitor is emulated employing five CCIIs, one VB, one AM, one resistor, and two capacitors. The paper[23] describes memcapacitor and meminductor emulators consisting of one Multi-Output OTA (MO-OTA), one MOSFET, two resistors, and one capacitor based on the usage of analog multiplier. Konal and Kacar presented a memcapacitor circuit using two MO-OTAs, two grounded capacitors, and two resistors[24]. The suggested circuit additionally includes an AM to get memcapacitor nonlinear behavior.

The following text details other memcapacitor emulator circuits in addition to the above-mentioned mutator- and analog multiplier-based implementations in the literature. Konal et al. developed a VDCC-based grounded memcapacitor emulator circuit[25]. Two capacitors and two resistors are also used as passive components. In Ref.[26], Raj et al. proposed mem-elements. In order to realize the memcapacitor circuit, two CCIIs, one OTA, two capacitors, and two resistors are used. In Ref.[27], a grounded memcapacitor emulator is presented employing a single Voltage Difference Transconductance Amplifier (VDTA) and two grounded capacitors. Although the proposed circuit uses few active and passive components, it does not have the orthogonal controllability of the fixed and variable parts. Ananda et al.[28] presented a charge-controlled memcapacitor emulator using one VDTA, one OTA, one VB, two capacitors, and one resistor. While the active elements in the circuit could be constructed using thirty-one transistors, passive elements were used to provide the memcapacitor structure.

The grounded memcapacitor circuit proposed in Ref.[29] consists of two current controlled Second-Generation Current Conveyors (CCCIIs), one CCII, and two VBs and does not contain any passive

elements. In this design, the intrinsic x-terminal resistance of the CCCII elements is employed as a resistor. Similarly, instead of conventional capacitors, the inherent capacitors present at the input port of the voltage buffers are utilized. Although this structure does not include passive elements, it contains many active components. The passive components in the memcapacitor emulators can also be implemented using MOSFETs. The following works employs MOSFETs instead of the resistor or capacitor. In Ref.[30], two OTAs, one unity gain amplifier (UGA), one resistor and two MOS capacitors were used to implement the memcapacitor emulator. In Ref.[31], one VDCC, four MOSFETs and two capacitors were used to implement the floating memcapacitor. M_P and M_N MOSFETs work as voltage-to-current (V-I) while MR_1 and MR_2 MOSFETs were used to obtain electronic resistance. Korkmaz *et al*.[32] proposed floating memcapacitor emulator consisting of an analog multiplier and only four transistors such as two of these transistors act as MOS capacitors whilst two of them are utilized to provide trans conductance gain. However, analog multiplication circuit give rises to extra power consumption and chip area.

In the literature review of memcapacitor emulators, it has been seen that most of the circuits described so far are very complex. Several emulator circuits in the literature have employed analog multipliers or memristor components (see Table 1). This paper presents a very simple circuit of grounded memcapacitor emulator which uses only one active block, namely voltage differencing current conveyor and four MOSFETs. The SPICE simulation has been utilized to check the workability of the proposed emulator. The following are the key features of the proposed memcapacitor emulator. (i) Because the suggested circuit does not use a mutator, there is no need for an additional memristor emulator circuit, (ii) It contains only one active element, (iii) The circuit has no passive components, (iv) No analog multiplier circuit is used, (v) The value of the memcapacitor can be controlled electronically, (vi) Both the fixed and variable parts can be electronically altered independently of one another.

Table 1 — Aspect ratio of transistors.

Transistors	W/L
M_1, M_4-M_8	7.2µm / 1.8µm
M_2, M_3	3.6µm / 1.8µm
M_9, M_{10}	9.0µm / 0.72µm
M_{11}, M_{12}	14.4µm / 0.72µm
M_{13}, M_{14}	3.6µm / 1.8µm
M_{15}, M_{16}	3.06µm / 0.72µm
M_{17}-M_{22}	2.4µm / 1.8µm
M_{23}, M_{24}	0.72µm / 0.72µm

2 Proposed VDCC-Based Grounded Memcapacitor Emulator

As described in Equation (1), a memcapacitor element can be identified from the non-linear correlation between sigma (σ) and flux (φ). Eqs (2) and (3) define the sigma and flux symbols in Eq. 1, respectively[33].

$$C_M(\varphi) = \frac{d\sigma}{d\varphi} \quad \ldots (1)$$

$$\sigma = \int_{t_0}^{t} q(\tau) d\tau \quad \ldots (2)$$

$$\varphi = \int_{t_0}^{t} V(\tau) d\tau \quad \ldots (3)$$

According to Eq. 4, given that φ is a function of σ, it is possible to construct a time-dependent memcapacitor function[20].

$$\frac{d\sigma}{dt} = \underbrace{\frac{d\sigma}{d\varphi}}_{C_M} \frac{d\varphi}{dt} \quad \ldots (4)$$

An Eq. 4 can be defined as voltage-controlled or charge-controlled according to an Eq. 5 or Eq. 6, respectively[9].

$$q(t) = C_M \left[\int_{t_0}^{t} V_C(\tau) d\tau \right] V_C(t) \quad \ldots (5)$$

$$q(t) = C_M \left[\int_{t_0}^{t} V_C(\tau) d\tau \right] V_C(t) \quad \ldots (6)$$

The Eq. 5 describes an ideal memcapacitor, but this equation is devoid of any parasitic effects and does not have an internal state vector. In the given Eq. 7, "β" and "α" are used to denote the initial value of memcapacitance and the change in capacitance corresponding to the movement of charge through it, respectively. In this study, we focus on a grounded structure memcapacitor emulator circuit, which uses the memcapacitance expression from Eq. 7[19, 34].

$$q(t) = \left[\beta \pm \alpha \sigma(t) \right] V_C(t) \quad \ldots (7)$$

In this work, a VDCC-based grounded charge-controlled memcapacitor emulator circuit is proposed. Fig. 1 illustrates the proposed emulator circuit, comprising a single VDCC and four MOSFETs. The circuit effectively achieves a transistor-based structure

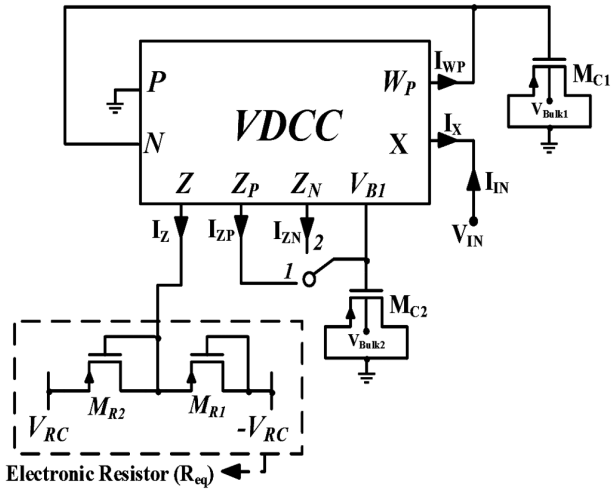

Fig. 1 — Proposed memcapacitor emulator circuit.

without using any passive components by having two of the MOSFETs (M_{R1} and M_{R2}) act as grounded electronic resistors and two of them (M_{C1} and M_{C2}) act as grounded capacitors. An equivalent resistor consisting of M_{R1} and M_{R2} can be described as $\mathrm{R}_{eq}=\frac{1}{2\mu_p C_{OX}\left(V_{RC}-V_{TH}\right)\left(W/L\right)_{M_{R1},M_{R2}}}$ [35]. As can be seen from the equivalent resistor equation, the value of the resistor can be adjusted electronically using the V_{RC} voltage. The total capacitance of transistors M_{C1} and M_{C2} seen at the gate terminals are defined as C_1 and C_2, respectively. The total capacitance of transistors M_{C1} and M_{C2} seen at the gate terminals is also inversely proportional to $\mathrm{V_{Bulk}}$ [36,37]. Since all the transistors used in the circuit instead of passive elements are in PMOS, a separate N-well structure for each of them can be easily provided in VLSI. In this way, MOS capacitors can be used separately and independently of each other. Consequently, the capacitance values can be electronically modified by altering the bulk voltages applied to the MOS capacitors. The mathematical models of the proposed circuit have been developed based on the characteristic structure of the VDCC element. Its characteristic equation sets are defined as $I_Z=I_{ZP}=-I_{ZN}=g_m(V_P-V_N)$, $V_X=V_Z$, $I_{WP}=I_X$ [38]. First of all, the mathematical equations of the decremental structure of the circuit according to the first position of the switch are given.

Then, the incremental structure is obtained when the switch is in the second position. Also, the Eq. 8 defines the current flowing through the W_P terminal, which is equal to the inverse of the input current:

$$I_{WP}=I_X=-I_{IN} \quad \ldots (8)$$

The circuit's input signal is connected via the X terminal. Fig. 1 indicates a negative correlation between the direction of current in the input signal and the current flowing through the X terminal. The Equation (8) states that the input current flowing from the X terminal is also flowing from the W_P terminal. Since no current flows from the N terminal, all of the input current flows through the capacitor C_1, forming the charge expression as shown in Eq. 9.

$$V_{WP}=V_N=\frac{1}{C_1}\int -I_{IN}dt=-\frac{q}{C_1} \quad \ldots (9)$$

In Fig. 1, it can be observed that the voltage at the Z terminal (V_Z) is determined by the multiplication of the resistance R and the current I_Z. The voltage V_N defined in Eq. 9 is used by substituting it in the characteristic equation of VDCC Since the P terminal voltage is grounded, the resulting V_Z voltage can be derived from Eq. 10.

$$V_Z=\mathrm{R}_{eq}I_Z=\mathrm{R}_{eq}g_m(V_p-V_N)=\mathrm{R}_{eq}g_m\frac{q}{C_1}$$
$$\Rightarrow V_Z=\frac{\mathrm{R}_{eq}g_m q}{C_1} \quad \ldots (10)$$

Since the input signal is applied to the X terminal, it can be written as $V_X=V_{IN}$ and $V_{IN}=V_Z$ since $V_X=V_Z$ thanks to the characteristic definition of VDCC. Since V_Z voltage in Eq. 11 is equal to V_{IN} voltage, V_{IN} voltage can be written as Equation.

$$V_{IN}=\frac{\mathrm{R}_{eq}g_m q}{C_1} \quad \ldots (11)$$

The transconductance gain (g_m) of the VDCC is expressed as in Eq. 12[39]. Here, the source voltage of the M_1 transistor in the internal structure of the VDCC element given in Fig. 2 is kept separate so that the g_m value can be adjusted electronically. In this way, the $\mathrm{g_m}$ value can be adjusted using the voltage V_{S1} as shown in Eq. 12.

$$g_m=K(V_{B1}-V_{S1}-V_{TH}) \quad \ldots (12)$$

Here, K is defined as $\mu_n C_{OX}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_{B1}\left(\frac{W}{L}\right)_{13,14}}$. The voltage at terminal V_{B1} is equal to the voltage produced on capacitor C_2 by the current flowing through terminal Z. Since the integral of the charge is equal to sigma (σ), the voltage V_{B1} is expressed as in Eq. 13.

$$V_{B1}=\frac{1}{C_2}\int I_Z dt \Rightarrow V_{B1}=\frac{1}{C_2}\int\left(\frac{g_m q}{C_1}\right)dt \Rightarrow V_{B1}=\frac{g_m\sigma}{C_1C_2} \quad \ldots (13)$$

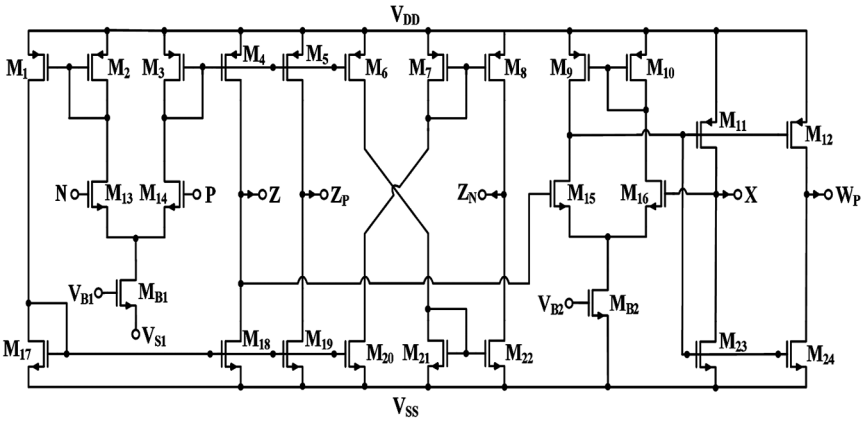

Fig. 2 — Internal structure of VDCC.

The value of g_m can be obtained as in Eq. 14, which is obtained by rearranging Eq. 12 and 13 together.

$$g_m = \frac{K(-V_{S1}-V_{TH})C_1C_2}{C_1C_2 - K\sigma} \quad \ldots (14)$$

Upon substitution of the expression g_m in Eq. 14 into Eq. 11, the resultant expression in Eq. 15 is derived.

$$V_{IN} = \frac{K(-V_{S1}-V_{TH})C_1C_2}{C_1C_2 - K\sigma}\frac{\mathrm{R}_{eq}\,q}{C_1}$$
$$\Rightarrow C_M = \frac{q}{V_{IN}} = \frac{C_1C_2 - K\sigma}{(-V_{S1}-V_{TH})K\,\mathrm{R}_{eq}\,C_2} \quad \ldots (15)$$

Eq. 15 can be simplified to derive the mathematical representation of the charge-controlled memcapacitor emulator circuit as shown in Eq. 16. This equation is derived by considering that the switch in Fig. 1 is in the first position and represents the decremental structure of the circuit.

$$\Rightarrow C_M^{-1} = \frac{V_{IN}}{q} = \frac{1}{\underbrace{\frac{C_1}{(-V_{S1}-V_{TH})K\,\mathrm{R}_{eq}}}_{\textit{Fix part}} - \underbrace{\frac{\sigma}{(-V_{S1}-V_{TH})\mathrm{R}_{eq}\,C_2}}_{\textit{Varaible part}}} \quad \ldots (16)$$

It is also possible to configure the proposed circuit as an incremental structure. When the switch is in the second position, the voltage V_{B1} has an incremental structure as shown in Eq. 18, since it is obtained using the current flowing through Z_N.

$$\Rightarrow C_M^{-1} = \frac{V_{IN}}{q} = \frac{1}{\underbrace{\frac{C_1}{(-V_{S1}-V_{TH})K\,\mathrm{R}_{eq}}}_{\textit{Fix part}} + \underbrace{\frac{\sigma}{(-V_{S1}-V_{TH})\mathrm{R}_{eq}\,C_2}}_{\textit{Varaible part}}} \quad \ldots (17)$$

It is important to note that since the value of the DC power supply (V_{S1}) is negative, the value of $(-V_{S1}-V_{TH})$ is positive. As seen from Eqs. 16 and 17, the fix part and variable part of the proposed memcapacitor can be both electronically and orthogonally controlled with C_1 and C_2 MOS capacitors with the help of V_{Bulk1} and V_{Bulk2}, respectively. While the fix part of memcapacitance can be adjusted electronically with V_{Bulk1}, the variable part can be adjusted electronically with V_{Bulk2}. Moreover, fix and variable parts of memcapacitance can be changed electronically at the same time using R_{eq} by means of the control voltage (V_{RC}). terminal.

3 Simulation Results

The simulations were constructed utilizing the LTspice software, with process parameters selected at TSMC 180 nm. As seen in Fig. 1, one VDCC and four MOSFETs are used to set up the simulation. The dimensions of the MOSFETs forming the electronic resistance structure were chosen as $W/L = 60\mu m/2\mu m$, and the dimensions of the MOSFETs forming the C_1 and C_2 capacitors were selected as $W/L = 350\mu m/5\mu m$. During the process of constructing the C_1 and C_2 capacitances, the capacitance values have been enhanced by employing a configuration of five transistors in parallel to avoid excessive size of the transistors. The capacitance values provided in the paper and all the outcomes obtained from simulations are derived from five MOS capacitors connected in parallel. The internal structure of the VDCC element is depicted in Fig. 2[38,39] and the aspect ratio of transistors used in the internal structure of the VDCC element is given in Table 1. In addition, the bulk terminals of PMOS transistors are connected to the source terminal, while the bulk terminals of NMOS transistors are connected to the lowest voltage, -0.9V.

The circuit's operational properties were evaluated through simulation studies using frequency, temperature, and Monte Carlo analysis. The circuit's

electronic tunability was demonstrated by independently modifying the MOS capacitors M_{C1}, M_{C2}, and the electronic resistor R_{eq}, and observing the resulting impact on the system. In addition, the circuit's memory effect was investigated by applying square waves in incremental and decremental structures to observe variations in the circuit's charge level.

Unless stated otherwise, the values described here were used in all simulations. The circuit operates with ±900 mV DC power supply voltages while V_{B2} and V_{S1} are selected as 0V and -660mV. During the simulations, the input signal utilized is a sine wave with a frequency of 70 kHz and an amplitude of 40 mV. The bulk voltages of the MOS capacitors in the circuit are chosen as 900 mV to ensure maximum linearity. At this voltage, the capacitors exhibit a capacitance of about 17 pF. By choosing the control voltage of the electronic resistor (V_{RC}) in the circuit as 340 mV, a resistance value of approximately 74 kΩ was obtained. A graphical representation of changes in input voltage and charge over a period of time is shown in Fig. 3. While Fig. 3(a) was obtained, a decremental structure was obtained by placing the switch in the first position. In Fig. 3(b), the switch was moved to the second position, the circuit was turned into an incremental structure and the charge voltage graph was obtained. In addition, in other simulation studies, a decremental structure with the switch position in the first position was used.

While performing the frequency analysis of the circuit, the input signal voltage was kept constant at 40mV and the frequency was changed to 60 kHz, 70 kHz, and 110 kHz. As expected, the increase in input signal frequency resulted in the linearization of the hysteresis curves as seen in Fig. 4(a). To investigate the impact of the input signal's amplitude on the hysteresis loop of the circuit, the input frequency was maintained at 70 kHz while modifying the signal's amplitude to 40 mV, 30 mV, and 20 mV. As depicted in Fig. 4(b), a reduction in the amplitude of the input signal corresponded to a decrease in the amplitude of the hysteresis loops.

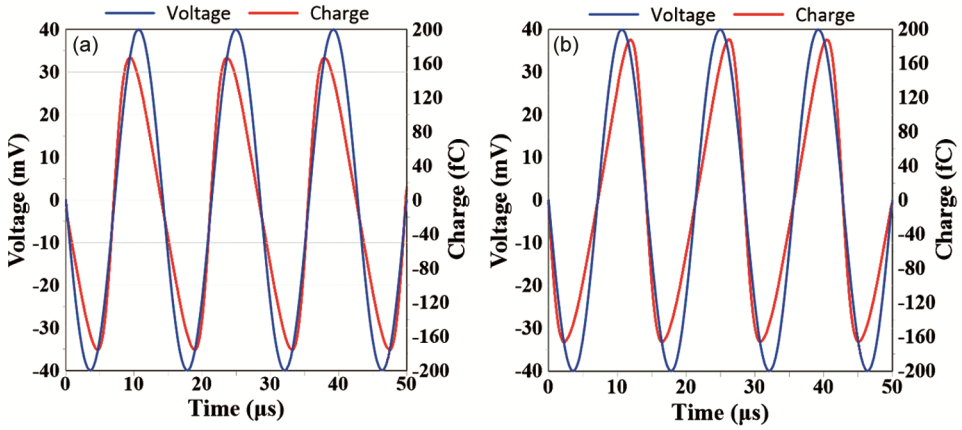

Fig. 3 — Time-dependent input voltage-charge graphs for (a) decremental and (b) incremental structures.

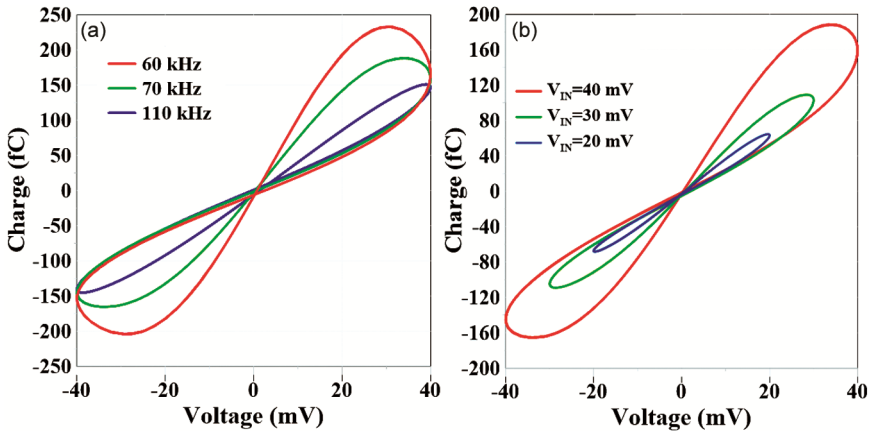

Fig. 4 — Hysteresis loops obtained from (a) frequency analysis and (b) amplitude change of the input signal of the circuit.

As seen in Fig. 1, capacitors C_1 and C_2 are constructed using MOSFETs. The V_{GS} voltages of both MOS capacitors vary between -120 mV and 80 mV. When the graph of MOS capacitors given in Fig. 5(a) is examined, it is seen that the capacitance values are almost linear in this voltage range. As a result, the capacitance values obtained by changing the bulk voltages to 0 V, 450 mV, and 900 mV by keeping the V_{GS} voltage in the range of -120 mV to 80 mV are presented in Fig. 5(a). For average V_{GS} voltage, the change in the total capacitance observed at the gate terminal of transistors M_{C1} and M_{C2} is presented in Fig. 5(b). It can be easily seen from Fig. 5(b) that total capacitance of transistors M_{C1} and M_{C2} seen at the gate terminals can be tuned by changing bulk terminal voltage (V_{bulk}). When the bulk voltage of the MOS capacitors is set at 900 mV, the average capacitance is measured at 17.2 pF. Similarly, at 450 mV, the capacitance increases to 19.31 pF, and at 0 V, it further rises to 22.69 pF.

In the mathematical expression of the proposed circuit according to Equations (16) and (17), it is seen that the MOS capacitor C_1 is in the numerator of the fixed part, and the MOS capacitor C_2 is in the denominator of the variable part. If the bulk voltage of the MOS capacitor C_2 is kept constant at 900 mV and the bulk voltage of the MOS capacitor C_1 is increased, it will lead to a decrease in the capacitance value of C_1 and the fixed part of the circuit. This reduction causes the slope of the hysteresis curve to decrease as shown in Fig. 5(c). If the bulk voltage of the MOS capacitor C_1 is kept constant at 900 mV and the bulk voltage of the MOS capacitor C_2 decreases, the variable part also decreases. This leads to the linearization of the hysteresis loops, as depicted in Fig. 5(d). In order to adjust the resistance value of the electronic resistor, the V_{RC} voltages seen in Fig. 1 were adjusted as 330 mV, 340 mV and 350 mV, and resistance values of 92.25 kΩ, 73.54 kΩ, and 58.73 kΩ were obtained, respectively. When Eqs. 16 and 17 are examined, it is seen that the resistance is in the denominator part of both the fixed part and the variable part.

Therefore, decreasing the V_{RC} voltage will cause an increase in the resistance value and this decrease will cause a decrease in both the fixed part and the variable part. As shown in Fig. 6(a), it is seen that the increase in resistance value decreases both the slope and amplitude of the hysteresis curve. As mentioned in Eq. 12, the g_m value can be adjusted with the V_{SI} voltage. The effect of V_{SI} voltage on the hysteresis of the circuit is shown in Fig. 6(b). The temperature analysis of the proposed circuit was made at -25, 27 and 80 °C

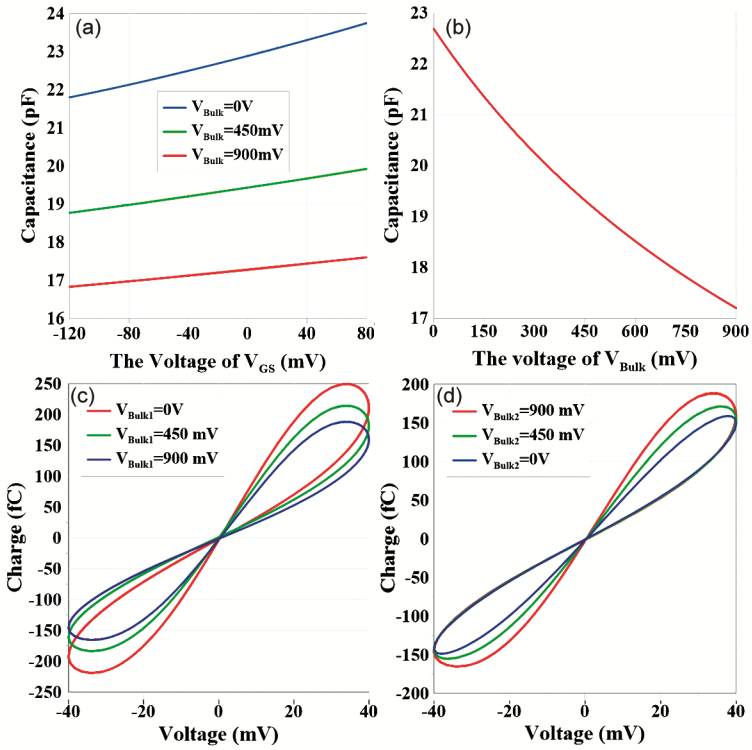

Fig. 5 — (a) The effect of the change in V_{GS} voltage on the capacitance (b) The effect of the change in V_{bulk} voltage on the capacitance and the effects of the change of capacitors (c) C_1 and (d) C_2 on the hysteresis curves.

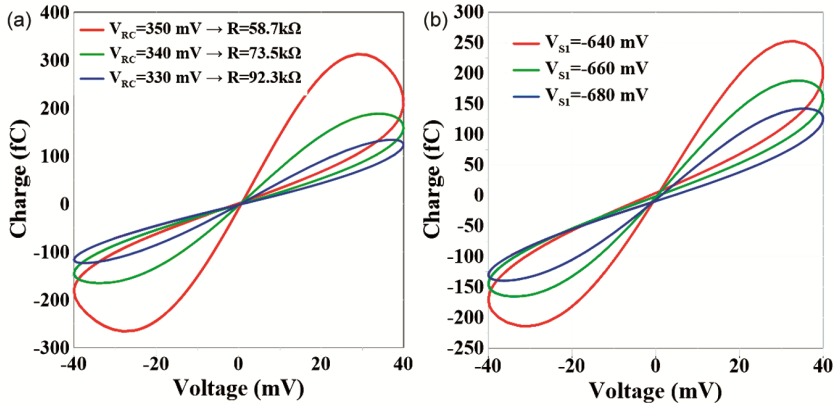

Fig. 6 — Effects of (a) resistance change and (b) V_{SI} voltage change of VDCC element on hysteresis.

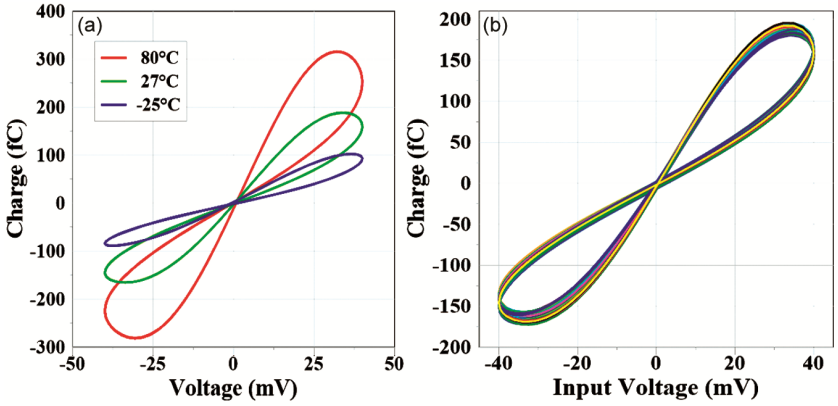

Fig. 7 — Hysteresis loops from (a) temperature analysis and (b) Monte Carlo analysis.

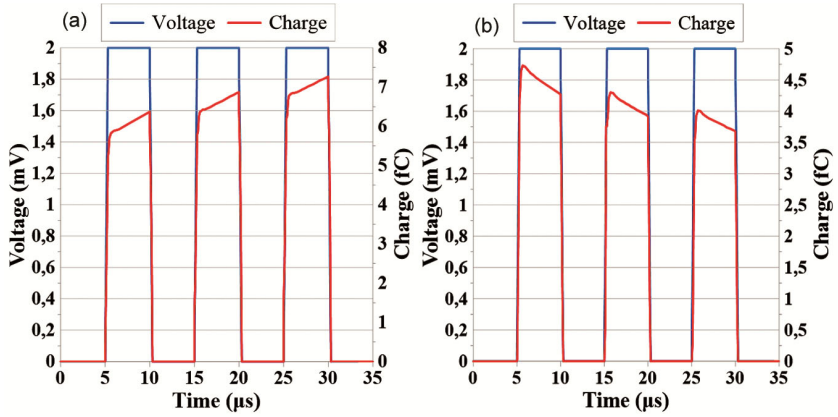

Fig. 8 — Memory effects of (a) incremental and (b) decremental states of the memcapacitor emulator.

temperatures. Since the circuit is designed using MOSFETs instead of passive elements, the performance of the circuit is temperature-dependent. As shown in Fig. 7(a), while temperature change causes a significant change in the hysteresis curves, the characteristics of the memcapacitor remain unchanged.

Monte Carlo analysis was performed in 100 iterations with 5% tolerance for W and L dimensions of MOSFETs used in electronic resistors and MOS capacitors. Additionally, the analysis included the simultaneous assessment of supply voltages, also subject to a tolerance of 5%. The hysteresis from 100 iterations is shown in Fig. 7(b). When the hysteresis is examined, it is seen that a 5% change in the W and L values of the MOSFETs and supply voltages does not change the general characteristic structure of the circuit much.

While analyzing the memory effect of the circuit, as seen in Fig. 8, three 2 mV signals were given to the

circuit at 5 μs intervals. Each signal was applied for 5 μs. When the results obtained in both increasing and decreasing structures are examined, it is seen that the capacitance value of the circuit increases and decreases as expected and the circuit maintains its capacitance value when no signal is applied to the circuit. Note that, while the memory graphics are being displayed, the two ripples formed at the rising edge of the charge curve have been corrected with the filter circuit, allowing the result to be seen more clearly.

4 Discussion

The suggested memcapacitor emulator circuit was compared to existing memcapacitor emulators published in the literature. The comparison is based on the number of active and passive components, electronic tunability property, types of realizations (mutator-based or use of analog multiplier), floating/grounded emulator setups, orthogonal controllability of the fix and variable part, experimental results, and frequency range. Based on, the following findings have been reached. Table 2 depicts a

Table 2 — Comparison of the memcapacitors in the literature and the proposed emulator in this paper.

Ref.	Number of Active Elements	Number of Passive Elements	Analog Multip.	Mutator	Floating/ Grounded Structure	Whether the fix part is set electronically	Whether the variable part is set electronically	Electronically tunable	Simulation/ Experimental	Maximum Operating Frequencies
10	1 Opamp	1 C, 1 R,1 MR	No	Yes	G	NA	NA	NA	Sim.	8 Hz
11	4 CCIIs	1 L, 1 R,1 MR	No	Yes	F	NA	NA	NA	No	-
12	2 CCIIs	1 C, 1 R,1 MR	No	Yes	G	No	No	No	both	280 Hz
13	2 CFOAs	1 C, 1 R, 1 MR,	No	Yes	F	No	No	No	Sim.	900 Hz
14	4 AD844s	1 C, 2 R,1 MR	No	Yes	F	No	No	No	Both	86.6 Hz
15	1 Opamp, 1 VB	1 C, 1 R, 1 MR	No	Yes	G	No	No	No	Yes	50 Hz
16	1 VDCC	1 C, 1 MR	No	Yes	F	No	No	Yes	Sim.	700 kHz
17	1 CBTA	1 C, 1 MR	No	Yes	F	No	No	Yes	Sim.	250 kHz
18	4 AD844s	2 C, 2 R, 1 VrD	No	No	F	No	No	No	Both	180 kHz
19	2 Opamps, 2 VB, 1 AM	3 C, 2 R	Yes	No	G	No	No	No	Sim.	100 Hz
20	2 Opamp, 1AM	2C, 1R, 1 D	Yes	No	F	No	No	No	Sim.	25Hz
21[a]	2 CCII, 1 AM	3 C, 1 R	Yes	No	G	No	No	No	Both	2 kHz
21[b]	1 CCII, 1 OTA, 1 AM	3 C	Yes	No	G	No	Yes	Yes	Sim.	2 kHz
22	3 CCIIs, 1 AM	3 R, 2 C	Yes	No	G	No	No	No	Both	5 kHz
23	1 MO-OTA, 1 MOSFET, 1 AM	1 C, 2 R	Yes	No	G	NA	NA	Yes	No	6 kHz
24	1 MO-OTA, 1OTA 1 AM	2 C, 2 R	Yes	No	G	NA	NA	Yes	Sim	10 Hz
25	2 VDCCs	2 C, 2 R	No	No	G	NA	NA	Yes	Both	10 kHz
26	2 CCII, 1 OTA	2 C, 2R	No	No	G	No	No	No	Both	800 kHz
27	1 VDTA	2 C	No	No	G	Yes	No	Yes	Both	50 MHz
28	1 VDTA, 1 OTA, 1 VB	2 C, 1 R	No	No	F	No	Yes	Yes	Yes	1.2 MHz
29	2 CCCIIs, 1 CCII, 2 VBs	-	No	No	G	Yes	Yes	Yes	Sim	80 MHz
30	2 OTA, 1 UGA, 2 MOSFET	1R	No	No	F	No	Yes	Yes	Both	24 MHz
31	1 VDCC, 4 MOSFETs	2 C	No	No	F	NA	Yes	Yes	Sim	1.2 MHz
32	1 AM, 4 MOSFETs	-	Yes	No	F	Yes	Yes	Yes	Both	100 MHz
Proposed	1 VDCC, 4 MOSFET	-	No	No	G	Yes	Yes	Yes	Sim.	110 kHz

AM: analog Multiplier, VrD: Varactor Diode, D: Diode, MR: Memristor, R: resistor, C: capacitor, L: inductor, VB: Voltage buffer, F: Floating, G: Grounded, Fig 1(b) [10], Fig 1(b)[11], Fig 3[14], Fig 2[15], Fig 4[16], Fig 3(b)[17], Fig 4[18], Fig 3[20], Fig 2[21a], Fig 3[21b], Fig 2(a)[22], Fig 4[23], Fig 1[27], Fig 4[28], Fig 1(a)[29],

comparison between the presented memcapacitor circuit and the other topologies documented in the literature. It can be easily observed from Table 2 that the proposed memcapacitance contains a small number of active elements, while no passive elements are used. Moreover, both the fix part and the variable part of the proposed structure are adjusted electronically, independently of each other.

5 Conclusions

This article discusses the implementation of the memcapacitor emulator circuit using four MOSFETs and a single VDCC, avoiding the use of passive elements. The proposed emulator circuit is grounded and mathematically defined as charge-controlled. The circuit can be operated both incrementally and decrementally, as demonstrated mathematically and in simulation studies. Since the proposed circuit has no mutator structure, a memcapacitor is obtained without the need for an additional memristor emulator. Moreover, no analog multiplier is used in the proposed circuit. Furthermore, the presented emulator allows independent electronic control of both fixed and variable components, which increases its versatility and adaptability.

The electronically adjustable structure of the circuit, the temperature stability, the Monte Carlo analysis, and the memory effect are illustrated by simulation studies with the LTspice. The comparison of the obtained results with the mathematical expression of the circuit shows that they are in good agreement.

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