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A Systematic Investigation of Dual Material Gate TFET for Improved Performance

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This study explores the influence of different metal gate combinations on the performance of dual-metal gate TFETs (DMG-TFET). The ON-state current in a TFET depends on band-to-band tunneling (BTBT) across the junction between the source and channel regions. Therefore, it is crucial to select a tunnel gate material with an appropriate work function to optimize the devices' overall performance. The present work explores the effect of dual metal gates having different work functions on tunnel barrier width of TFET. In this work, three distinct Double Gate TFET structures; Double Gate (DG) TFET, Dual Metal Gate (DMG) TFET, and Dual Metal Gate Hetero-Dielectric (DMG-HD) TFET are designed using TCAD device simulator. The proposed device (DMG-HD) TFET is benchmarked by considering various performance metrics such as ON-state current I_{ON}, OFF-state current I_{OFF}, ON-to-OFF current ratio I_{ON} /I_{OFF}, and sub-threshold slope (SS). This study also highlights the key finding of optimizing the length of dual metals and the work functions of metal gates (M-1) and (M-2)in TFETs. The results show that the proposed device (DMG-HD TFET) gives improved performance compared to the other two devices. The proposed TFET structure improves the ON-current by two orders (10^{-5} to 10^{-3} (A/μm)), *ION* /*IOFF* ratio by three orders (10^{9} to 10^{12} (A/μm)) and sub-threshold swing (SS) by 23.82% compared to the conventional TFET device.

Keyword: DG TFET; DMG HD TFET; Dual Metal Gate; HD TFET; Tunnel FET

1 Introduction

Now a days MOSFET is a kind of transistor abundantly used in electronic devices. Before MOSFETs were in- vented, bipolar junction transistors (BJTs) were commonly used in electronic devices. However, BJTs had limitations such as low input impedance, high power consumption, and limited frequency response. These limitations led to the developmentof MOSFETs, which had higher input impedance, lower power consumption, and faster switching speed.

While MOSFETs have revolutionized the field of electronics and are widely used in various applications, they also face several challenges. Some of the key challenges associated with MOSFET technology are: Power Dissipation, Scaling Limitations, Higher OFF current (which increases the Leakage current), Lower I_{ON} /I_{OFF} ratio and the sub-threshold swing is restricted to 60 mV/decade[1-4].

The basic architecture of the Tunnel Field Effect Transistor (TFET) involves a gated P-I-N diode that functions through gate-controlled band-to-band tunneling (BTBT). According to sources[5-6], the TFET has several advantages over the MOSFET, including a sub-threshold swing (S.S) that cannot be restricted to 60 mV/decade, increased tolerance to short channel effects, faster operation due to tunneling, significantly lower threshold potential (V_t) roll-off, reduced off current, and improved on/off current ratio. These features make TFET a hopeful substitute to MOSFET for low-power applications requiring faster speed. Thus, TFET could potentially replace MOSFET in such applications[7-11].

TFETs exhibit lower on current I_{ON} compared to MOS- FETs when the source, channel, and drain are composed of the identical material, because the band-to-band tunneling process becomes less efficient. As an outcome, the on current in TFETs is frequently less compared to MOSFETs. To enhance I_{ON}, hetero junction TFETs utilize different materials in distinct regions along with a single gate, ensuring that the sub-threshold slope (S.S) remains below 60 mV/decade[12-13].

Indeed, in addition to single-gate hetero junction TFETs, TFET structures with multiple gates have shown promising results. These multi-gate TFETs utilize multiple gate electrodes to control the flow of charge carriers and improve device performance. By applying different voltages to the individual gates,

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enhanced electrostatic control can be achieved, leading to better current[14-15].

The incorporation of high-k materials in TFETs is another technique employed to enhance their electrical properties. High-k dielectric materials have a higher permittivity com- pared to traditional low-k materials. This high permittivity al- lows for better gate dominance over the channel and decreases the gate leakage current. By using high-k materials as the gate dielectric, TFETs can achieve improved sub-threshold swing, reduced threshold voltage, and enhanced on/off current ratio[16-18].

Over the past few years, a novel design approach has emerged for work function engineered twin or triple material gates in DG TFETs. This innovative configuration focuses on altering the overall electric field in the channel, leading to enhancements in the devices ON current. The increased electrical properties of the surrounding gate are further examined utilizing the dual gate material, which has two separate work functions[19-22].

In previous research, there has been a lack of systematic exploration regarding the utilization of existing gate materials for M-1 and M-2 purposes and the subsequent optimization of metal gate lengths. However, this study aims to address this gap by conducting a comprehensive investigation into various gate metals' availability and optimizing their gate lengths systematically. Additionally, hetero-dielectrics will be employed to enhance the ON current of TFET as well.

2 Device Structure

Figure 1 displays the visual representations of the three de- vices analysed in this study. Fig. 1(a) depicts the traditional DG-TFET featuring SiO_2 as the gate oxide (referred to as structure-1). In the mentioned designs, the doping concentrations for the source (p^{++}), intrinsic channel, and drain (n) are 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, 5×10^{18} cm^{-3}, and the work function of the doped silicon channel is 4.94 eV respectively, with a channel length of 50 nm. To minimize ambipolarity, the doping concentration in the drain region is deliberately lower than that in the source region.

TFET's operate based on band-to-band tunneling, where carriers tunnel through a barrier formed between the source and channel region. Due to higher doping concentration in the source region, the electric field between the source and channel junction becomes stronger. This electric field assist in facilitating tunneling process by lowering the effective width of the tunneling barrier and enhancing the tunneling probability.

When the doping concentration in the drain region is low, it leads to a larger depletion region and weaker electric field between the channel and drain region. A weaker electric field means that electrons require more energy to tunnel through this extended region, thus increasing the tunneling distance. It helps to reduce the off-state leakage current and enhancing the transistor's ability to turn off effectively. This is crucial for maintaining a high on/off current ratio and improving energy efficiency in the off-state.

Figure 1(b) illustrates the Dual-Metal DG-TFET with a gate oxide thickness (T_{OX}) of 2 nm. This design incorporates a pair of metal gates, Tunnel gate (M-1) and Auxiliary gate (M-2), with distinct work functions positioned adjacent to each other (see Table 1). The

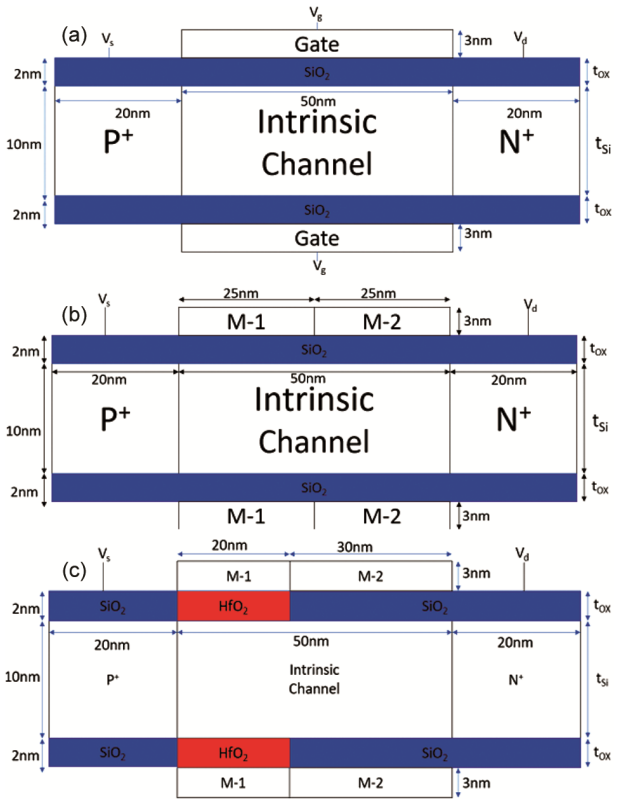

Fig. 1 — Schematic of (a) Double Gate TFET, (b) Dual Metal Gate TFET and (c) Dual Metal Gate Hetero Dielectric TFET.

Table 1 — Shows the different combinations of metals usedfor M-1 and M-2 as shown in [Fig 1(b)] and [Fig 1(c)].

S. NO	Tunnel gate (M-1)	Auxiliary gate (M-2)	ϕ_{M1} (eV)	ϕ_{M2} (eV)
1.	Aluminum	Platinum	4.20	5.60
2.	Tungsten	Platinum	4.55	5.60
3.	Titanium	Platinum	4.60	5.60
4.	Copper	Platinum	4.70	5.60

arrangement of these gates leads to improved characteristics such as higher I_{ON}, lower I_{OFF}, and a more favourable sub-threshold swing. The metal gates M-1 and M- 2, with lower and higher work function values, respectively, are situated in close proximity to both the source and drain regions. This Dual-Metal DG-TFET design utilizes dual-gate materials, with metal-1 having a work function (Φ_{M1}) of 4.20 eV, chosen for its high thermal conductivity, while metal-2 possesses a work function (Φ_{M2}) of 5.60 eV.

Figure 1(c) presents the proposed structure, referred to as a Dual Metal Gate Hetero Dielectric TFET. This design incorporates two different dielectric materials: low-k dielectric SiO_2 ($\varepsilon = 3.9\varepsilon_0$) near the drain end and high-k dielectric HfO_2 ($\varepsilon = 21\varepsilon_0$) towards the source end. The inclusion of a high-k dielectric near the tunnel junction enhances the tunneling probability of the device. Device Geometry and process parameters are shown in Table 2.

3 Simulation Methodologies

To simulate structures and analyse band-to-band tunneling (BTBT), the Sentauras TCAD tool is utilized[23]. The simulation method incorporates a non-local BTBT model, enabling the examination of variations in electric field distributions and tunneling generation rates along the tunneling length of the device. This non-local approach effectively considers the impact of occupancy levels and density of states. The model is especially well-suited for reverse bias tunneling junctions characterized by high doping concentrations.

The simulation takes into account Fermi-Dirac statistics, high- density carrier concentrations, and device recombination processes by incorporating Auger and SRH recombination models. The BGN model, a doping-dependent mobility model, and drift-diffusion carrier transport model are also employed. The specific parameters for band-to-band tunneling are determined based on reference[24], while the simulation setup is calibrated according to the information presented in Fig. 2[25]. In summary, the Sentauras TCAD tool, in conjunction with the implemented models and calibration procedures, facilitates a thorough analysis and simulation of structures. It particularly emphasizes the examination of band-to-band tunneling, electric field distributions, and tunneling generation rates, allowing for comprehensive insights into these aspects.

4 Results and Discussion

4.1 Selection of Gate Metals

In this study these are some different metal combinations applied for structure 2 and structure 3 and examines howthe work functions of these metals improves the device ON current and other parameters like sub-threshold swing, ON- OFF current ratio, Ambipolar current.

Work Function of Metal-1 (M-1): Lowering the work function of M-1 can decrease the tunneling barrier height, which can potentially enhance the tunneling probability and thus improve TFET performance in terms of current flow and switching characteristics.

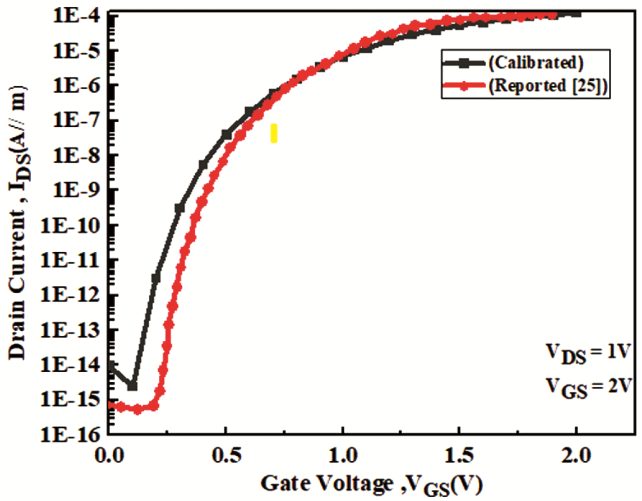

Fig. 2 — I_D vs V_{GS} Calibrated from the result's described in[25].

Table 2 — Device Geometry and process parameters

Parameters	Symbol	Structure-1	Structure-2	Structure-3 (The proposed structure)
Gate length	L_G	50 nm	50 nm	50 nm
SiO_2 thickness	TOX	2 nm	2 nm	2 nm
Si thickness	TSi	10 nm	10 nm	10 nm
Source length	L_S	20 nm	20 nm	20 nm
Channel Length	LCH	50 nm	50 nm	50 nm
Source doping	N_A	1×10^{20}cm^{-3}	1×10^{20}cm^{-3}	1×10^{20}cm^{-3}
Channel doping	Intrinsic	1×10^{16}cm^{-3}	1×10^{16}cm^{-3}	1×10^{16}cm^{-3}
Drain doping	N_D	5×10^{18}cm^{-3}	5×10^{18}cm^{-3}	5×10^{18}cm^{-3}
Work function (Tunnel gate)	ϕM1	4.25 eV	4.20 eV	4.20 eV
Work function (Auxiliary gate)	ϕM2	-	5.60 eV	5.60 eV

Work Function of Metal-2 (M-2): A higher work function can increase the barrier height, making it more challenging for carriers to tunnel through the barrier. A higher work function at Metal-2 might help in better modulating the off-state behaviour by effectively controlling the tunneling barrier width or reducing the tunneling probability in the off-state. This could potentially reduce the off-state leakage current of the TFET.

When the tunnel gate's work function is appropriately aligned with the energy bands of the channel material, it facilitates the efficient tunneling of electrons. The alignment can be achieved by selecting a tunnel gate material with a suitable work function or by employing a work function engineering technique.

If the work function of the tunnel gate is too high, it creates a larger energy barrier, which can impede the tunneling process. On the other hand, if the work function is too low, it can lead to increased off-current and diminished transistor performance. Therefore, in TFET design, it is crucial to select a tunnel gate material with an appropriate work function to optimize the device's overall performance.

4.2 Performance Comparision

In evaluating the performance of various metal combinations for the devices Structure 2 and Structure 3, it is evident from Figs. 3, 4, 5 & 6 that the combination of aluminum (M-1) with a work function of 4.20 eV and platinum (M-2) with a work function of 5.60 eV would perform the best, in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, and Sub threshold swing than other metal-gate combinations.

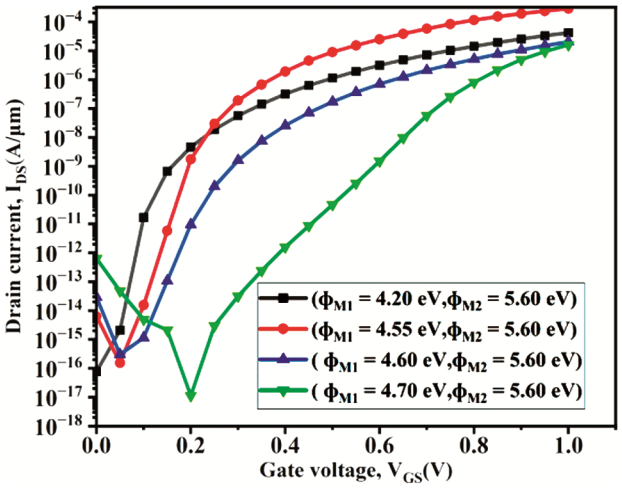

Fig. 3 — Comparison of I_{DS} vs V_{GS} curve of the DMG TFET as shown in [Fig. 1(b)] by varying the work functions of the metals M-1 and M-2.

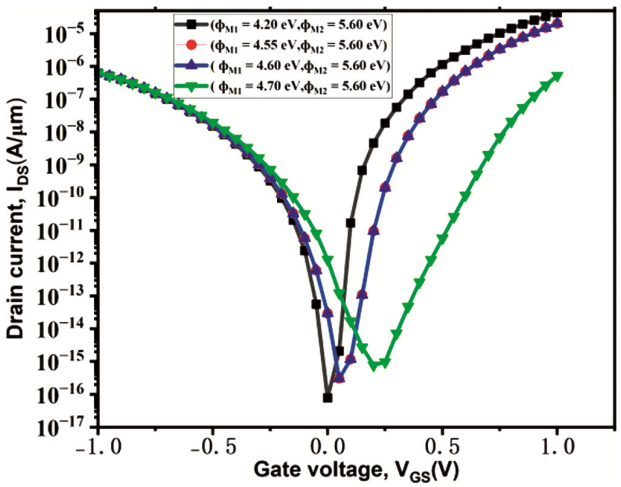

Fig. 4 — Comparison of Ambipolar currents of the DMG TFET as shown in [Fig. 1(b)] by varying the work functions of the metals M-1 and M-2.

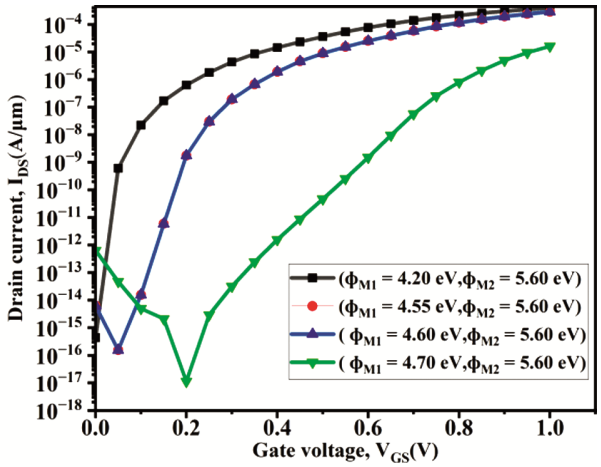

Fig. 5 — Comparison of I_{DS} vs V_{GS} curve of the DMG-HD TFET as shown in [Structure 3] by varying the work functions of the metals M-1 and M-2.

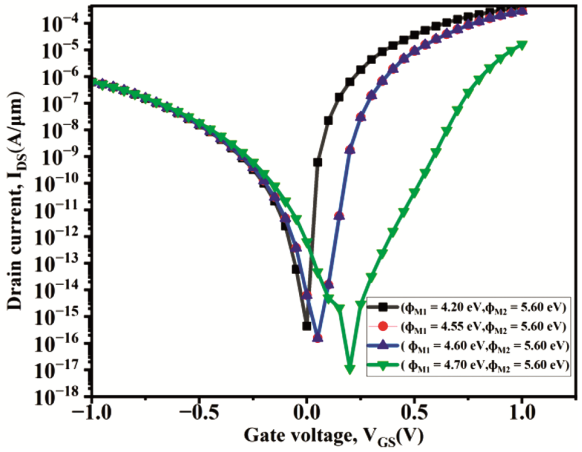

Fig. 6 — Comparison of Ambipolar currents of the DMG-HD TFET as shown in [Structure 3] by varying the work functions of the metals M-1 and M-2.

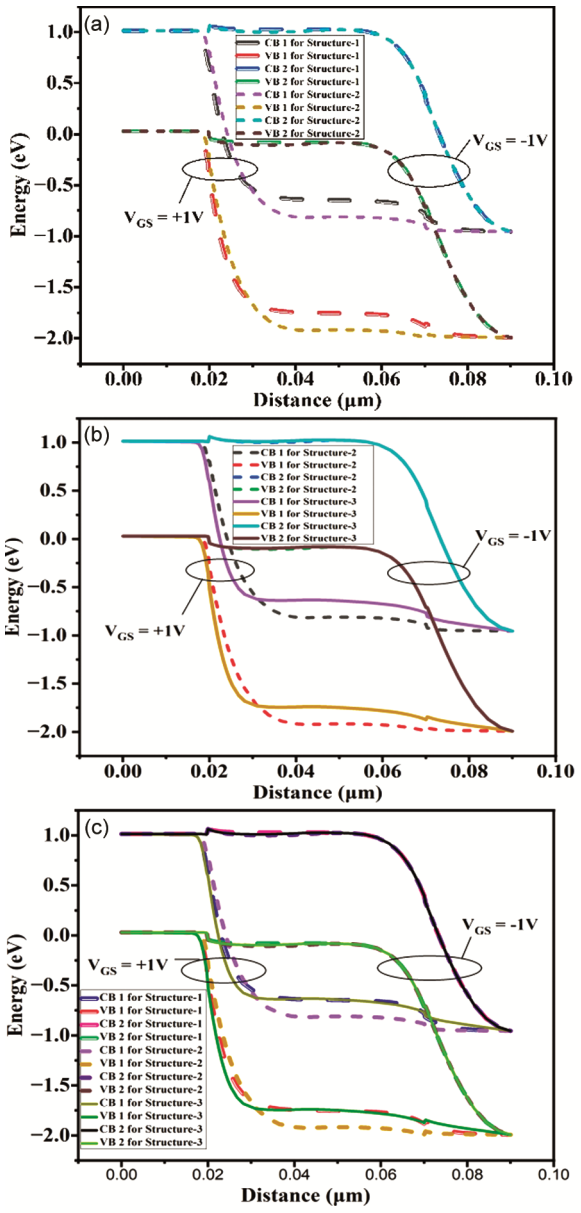

Fig. 7 — Comparison of Energy-band diagrams for (a) Structure- 1,2 (b) Structure-2,3 and (c) Structure-1,2,3

In Fig. 7, the band diagrams illustrate the energy levels and electron behaviour in the DG TFET, DMG TFET, and DMG-HD TFET for different gate and drain voltages.

In Fig. 7(c) compared to the Double gate TFET, the tunneling barrier width is significantly smaller in the Hetero dielectric dual metal gate TFET due to the influence of the high-k dielectric. This smaller barrier width facilitates more efficient electron tunneling across the barrier. As a result, the ON current of the Hetero dielectric dual metal gate TFET improves, and the Sub threshold swing decreases.

Table 3 — Shows the tunneling barrier width when V_{GS} = +1V

Structure	Tunneling barrier width in ONstate
Structure 1 (Conventional Struc-ture)	5.2 nm
Structure 2	5.1 nm
Structure 3 (Proposed Structure)	4.5 nm

Table 3 illustrates that the width of the tunnel barrier width in the proposed device, specifically the DMG-HD TFET in its ON state, is reduced because of the inclusion of the High-k dielectric material in the p^+ source-channel region. This reduction in barrier width increases the likelihood of tunneling occurring at the source-channel region, consequently leading to an improvement in the current during the ON state. By reducing the tunneling barrier width, high-k dielectrics can improve the performance of semiconductor devices. For example, they can enable the scaling of transistors to smaller dimensions, leading to higher device densities and improved circuit performance.

4.3 Transfer Characteristics

Transfer Characteristics of DG TFET and DMG-HD TFET (Proposed device) are shown in Fig. 8. By referring Fig. 9 Band-to-band generation is the process where electrons from the valence band gain enough energy to transition to the conduction band, creating electron-hole pairs. band-to-band generation is primarily influenced by the material properties of the semiconductor itself, such as its bandgap energy and electron affinity. In Structure 3 high-k dielectrics are used to improve the performance of TFETs, but they do not have a direct impact on band-to-band generation in the device. The electric field plays a vital role in analyzing the performance and functionality of TFETs. A high electric field peak near the source-channel interface reduces tunnel barrier width, thereby facilitating the attainment of a substantial ON-state current (see Fig. 10). As a result, the most notable tunneling occurrences take place near the source-channel junction, where the BTBT rate (denoted as G_{BTBT}) relies on the existence of a particular electric field (ε), as outlined in equation 1 below.

$$G_{BTBT} = A\varepsilon^{\sigma}\exp^{(-B/\varepsilon)} \quad \ldots (1)$$

In equation 1, constant A symbolizes the effective mass of the electron, while constant B quantifies the likelihood of tunneling, and σ stands for the transition constant.

In Structure 3 by introducing a high-k dielectric material near the source-channel region, the effective dielectric constant in that area is increased. This

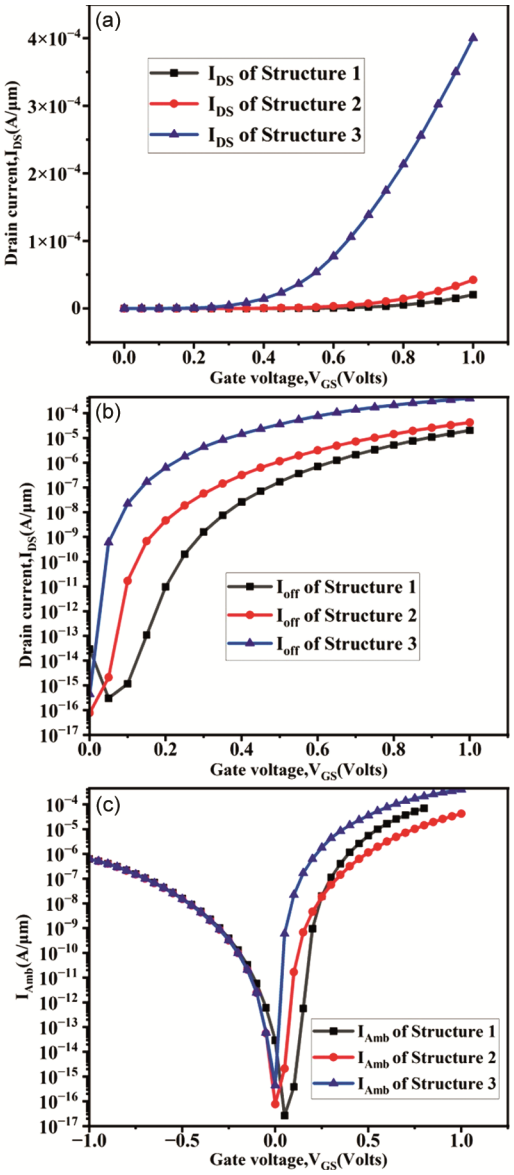

Fig. 8 — Transfer characteristics of (i) DG TFET [Fig. 1(a)] (ii)DMG TFET [Fig. 1(b)] (iii) DMG-HD TFET [Fig. 1(c)].

change in dielectric constant alters the electric field distribution in the TFET structure. The high-k dielectric increases the electric field strength, which helps to enhance the tunneling probability and increase the ON-state current (as shown in Fig. 9).

To understand the cause of less off-state current in structure 3, the energy band diagram of all three structures has been plotted at zero gate bias (see Fig. 11). This diagram shows that using a dual metal gate (structure 2) increases the coupling between the gate and channel region, reducing the energy barrier near the source-channel barrier. Incorporating dual-dielectric (structure 3) further

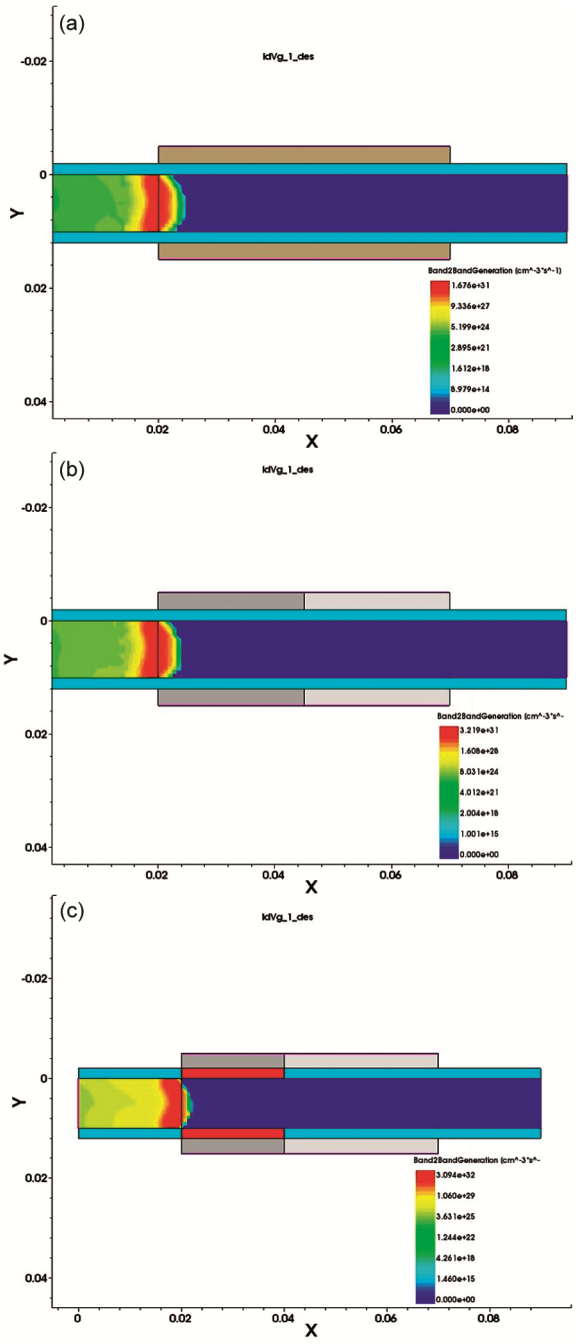

Fig. 9 — Electron band-to-band generation rate for (i) DG TFET [Fig. 1(a)] (ii) DMG TFET [Fig. 1(b)] (iii) DMG-HD TFET [Fig. 1(c)].

strengthens the coupling between the gate and channel region near the source-channel junction, reducing the energy barrier. Due to the dip in the conduction band of structure 3 (shown in a solid red colour line), charge carriers will experience a little barrierwhile moving from channel to drain when compared with the other two structures. Therefore, the off-state

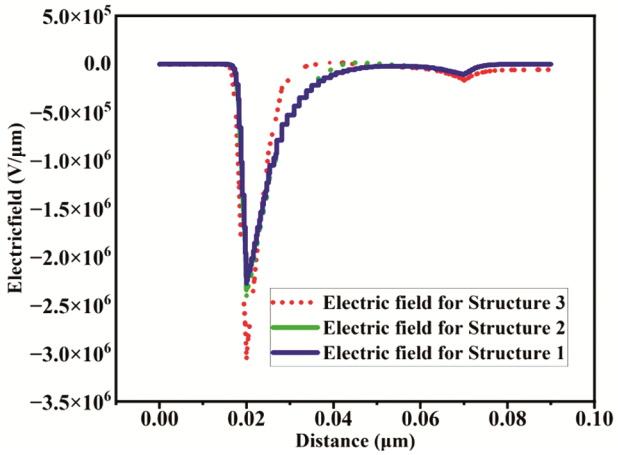

Fig. 10 — Electric field component of (a) DG TFET, (b) DMG TFET and (c) DMG-HD TFET.

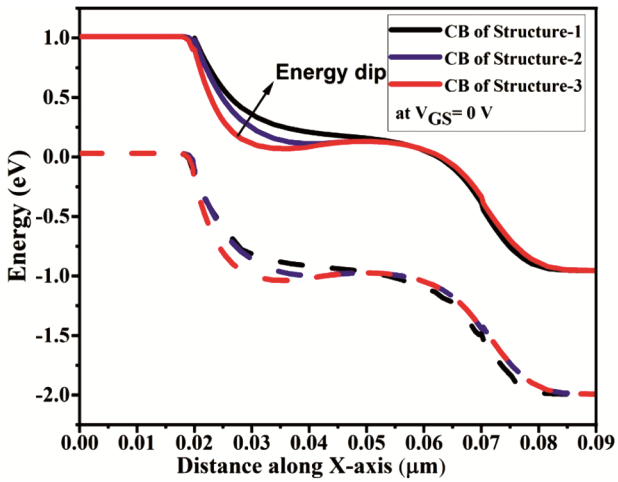

Fig. 11 — Comparison of Energy band diagrams for Structures 1,2 and 3 at V_{GS} = 0V.

current is less in structure 3 followed by structure 2 and structure 1 (see Fig. 8(b)).

4.4 Optimization

This section uses graphical representation to show how the resulting structure is taken into consideration using lengths of M-1, HfO_2, and M-2, SiO_2 of 20 nm and 30 nm, respectively. Here are a few charts. Figs. 12-16 depicts how ON-current (I_{ON}), OFF-current (I_{OFF}), ON-current ratio to OFF-current ratio (I_{ON}/I_{OFF}), Sub-threshold swing (S.S), Ambipolar current (I_{Amb}) changes, depending on how long the metals and oxides are. The proposed architecture (DMG- HD TFET) has been optimized for the metal gate to dielectric length ratios, leading to the emergence of work function valuesof 4.20 eV and 5.60 eV to be used as M-1 and M-2. Performance comparison between DG TFET (Conventional

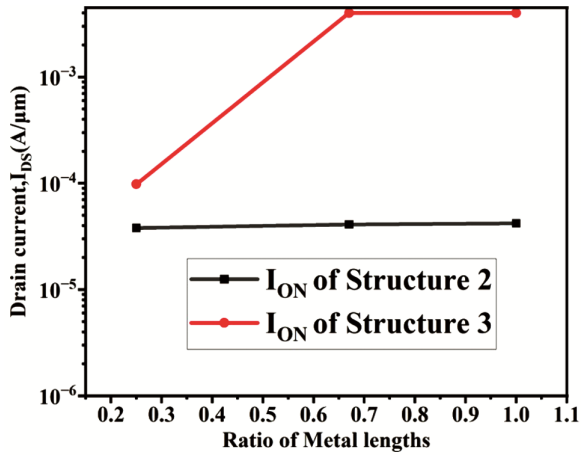

Fig. 12 — Variation of ON current for change in metal lengths along with the dielectric lengths of (a) DMG TFET (b) DMG- HD TFET.

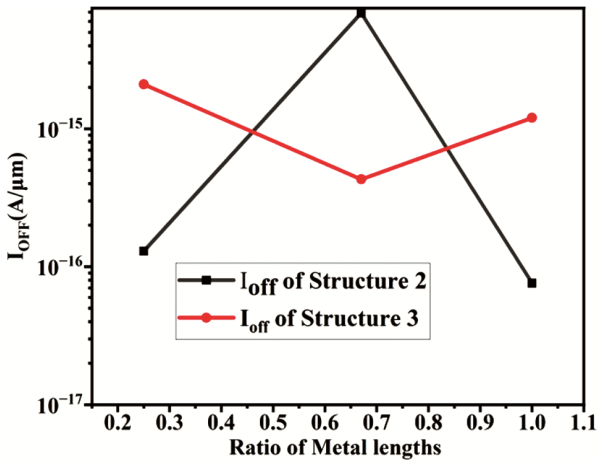

Fig. 13 — Variation of OFF current for change in metal lengths along with the dielectric lengths of (a) DMG TFET (b) DMG- HD TFET.

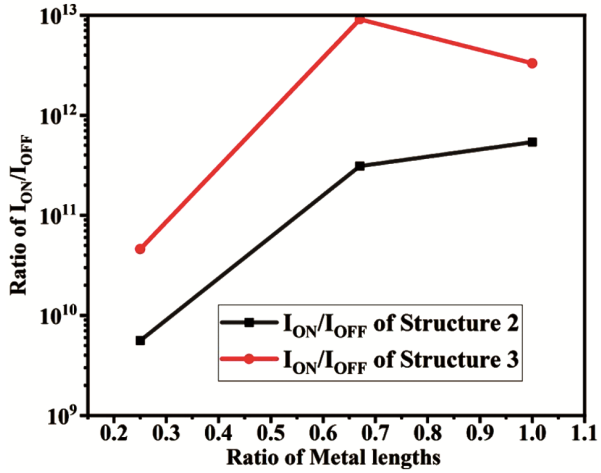

Fig. 14 — Variation of I_{ON} /$I_{OF\ F}$ current for change in metal lengths along with the dielectric lengths of (a) DMG TFET (b) DMG-HD TFET.

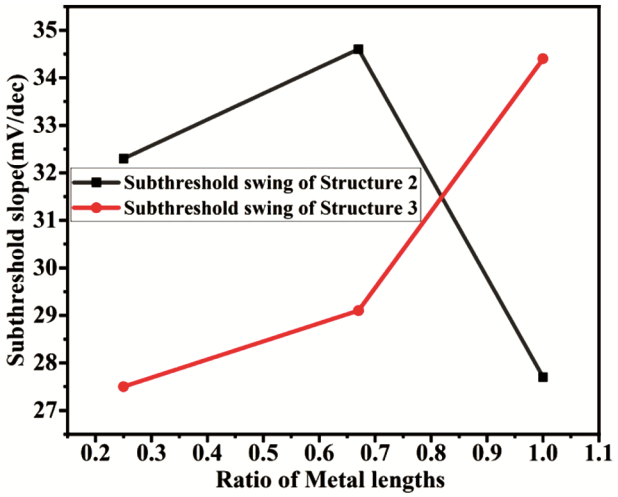

Fig. 15 — Variation of Subthreshold swing for change in metal lengths along with the dielectric lengths of (a) DMG TFET (b) DMG-HD TFET.

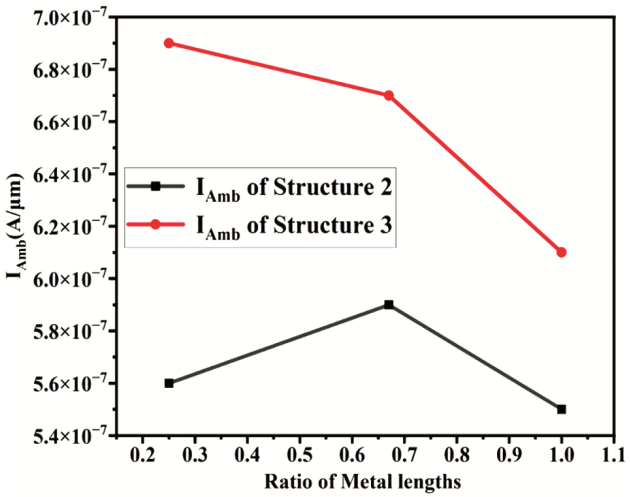

Fig. 16 — Variation of I_{Amb} current for change in metal lengths along with the dielectric lengths of (a) DMG TFET (b) DMG-HD TFET.

Table 4 — Shows the comparison between DG TFET (Conventional structure), DMG TFET and DMG-HD TFET (Proposedstructure).

Structure	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	Subthreshold Swing (mV/decade)	I_{Amb} (A/μm)
Double Gate TFET (Conventional device)	6.9×10^{-5}	1.6×10^{-14}	4.3×10^{9}	38.2	8.8×10^{-7}
DMG TFET	4.2×10^{-5}	7.6×10^{-17}	5.4×10^{11}	27.7	5.5×10^{-7}
DMG-HD TFET (Proposed device)	4.0×10^{-3}	4.3×10^{-16}	9.1×10^{12}	29.1	6.7×10^{-7}

structure), DMG TFET and DMG-HD TFET (Proposed structure) is shown in Table 4.

Figure 12 depicts the alterations in ON current when comparing structure 2 to structure 3. The improved ON-state current in structure 3 can be attributed to the incorporation of a high-k dielectric, leading to enhanced control and management of the channel.

In structure 3, the incorporation of high-k dielectric materials enhances gate capacitance, resulting in improvement in gate electrostatics integrity. This improvement leads to a sharper sub-threshold slope and a decrease in off-state current so that $I_{ON}/I_{OF\ F}$ is also increased as compared to structure 2 (shown in Figs. 13, 14 & 15). The variation in the ambipolar current of structures 2 and 3 with the ratio of metal lengths is shown in Fig. 16. Performance comparison between DG TFET (Conventional structure), DMG TFET and DMG-HD TFET (Proposed structure) is shown in Table 4.

5 Conclusion

This article examines the Dual Metal Gate Hetero Dielectric (DMG-HD) TFET outcomes to address the challenges of conventional TFET using 2-D simulations. Through this research, it found that hetero-structures exhibit lower threshold voltages. This is attributed to the presence of a high-k dielectric near the tunnel junction, which enhances the coupling of the gate voltage to the tunnel junction, which results in tunneling at a lower gate voltage. DMG-HD TFET improvises the drain current from an order of 10^{-5} to 10^{-3}, I_{ON}/I_{OFF} ratio increases from an order of 10^{9} to 10^{12}, and SS by 23.82% over the Conventional device (DG TFET).

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