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BDCDTA-based Reconfigurable Frequency Selective Filter Structures for Medium Wave Communication and Biomedical Signal Processing Applications

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Frequency-selective filters are usually required at the receiving end of a communication system to change the frequency range of a band-pass filter (BPF), which is used to extract the broadcast signal. In this study, we have designed such frequency-selective filters using a novel bulk-driven current differential transconductance amplifier (BDCDTA) as its fundamental building block. This BDCDTA is first used to create a biquad filter, and the designed filter is then reconfigured for frequency selection. The proposed frequency-selective filter structures have the capability of providing a constant gain based on the communication system's requirements. The suggested structures with CMOS 180 nm technology parameters are validated using PSPICE and the Cadence Virtuoso design environment. The theory is confirmed by pre and post-layout simulation. PVT corner and Monte-Carlo analysis demonstrate its applicability for a broad range of applications and provide a range for its use under various conditions. This design is suitable for low voltage and low power applications due to the bulk-driven transistors, and the suggested structures are designed especially for medium wave communication and biomedical signal processing.

Keywords: Reconfigurability; Frequency selective filter (FSF); Bulk-driven current differential transconductance amplifier (BDCDTA); Band-pass filter (BPF); Communication system

1 Introduction

The rising demand for multiband communication systems, which require designing with fewer components, has drawn more attention to programmable or reconfigurable circuits for research and development[1-4]. Tuneable and programmable band-pass filters[4-8] have drawn a lot of attention because they can replace massive filter banks in frequency-selective systems. One must be able to modify the filter's shape, gain, bandwidth (BW), and frequency range; this can only be done with the help of a reconfigurable filter structure, which in itself should have a simple design with minimal components. To accomplish this goal, this study describes alternative frequency selective filter (FSF) structures that can be used, depending on the desired gain and frequency range.

The current difference transconductance amplifier, is an essential active component in current mode signal processing due to its ability to provide high output and low input impedances[9-13]. As outlined in[14], this CDTA block has been widely used in a variety of circuits, including filters[15-17], rectifiers[18-20], oscillators[21-22], modulators[23], multipliers[24], current limiters[25], square-rooters[26], squarer[26], Schmitt triggers[27], and dividers[26].

Furthermore, bulk-driven technology, which emerged from CMOS technology, operates at a lower voltage, resulting in a significant advantage of substantially lower power consumption. However, because bulk-driven transistors have lower bandwidth and transconductance than gate-driven metal oxide semiconductor field effect transistors (MOSFETs), bulk-driven circuits have a substantially lower gain bandwidth than gate-driven MOS circuits. This is the reason why the bulk-driven CDTA (BDCDTA) that was proposed in[28] is insufficient for transconductance control and frequency selectivity. The improved design that we have proposed can enable the implementation of the frequency selection filter by varying the transconductance with the help of only one such element. It reduces the number of components while providing a suitable and easily integrated design.

Frequency agile filters based on CDTA were proposed in[29-31], whereas other elements based filters were reported in[32-35]. Each of these topologies, either overcomplicated the circuit by requiring too many

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components or failed to control the transconductance while simultaneously altering the frequency range. This study's main objective is to present multiple reconfigurable filter topologies that each only require a single, integration-suitable BDCDTA element with two capacitors and one resistor. These frequency-selective filter topologies are developed especially for use in medium-wave communication and biomedical signal processing. In this work, we have proposed the following:

- A novel performance-upgraded BDCDTA.
- Reconfigurable frequency selective filter structures utilizing this novel performance-upgraded BDCDTA.
- Tunable filters with and without constant gain for medium wave communication and bio-medical signal processing applications.

This paper presents our study as follows: Section 2 provides a performance-upgraded BDCDTA circuit description. Section 3 incorporates proposed reconfigurable frequency-selective filter structures, while Section 4 includes simulation results, relevant discussion, and performance evaluation. Section 5 contains conclusions and predictions for the future.

2 Characteristics of proposed performance upgraded BDCDTA circuit and its simulation results

The schematic block diagram realizing the proposed performance upgraded BDCDTA is shown in Fig. 1.

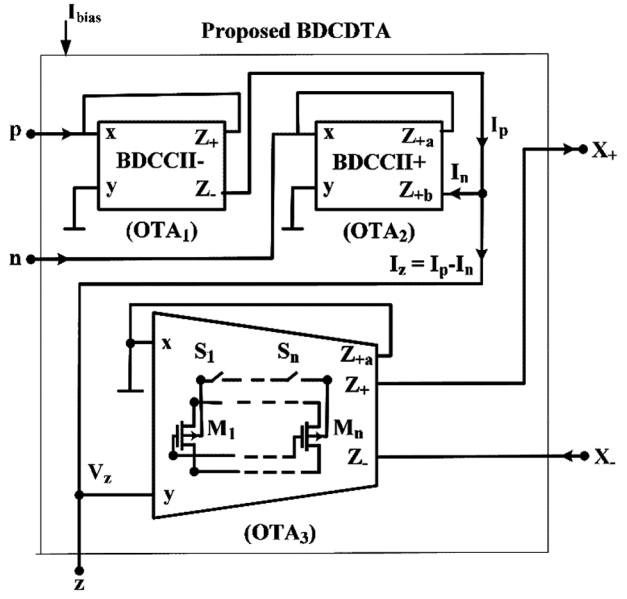

Fig. 1 — Schematic block diagram of performance upgraded BDCDTA.

It consists of a total of three bulk-driven operational transconductance amplifiers (OTAs) with the input terminals connected to the first two OTAs while output is taken from the third OTA with dual polarity. The first two OTAs behave as current conveyors (CCII) in a manner to pass the two input currents and form the current difference unit while the third one provides the required transconductance gain. For the first bulk-driven current conveyor (BDCCII), the applied current I_p moves from its 'z-'terminal, and for the next BDCCII the current I_n moves towards its 'z_+' terminal, hence both are in the opposite direction. Therefore, the current, obtained at the z terminal of this BDCDTA, comes out to be simply the difference between these two currents I_p and I_n.

The characteristics of the performance-upgraded BDCDTA are described by the set of equations below:

$$I_z = I_p - I_n$$
$$V_p = V_n = 0$$
$$V_z = I_z * R_z$$
$$I_{x+} = n\, g_{mb} V_z \text{ and } I_{x-} = -n\, g_{mb} V_z \quad \ldots(1)$$

where 'n' is the number of transistors utilized in the split network, g_{mb} is the transconductance of the bulk-driven OTA, and R_z is the external impedance coupled to the 'z' terminal to generate the appropriate voltage V_z.

The function of the third OTA is to provide sufficient gain, but due to bulk mode, its transconductance (g_{mb}) is naturally much lower than its conventional counterpart (g_m). So, to improve its value we have used a split transistor network approach to increase the output current and hence the overall trans-conductance. The value of the current I_D for the bulk-driven MOSFET can be obtained as

$$I_D = \frac{\beta}{2}\{V_{SG} - V_{TP0} - \gamma_p(\sqrt{V_{BS} + 2\emptyset_f} - \sqrt{2\emptyset_f})\}^2 \quad \ldots(2)$$

with $\beta = \mu_p C_{ox} \frac{W}{L}$

where V_{SG} is source to gate potential, V_{TP0} is threshold voltage without any substrate voltage, μ_p is hole mobility for PMOS, C_{ox} is oxide capacitance and W/L is the aspect ratio of the transistor. It suggests that the total current I_D can be raised by increasing the aspect ratio, even when the gate to source potential and the bulk to source potential remain constant.

The transistor level implementation of the BDCDTA using this split transistor network in OTA_3 is proposed in Fig. 2. We have used transistors M_{25},

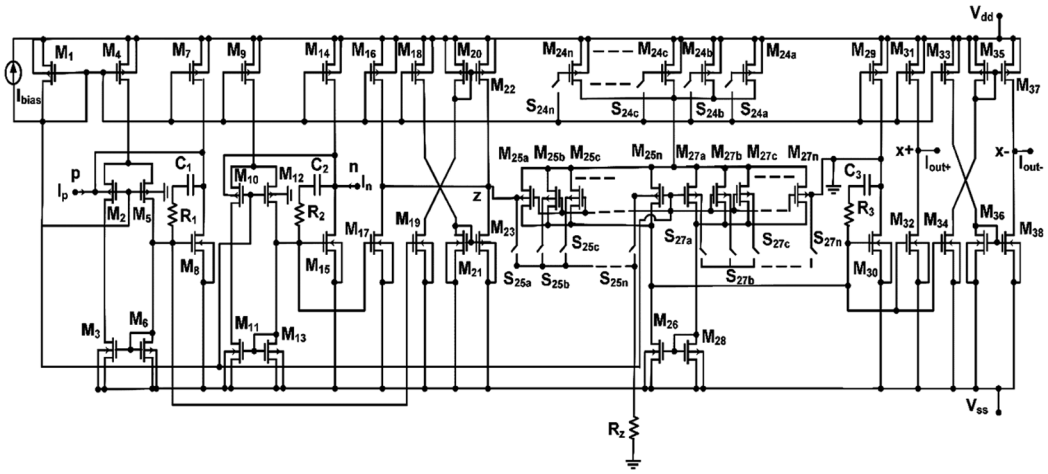

Fig. 2 — Transistor level implementation of performance-upgraded BDCDTA.

M_{27} as well as M_{24} as 'n' parallel transistors as mentioned as M_{25a} to M_{25n}, M_{27a} to M_{27n} and M_{24a} to M_{24n} respectively. Suitable size selection provides not only better transconductance but also increased bandwidth with increasing the value of 'n'.

A current bias is also utilized, as shown in Fig. 2, to guarantee that the circuit is properly biased and has electronic tuning capabilities. Transistor M_1 is biased in such a way that it can offer sufficient potential to the gate terminals of the bulk-driven transistors in all three OTAs, while simultaneously supplying biasing current to all the other transistors employed for this purpose. Switches S_{25a} to S_{25n}, S_{27a} to S_{27n}, and S_{24a} to S_{24n} are used to select the required number of transistors as per the requirement of gain and bandwidth.

The small signal analysis of the input current difference section confirms that the current gain of the current differencing unit is unity with equivalent transistor ratios as specified in Table 1. Further, the small signal analysis of the OTA section confirms the relation of output current in proportion to the number of transistors used in this section as mentioned in Equation (1).

2.1 Simulation results of performance upgraded BDCDTA

The simulations are performed by using PSPICE CMOS 0.18 µm technology parameters. Supply voltages are taken as $V_{DD} = -V_{SS} = 0.6$ V and the biasing current I_{bias} is fixed at 10 uA. The resistance and capacitance combination which is used for frequency compensation to split the parasitic poles of the OTAs and to make the first stage pole dominant are taken as 2.2 kΩ and 0.2 pF respectively for each OTA stage. The transistors' W/L ratios used in the design as shown in Fig. 2 are provided in Table 1.

Table 1 — CMOS transistor W/L ratios used in Fig. 2

Transistors	W/L ratio (µm)
M 1, 4, 9	2.4/0.18
M 24, 25, 27	0.9/0.18
M 2, 5, 10, 12	2.7/0.18
M 3, 6, 11, 13, 26, 28	0.36/0.18
M 7, 14, 29	3.6/0.36
M 16, 18, 20, 22, 31, 33, 35, 37	3.96/0.36
M 8, 15	1.08/0.18
M 17, 30, 32	1.17/0.18
M 19, 21, 23, 34, 36, 38	1.26/0.18

The plot of OTA_3's transconductance (g_m) against the potential V_z that appears at its input terminal is displayed in Fig. 3. The g_m value goes up as the transistor count in the network increases from 365 µS to 862 µS, which is much higher than the existing BDCDTA block available in the literature.

Table 2 lists the specifications of the performance-upgraded BDCDTA circuit with '4' transistors in its OTA network and compares its performance to earlier published research. Since there is only a single BDCDTA in the literature, we included CDTA for comparison of its basic features. Table 2 makes it obvious that adopting this split transistor network technique has greatly boosted transconductance and the gain-bandwidth product.

Figure 4 depicts the histogram of the transconductance gain obtained from Monte Carlo (MC) analysis with a two-transistor network in the OTA_3 section. The mean g_m value is 469.45 µS, with a standard deviation of 0.3 µS. The MC investigation supports the BDCDTA's low sensitivity to transistor mismatch.

The simulations are then carried out in the Cadence environment for process, voltage, and corner (PVT) analysis, as well as the post-layout simulation findings. The MOS transistor corners were [ff, fs, sf, ss], the supply voltage corners ($+V_{DD}$ = $-V_{SS}$) were [595 mV, 605 mV], and the temperature corners were [0, 27 ºC, 50 ºC]. The results of this investigation, including the minimum, typical, and maximum values, are mentioned in Table 3, which confirms the circuit's acceptable performance under PVT variations.

Figure 5 represents the layout of BDCDTA, focusing on its transconductance gain. This setup has one transistor in the OTA3 network and doesn't have any pole compensation. The area of this arrangement was calculated to be 427 μm^2. Additionally, the circuit layout of the currently available BDCDTA was created at the same technology node, following the specified dimensions, and its area was also calculated for comparison. It was determined that the total area occupied by the existing circuit is 7370 μm^2, which is significantly larger in comparison to the proposed design. Fig. 6 (a & b) show the pre and post-layout simulation results for transconductance gain. The results indicate that the extracted parasitic component values are acceptable and have minimal effect on the characteristics.

Later on, this BDCDTA circuit was redesigned to accommodate the requirements of biomedical devices, and parameter values were set accordingly. Here, the derived transconductance range was modified from 7.2 µS to 93.9 µS, and the biasing current was limited to 0.1 µA.

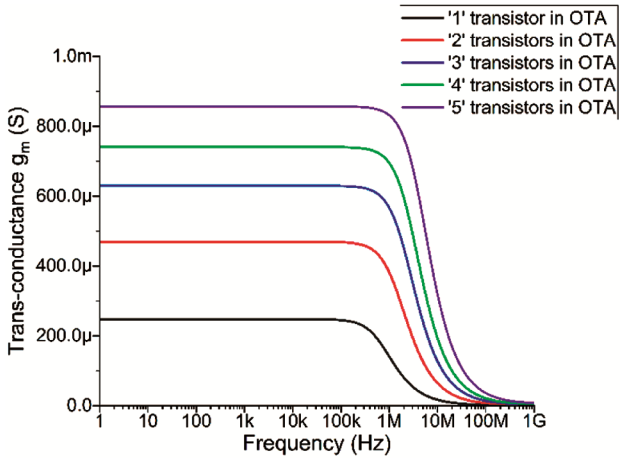

Fig. 3 — Transconductance variation of performance upgraded BDCDTA with the transistor count in the network.

3 Proposed reconfigurable frequency selective filter structures

Frequency agile filters are generally categorized by their basic terms range, adaptability, tunability, reconfigurability, and agility[32]. The filter's center frequency (f_0) range is referred to as the adjustment range. The tunablity is defined as the ratio between the maximum and least center frequency. The range of variation and switching capacity are both described, respectively, by reconfigurability and agility.

The concept of reconfigurable and frequency agile filters was initially described in[33] using a second-order filter and a feedback amplifier. The idea that the

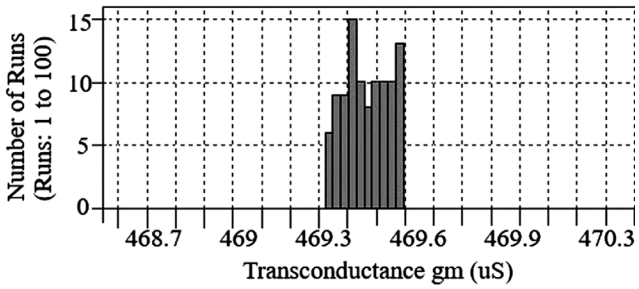

Fig. 4 — Monte Carlo simulation for the transconductance gain of performance upgraded BDCDTA.

Table 2 — Parameter values and performance comparison with the previously reported work

Parameter	Proposed design	Reference[24] 2011	Reference[9] 2006	Reference[10] 2018	Reference[11] 2021	Reference[12] 2021
Device used	BDCDTA	BDCDTA	CDTA	FGCDTA	CDTA	CDTA
Driving method	Bulk-driven	Bulk-driven	Gate-driven	Floating-gate	Gate-driven	Gate-driven
Technology (µm)	0.18	0.18	0.5	0.18	0.18	0.18
Supply voltage (V)	0.6	0.6	2.5	1	0.9	1.5
Power Consumption (µW)	144	144.1	2190	1100	432	525
Bandwidth of I_z/I_p (MHz)	809	16.2	104	52	475	0.45
Bandwidth of I_z/I_n (MHz)	2740	51.6	55	32	480	0.45
DC current swing of I_p, I_n (µA)	-9	-9	-78	-75	-100	-100
Transconductance g_{mb} (µS)	862.2	99.1	480	--	6000	--
Bandwidth of g_{mb} (MHz)	2.4	1.2	--	--	--	--

voltage of the low pass output is first amplified using a gain-adjustable amplifier, which was initially developed for voltage mode circuits, is illustrated in Fig. 7. The amplified voltage is then used to raise the input voltage of the circuit before it. The new input voltage of the filter is then modified and hence the output. In this circuit, the outputs for low pass and band pass are both present.

According to the classification of reconfigurable active and passive filters provided in[32], active filters are a better option because they have lower insertion losses, a smaller footprint, and can be integrated on a chip, but their higher power dissipation needs to be kept to a minimum. This opportunity is given to us by the bulk-driven technique, which helps us to solve the higher power dissipation issue.

Several Biquad implementations in the literature demonstrate the incorporation of multiple active elements. The majority of the reconfigurable filters that have been used up to this point contain these structures, which makes them bulky. Similar issues also arise in circuits with greater orders. Here, we have applied a second-order, single-element filter design approach as described in[29]. We propose the following alternate ways for implementing reconfigurable filter structures that include our recently developed, performance-upgraded BDCDTA and provide variable output.

Table 3 — Process, voltage. Temperature corner analysis

	Min	tt	Max
Current Gain Ix/I_n	1.62	2.76	3.27
Current Gain I_x/I_p	1.65	2.81	3.28
BW of I_x/I_n (MHz)	4.85	5.41	5.59
BW of I_x/I_p (MHz)	4.92	5.45	5.59
Gm (µS)	432.75	527.03	613.54
BW of g_m (MHz)	4.14	4.45	5.42

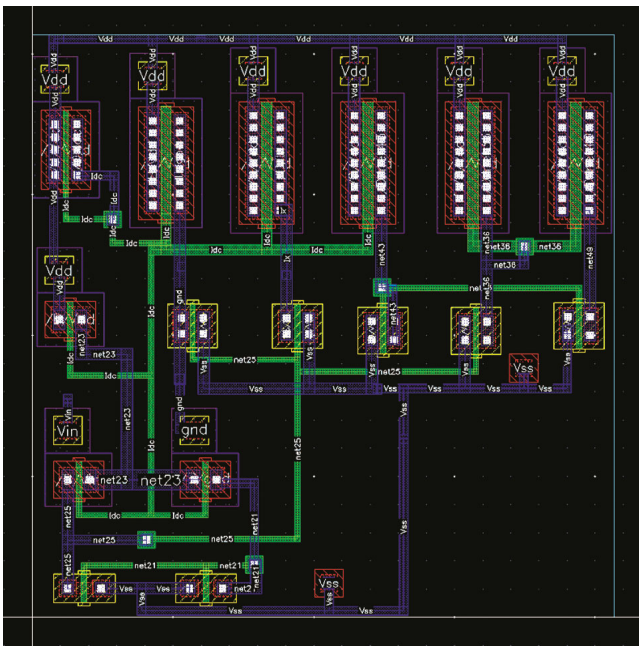

Fig. 5 — Layout of OTA_3 section of BDCDTA with a single transistor in the split network.

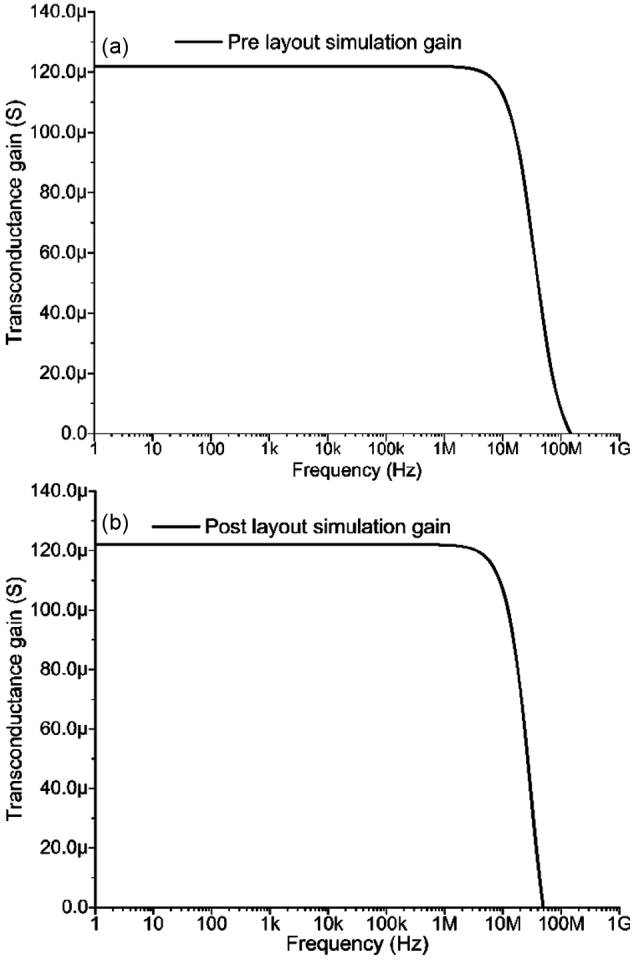

Fig. 6 — (a) - Pre-layout (b) Post-layout simulation results for transconductance gain of the BDCDTA.

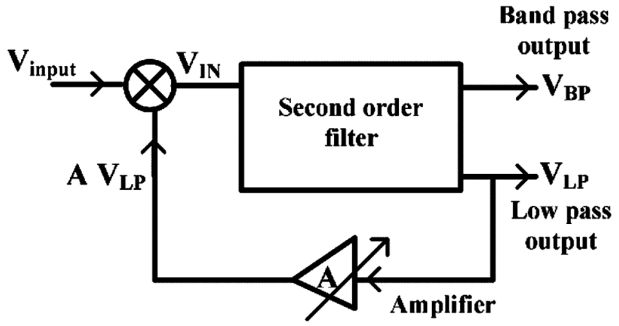

Fig. 7 — Basic concept of frequency agile filter[33].

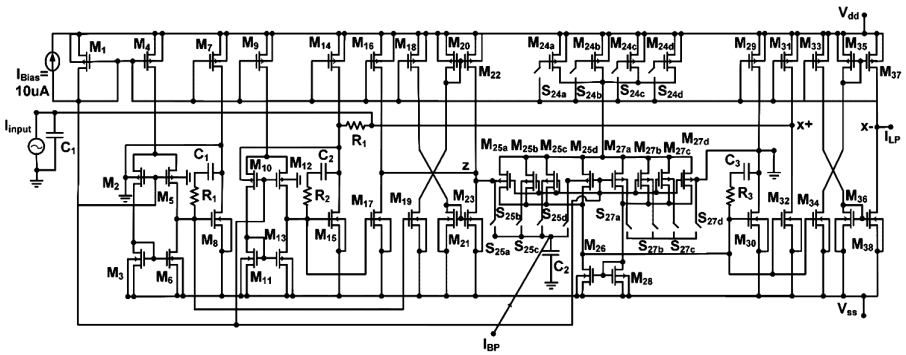

Fig. 8 — Proposed FSF utilizing BDCDTA with split transistor network.

3.1 FSF utilizing BDCDTA with the split transistor network for frequency selection

The circuit based on the idea shown in Fig. 7 uses a feedback network, which increases complexity. In contrast, the structures we have proposed don't employ a feedback amplifier, which reduces the design's size and cost. Fig. 8 depicts the FSF, which implements the second-order filter using our performance-upgraded BDCDTA circuit with a split transistor network as its fundamental component, two capacitors C_1, and C_2, and a resistance R_1. The bandpass output of the BDCDTA is produced by the 'z' terminal, whereas the low pass output is produced by the 'x-'terminal. The transconductance value of the split network, which varies with the number of transistors used in total, adjusts the center frequency of the bandpass filter.

Applying simple mathematical analysis, the following transfer functions are derived at the 'z' and 'x-'terminal of the BDCDTA circuit shown in Fig. 8-

$$\frac{I_{BP}}{I_{in}} = \frac{s\,C_2}{\{R_1C_1C_2s^2+C_2s+n\,g_{mb}\}} \quad \ldots(3)$$

$$\frac{I_{LP}}{I_{in}} = \frac{n\,g_{mb}}{R_1C_1C_2s^2+C_2s+n\,g_{mb}} \quad \ldots(4)$$

where 'n' is the number of transistors employed in the split network of OTA of the BDCDTA and g_{mb} is the transconductance gain of the performance-upgraded BDCDTA block.

The center frequency f_o and the quality factor Q of this filter's key parameters are as follows:

$$w_0 = \sqrt{\frac{n\,g_{mb}}{R_1C_1C_{2mb}}} \text{ and } Q = \sqrt{n\,g_{mb}R_1\frac{C_1}{C_2}} \quad \ldots(5)$$

It is obvious from Equation (5) that the center frequency can be changed without affecting any other parameters by simply adjusting the value of 'n'. The split network's center frequency moves and the quality factor value rises as the number of transistors grows.

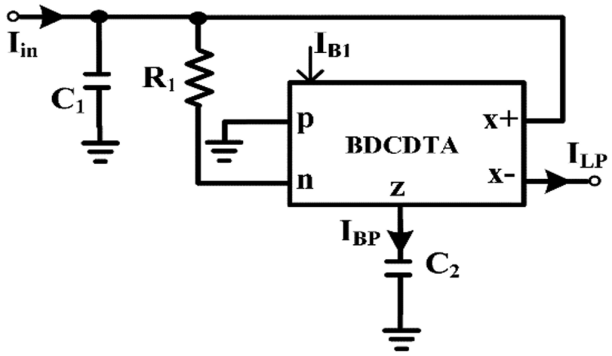

Fig. 9 — Proposed FSF utilizing BDCDTA with current tuning.

3.2 FSF utilizing BDCDTA with current tuning for frequency selection

The performance-upgraded BDCDTA block with a fixed value of 'n' and variable biasing current is used in Fig. 9 to implement the FSF. In this instance, the center frequency of the signal is shifted by a change in the biasing current value.

The transfer function in this case is obtained as:

$$\frac{I_{BP}}{I_{in}} = \frac{s\,C_2}{\{R_1C_1C_2s^2+C_2s+g_{mb}\}} \quad \ldots(6)$$

$$\text{with} w_0 = \sqrt{\frac{g_{mb}}{R_1C_1C_2}} \text{ and } Q = \sqrt{\frac{g_{mb}R_1C_1}{C_2}} \quad \ldots(7)$$

$$\text{where } g_{mb} = \sqrt{2\,\mu\,C_{ox}\left(\frac{W}{L}\right)_{26,28} I_{Bias}} \quad \ldots(8)$$

It is evident from equations (7, 8) that changing the value of the bias current I_{Bias} can shift the center frequency because doing so changes the transconductance, which in turn changes the center frequency.

3.3 FSF utilizing BDCDTA with a current source and passive resistor for frequency selection with constant gain

The structures suggested in sections 3.1 and 3.2 offer a wide enough range for frequency selection, but the calculations above also demonstrate that the center frequency shifting is not independent of the system's

quality factor and gain. A straightforward approach is suggested in Fig. 10 as a way to do this. The variable resistance $R_2$is preceded by a series capacitance C_2at the 'z' terminal.

Applying simple mathematical analysis, the following transfer functions are derived:

$$\frac{I_{BP}}{I_{in}} = \frac{s\,C_2}{\{R_1C_1C_2s^2+(1+g_mR_z)C_2s+g_{mb}\}} \quad ...(9)$$

$$\text{with } w_0 = \sqrt{\frac{g_{mb}}{R_1C_1C_2}}, Q = \sqrt{\frac{g_{mb}R_1C_1}{C_2}}\left(\frac{1}{1+g_mR_z}\right) \quad ...(10)$$

$$\text{and } \left|\frac{I_{BP}}{I_{in}}\right|_{\text{at } f=f_0} = \frac{1}{(1+g_mR_z)} \quad ...(11)$$

Equation (10), in which center frequency is independent of the resistance value R_z, clearly indicates that changing the bias current modifies the transconductance, leading to shifts in the center frequency. However, the gain and quality factor can be suitably altered by adjusting the value of R_z. Thus, a well-designed measure can shift the frequency range without sacrificing the quality factor and maintaining a constant gain.

4 Simulation results and discussion of proposed reconfigurable frequency selective filter structures using performance-upgraded BDCDTA

The simulations were done using PSPICE CMOS 0.18 µm technology parameters. The supply voltages, transistor aspect ratios, and resistance/capacitance combinations employed in the BDCDTA circuit for frequency compensation are the same as those described in Section 2. First, the parameters were chosen to design the FSF for medium wave communication systems, and then the design was modified to meet the requirements of equipment used in bio-medical signal processing.

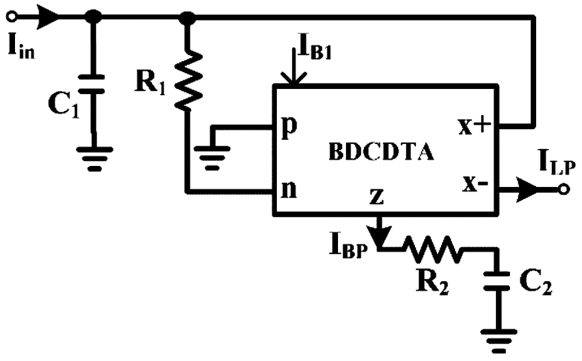

Fig. 10 — Proposed FSF utilizing BDCDTA with a current source and passive resistor for constant gain.

4.1 Simulation results of FSF for medium wave communication

ITU regulations specify a range for medium wave transmission of roughly 300 kHz to 3 MHz, which is ideal for AM radio broadcasting, navigational radio beacons, maritime ship-to-shore communication, etc. The outcomes for the structures specified in Section 3 are retained in line with that.

4.1.1 Simulation results of FSF utilizing BDCDTA with split transistor network for frequency selection

A single transistor in the OTA network of the BDCDTA has a transconductance value of 242 µS while the current I_{Bias} is maintained at 10 µA. The total number of transistors in the split network might range from one to four with the help of selection switches. While R_1 is estimated to have a resistance of 5.5 kΩ, the capacitance values C_1 and C_2 are taken to be 24 pF and 45 pF, respectively.

The results are displayed in Fig. 11. The obtained frequency f_0 for a single transistor in the network is 1.15 MHz, whereas it is 1.64 MHz for all four transistors together in the network. Note that the quality factor and gain of the filter response increase with the number of transistors.

4.1.2 Simulation results of FSF utilizing BDCDTA with current tuning for frequency selection

Figure 12 presents the outcomes for the instance shown in Fig. 6. The calculated capacitance values for C_1 and C_2 are 10 pF, each, whereas the estimated value of resistance R_1 is 10 kΩ. In this situation, the overall number of transistors in the OTA is fixed. With an input bias current of 1 µA to 30 µA, a total of two transistors can supply the transconductance variation of 38 µS to 857 µS. The frequency shift

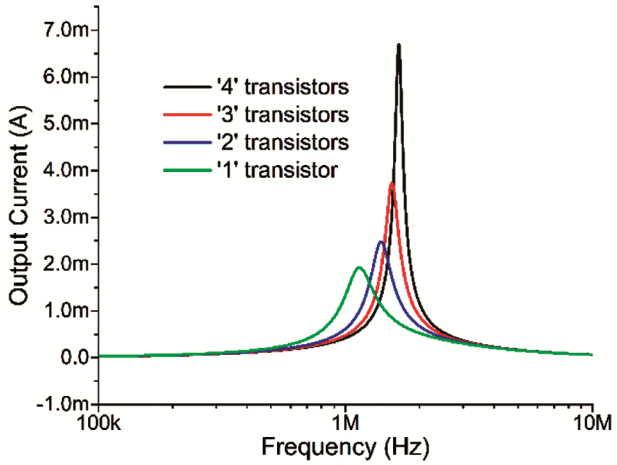

Fig. 11 — Simulation results of FSF utilizing BDCDTA with split transistor network.

obtained in this case spans the entire medium frequency range, from 495 kHz to 4.1 MHz.

4.1.3 Simulation results of FSF utilizing BDCDTA with a current source and passive resistor for frequency selection with constant gain

According to Fig. 10 and Equations (9) to (11), a variable resistor with an initial value of 8 kΩ is added to the 'z' terminal of the BDCDTA while maintaining the other parameters from the prior scenario. To maintain gain when increasing input bias current from 1 µA to 30 µA, the resistance value varies between 8 kΩ to 3.1 kΩ. It offers a steady gain, as depicted in Fig. 13, with a nearly identical quality factor. The outcomes support the theoretical calculations and offer a frequency shift from 501 kHz to 4.89 MHz that is perfectly suited for medium-wave communication.

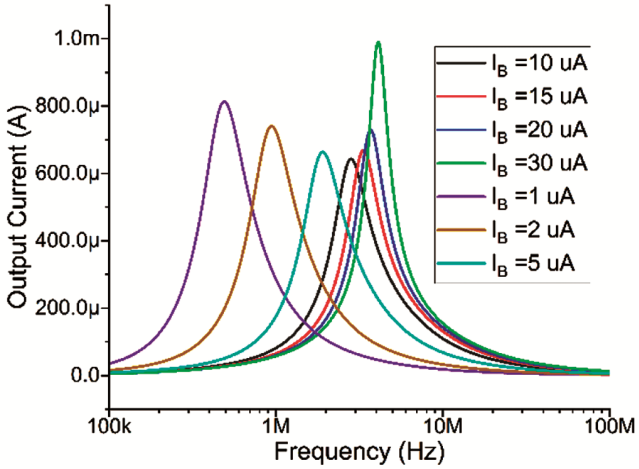

Fig. 12 — Simulation results of FSF utilizing BDCDTA with current tuning.

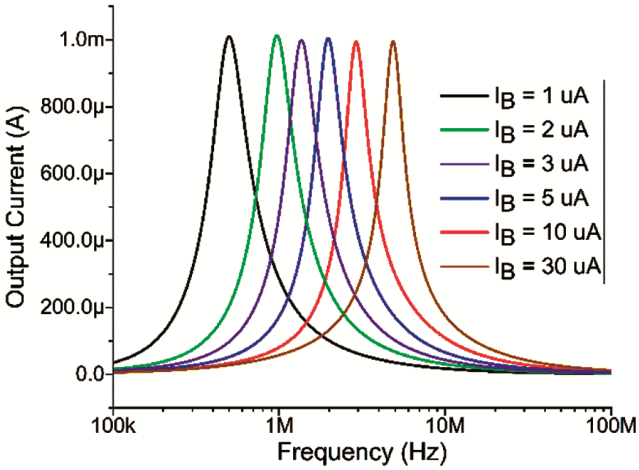

Fig. 13 — Simulation results of FSF utilizing BDCDTA with a current source and passive resistor for constant gain.

4.1.4 Simulation results of FSF utilizing BDCDTA with a variable resistor for frequency selection

To demonstrate the effect of voltage-controlled resistance frequency response, the value of resistance R_1 as shown in Fig. 8 is changed and the resulting frequency shift is displayed in Fig. 14. It shows a frequency shift from 1.5 MHz to 5.4 MHz.

4.2 Simulation results of FSF for bio-medical signal processing applications

The frequency range of bio-medical signals typically ranges from a few millihertz to hertz. Therefore, to acquire the output frequency within the required constraints, we first determined the characteristics of the circuit using the topology shown in Fig. 9. The supply voltages, in this case, are reduced to 0.4 V to operate with weak signals. Biasing current is delivered in the 100nA to 1 µA range. Resistance R_1 is set to 12 kΩ for the second-order filter parameters, and capacitance C_1 and C_2 are each given a value of 12 µF.

The graphs of a bandpass filter with a frequency shift from 215 mHz to 1.2 Hz are shown in Fig. 15 by

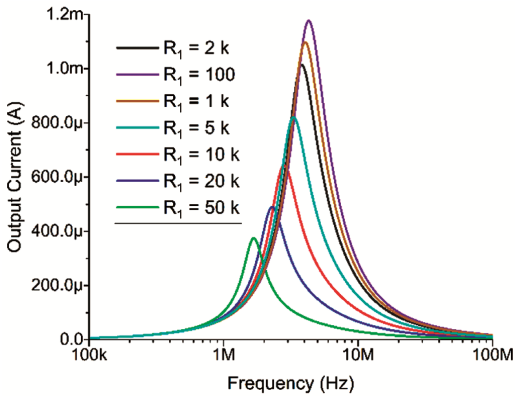

Fig. 14 — Simulation results of FSF utilizing BDCDTA with Resistance R_1 variation.

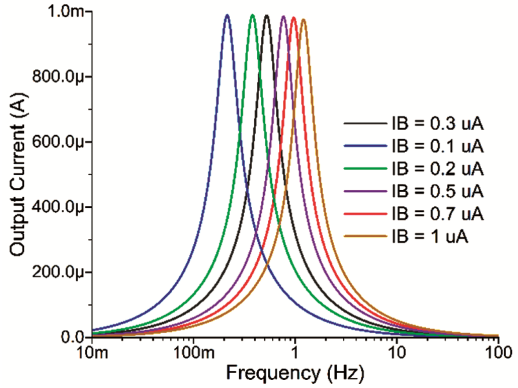

Fig. 15 — Simulation results of FSF for bio-medical signal processing.

increasing the input bias current from 100 nA to 1 μA. It displays a nearly excellent response for bio-medical signal processing applications, with practically constant gain, a comparable quality factor, and frequency shifting from 0.2 Hz to 1.2 Hz.

5 Conclusion

The design that has been proposed to date incorporates the idea of nth-order filters, which increases the size, complexity, and power consumption. Nevertheless, the straightforward structures that we propose, offer a suitable tuning range while also preserving the constant gain of the filter.

The simulation results of the performance-upgraded BDCDTA design clearly show a significant improvement in the gain bandwidth product and transconductance value. Even with more transistors in the split network, the power dissipation is still lower than it is in the existing circuit.

The first FSF structure demonstrates a straightforward idea and the simplest way to alter the frequency range by just changing the number of transistors with the help of a small number of switches. The benefit of this circuit is that, in comparison to previous designs, it doesn't significantly increase power dissipation. The second approach enables simple tuning with the aid of biasing current, and the third one has the benefit of maintaining gain constant. These two ideas provide a wide range of frequency selections.

Based on this study's findings, medium-wave communication and biomedical signal processing can benefit from the newly created structures. In the future, we'll apply this idea to alternative CDTA structures to achieve selectivity for high-frequency range applications.

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