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2D Analytical Subthreshold Model and Inverter/Ring Oscillator Design for TMGS-DG MOSFETs

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This paper presents a 2D analytical model for subthreshold current and swing characteristics in short-channel triple-material symmetrical gate-stack double-gate (TMGS-DG) MOSFETs. The formulation employs drift-diffusion transport principles integrated with virtual cathode analysis to capture minimum channel potential across three distinct gate regions defined by work functions $\phi_{m1} > \phi_{m2} > \phi_{m3}$. Surface potential distribution, derived from parabolic Poisson solutions, yields $\phi_{min} \approx \phi_1 + (\lambda n^2/L1^2)$ $(\partial^2\varphi/\partial x^2)$, enabling explicit expressions for inversion charge $Q_{inv} \propto \exp(-q\phi_{min}/kT)$ and $I_{sub} \approx \mu\ C_{ox}$ $(V_{GS} - V_{FB})$ $(t_{si}/2)$ $\exp(-q\phi_{min}/\eta kT)/L_1$. Subthreshold swing follows $S = (kT/q\ \ln 10)/(1 - \partial\varphi_{min}/\partial V_{GS})$, quantifying short-channel effect (SCE) degradation.Model validation against Silvaco ATLAS™ simulations (drift-diffusion model, Fermi-Dirac statistics, field-dependent mobility) demonstrates excellent agreement for key parameters: t_{si}=20 nm, t_{ox}=2 nm, t_k=4 nm (high-k ε_r=20), $N_A=10^{16}$ cm^{-3}, $N_{SD}=10^{20}$ cm^{-3}, L=60-120 nm. Parametric analysis reveals optimal L_1: L_2: L_3=1:2:3 configuration suppresses off-state leakage by >50 % versus uniform gates while achieving S < 75 mV/decade, with thinner t_{si}/t_{ox} enhancing gate control against DIBL. Circuit demonstrations include TMGS-DG CMOS inverters (VTC gain >30, propagation delay 198 ps) and 3-stage ring oscillators (445 MHz oscillation, rail-to-rail swing), confirming suitability for ultra-low-power digital and RF applications.

Keywords: Triple material symmetrical gate stack double gate (TMGS-DG) MOSFET, Gate stack, Short channel effect, Drains induced barrier lowering, Subthreshold current, Subthreshold swing

1 Introduction

In the last few decades, the engineered MOSFET structures have governed the rapid and significant growth of integrated circuits[1,2]. It happened due to the constant miniaturization of the channel length of MOSFETs, which is in accordance with the international-technology-roadmap for semiconductors (ITRS) report[3, 4]. These downscaled devices have significantly increased packing density, lower power dissipation, and enhanced operating speed[5]. As these devices are downscaled below 100nm, special attention is given to several performance-degrading effects such as hot carrier effects (HCEs), short channel effects (SCEs), etc[6]. To overcome these issues, several approaches, such as novel device architecture[6], alternate device models[6], engineered materials[7], etc. have been adopted. Among these, one of the most promising methods is the dual material gate technology[8]. In this methodology, the device's gate contact is formed by substituting two distinct materials with different work functions instead of a single gate metal. The material with a lower work function is positioned at the drain end of the oxide layer, while the material with a greater work function is positioned at the source end. The screening effect at the gate material having reduced work function causes the high electric field close to the drain end to efficiently suppress the HCEs[9].

The double metal gate (DMG)-MOSFETs have been previously designed and analyzed for their respective performances on the basis of simulations and theoretical models[10]. The first structure of DMG-MOSFETs was proposed[11] in 1999. The proposed model was based on numerical simulation and it was able to solve both the problems of carrier transport efficiency and SCEs. A novel structure of fully depleted DMG silicon on insulator (SOI)-MOSFETs designed and reported a complete simulated analysis

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in 2004, However, they couldn't support their outputs or conclusions with the help of any analytical model[12]. A complete development of the first mathematical model of the threshold voltage and 2D channel voltage for DMG-SOI MOSFETs discussed[13]. In 2009, a drift diffusion-based theoretical model of DMG-SOI MOSFETs with an approximated parabolic potential in the channel region developed[14]. It mitigated the problems associated with the short-channel subthreshold current of DMG-SOI MOSFETs. In order to generate the analytical model for subthreshold current, the surface potential was approximated piecewise. In a similar development, an innovative MOS structure was developed[15] and termed dual-material double-gate (DM-DG) MOSFETs. They further reported that the proposed device structure offers a noteworthy diminution in HCEs, owing to the prominent reduction in the peak electric field close to the drain end. A device schematic of triple material gate-stack double gate (TMGS-DG) MOSFET Proposed by utilizing the benefits of gate stack and straddle gate structure[16]. In further development, a two-dimensional (2D) subthreshold current model for the TMGS-DG MOSFETs was introduced[17], in which they used the evanescent mode analysis to solve the 2D Poisson's equation for the potential circulation in the channel. In 2014, a straddle-gate structure with three gate materials as electrodes to diminish the source-drain leakage current proposed[18]. The effect of multiple number of gate materials on devices performances in terms of electrical parameters discussed in further consecutive years [19, 20]. From the extensive literature survey, it was observed that in order to achieve the desired results significant improvements are required to further reduce the leakage current and subthreshold swing. Therefore, the channel-potential and threshold-voltage analytical model have been investigated for TMGS-DG MOSFET devices. In continuation, the present work reports a two-dimensional analytical model of TMGS-DG MOSFET for the subthreshold current and subthreshold swing. The current analytical model has been validated with the simulation data using the commercially available 2D device simulation program ATLAS TM[21].

2 Methods and Materials

The schematic device structure of TMGS-DG MOSFET used for simulation and analysis is shown in Fig. 1, Where L is the sum of three segmented gate materials ($L = L_1 + L_2 + L_3$), t_k, t_{ox}, and t_{si} are gate

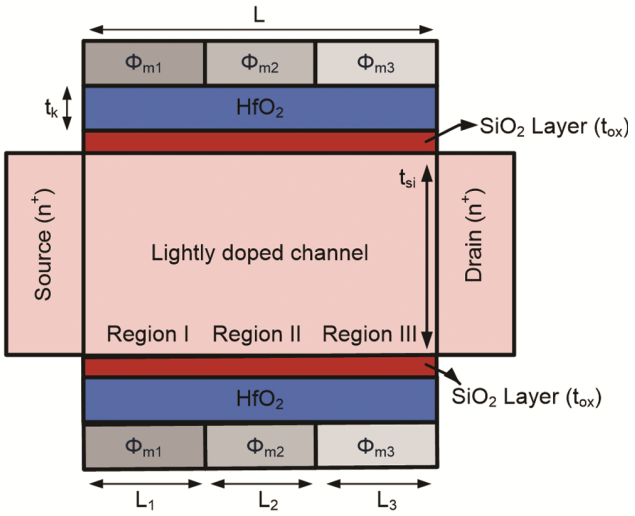

Fig. 1 — Schematic of the proposed device structure of TMGS-DG MOSFET

length, material thickness with high dielectric constant, gate oxide thickness, and channel thickness, respectively. The channel thickness and channel length are considered along with the y and x axes of the schematic structure, respectively.

The gate electrode of the TMGS-DG MOSFET consists of three materials with distinct work functions, ϕ_{m1}, ϕ_{m2} and ϕ_{m3} (such that $\phi_{m1} > \phi_{m2} > \phi_{m3}$) that are deposited over the gate oxide layer over the corresponding lengths L_1, L_2, and L_3, respectively. It is divided into three parts such that, (i) the control gate with the maximum work-function (ϕ_{m1}) placed close to the source end (ii) the first screen gate is a middle material with intermediate work-function (ϕ_{m2}), and (iii) second screen gate with the lowermost work function (ϕ_{m3}) deployed near the drain side. The work-function values of the three gate segments were selected according to the condition $\phi_{m1} > \phi_{m2} > \phi_{m3}$, which establishes a graded electrostatic potential profile along the channel. This work-function engineering improves control of the minimum channel potential and suppresses carrier injection under off-state conditions.

The selected work-function range was chosen to provide a meaningful electrostatic contrast among the three segments while remaining within a practically achievable range for metal-gate technologies. The chosen work function for $(\phi_{m1}, \phi_{m2}, \text{and } \phi_{m3})$ are WSi_2 (ϕ_{m1} = 4.8 eV), $Hf_{0.27}Ta_{0.58}N_{0.15}$ (ϕ_{m2} = 4.6 eV), and $Hf_{0.27}Ta_{0.58}N_{0.15}$ (ϕ_{m3} = 4.4 eV), respectively[22]. The effective gate oxide thickness (t_{eff})[23], which can be expressed as

Eq. (1), is employed in place of t_{ox} in the proposed schematic because the high-k gate stack is used to counteract the SCEs[24].

$$t_{eff} = \frac{\varepsilon_k t_{ox} + \varepsilon_{ox} t_k}{\varepsilon_k} \quad \ldots (1)$$

where, ε_k and ε_{ox} are the dielectric constant of the high-k dielectric and SiO_2 layer, respectively. And, t_k and t_{ox} are the thickness of the high-k dielectric and SiO_2 layer, respectively.

3 Model Derivation

The analytical modeling of subthreshold current has been done by using the drift-diffusion equation in conjugation with the virtual cathode concept.

3.1 Model for Subthreshold Current

The analytical model is based on the two-dimensional Poisson equation in the silicon channel[25].

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{qN_A}{\varepsilon_{si}} \quad \ldots (2)$$

where, $\phi(x,y)$ represents the electrostatic potential in the silicon channel, q is the elementary electronic charge, N_A is the acceptor concentration, and $\varepsilon_{si}$is the permittivity of silicon. For the short-channel double-gate structure, the channel potential is approximated by a parabolic function in the vertical direction.

$$\phi(x,y) = \phi_s(x) + a(x)y + b(x)y^2 \quad \ldots (3)$$

where $\phi_s(x)$represents the surface/channel potential and $a(x)$and $b(x)$are coefficients determined from the electrostatic boundary conditions at the gate interfaces. Considering the symmetrical double-gate structure, the vertical electric-field contribution can be related to the gate-to-channel potential difference. Substitution of the parabolic potential into Poisson's equation results in a one-dimensional differential equation along the channel. The solution is obtained separately for the three gate-controlled regions.

$$0 < x < L_1,\ L_1 < x < L_1 + L_2,\ L_1 + L_2 < x < L$$

The three regions possess different gate work functions. The continuity of electrostatic potential and electric field at the interfaces between adjacent regions is imposed to obtain the complete surface-potential distribution. The minimum channel potential, which determines the subthreshold conduction path, is subsequently obtained from the surface-potential distribution. The minimum potential can be expressed in the form;

$$\phi_{\min} \approx \phi_1 + \frac{\lambda_{n2}}{L_{12}}\left(\frac{\partial^2 \phi}{\partial x^2}\right) \quad \ldots (4)$$

where, $\phi_1$represents the potential contribution associated with the first gate-controlled region, $\lambda_{n2}$is the characteristic natural electrostatic length associated with the second region, and L_{12}represents the effective distance over which the potential variation is evaluated. The minimum potential point in the direction of channel-length potential distribution through the channel is identified as a 'virtual cathode'[26]. It is a crucial point for consideration in device modeling. The subthreshold drain current occurs because of the free electron diffusion from the source to the drain due to the virtual cathode obstruction. The two-dimensional (2D) channel potential distribution throughout the three channel regions can be represented as Eq. (5)[27],

$$\varphi_n(x,y) = \left[M_n \exp(\eta x) + N_n \exp(-\eta x) - \frac{\beta_n}{\alpha} + \frac{p}{4}\left(V_{gs} - V_{fbn}\right)\right] \left(\left[\frac{4}{4+p}\right]\right)\left[1 + \frac{p}{t_{si}}y - \frac{p}{t_{si}^2}y^2\right] - \left(V_{gs} - V_{fbn}\right)y\left[\frac{p}{t_{si}} - \frac{p}{t_{Si}^2}y\right];$$
$$n = 1,2,3, \quad \ldots (5)$$

where, M_n and N_n are unidentified coefficients that can be obtained through the boundary conditions as provided elsewhere[23] and $p = \frac{\varepsilon_{ox} t_{si}}{\varepsilon_{si} t_{ox}}$ is the ratio of channel and oxide capacitance. The permittivity of the gate oxide and silicon are represented as ε_{ox} and ε_{si}, respectively. β_n and α are two arbitrary constant whereas V_{gs} is gate to source voltage.

Using Eq. (6) the virtual cathode potential ($\phi_{vc}(y)$) can be given as;

$$\varphi_{vc}(y) = \left[\frac{4}{4+p}\right]\left[\varphi_{C1\min} + \frac{P}{4}\left(V_{gs} - V_{fb1}\right)\right]\left[1 + \frac{P}{t_{si}}y - \frac{P}{t_{Si}^2}y^2\right] - \frac{\left(V_{gs} - V_{fb1}\right)y}{t_{si}}\left[P - \frac{P}{t_{si}}y\right] \quad k = 1,2,3, \quad \ldots (6)$$

where, λ and N_a are the characteristic length of the center potential and channel doping, respectively. The gate source voltage and flat band voltage are V_{gs} and $V_{fb1,}$ respectively. An exponential relationship exists between the virtual cathode potential ($\varphi_{vc}(y)$) and the inversion charge density (Q_{inv}). Consequently, the density of the inversion carrier charge sheet (Q_{inv}) can be expressed as in Eq. (7)[26],

$$Q_{inv} = n_i \int_0^{t_{si}} \exp\left(\frac{q}{kT}\varphi_{vc}(y)\right) dy \quad \ldots (7)$$

To achieve analytical expression of Q_{inv}, the undoped DG-MOSFET characteristic has been utilized, which allows to locate the effective conduction path at $y = \frac{t_{si}}{4}$ from the silicon surface.

Thus, assuming $y = \frac{t_{si}}{4}$, Q_{inv} can be approximated as follows;

$$Q_{inv} = n_i \int_0^{t_{si}} \exp\left(\frac{q}{KT} \phi_{vc1}(y)\Big|_{y=\frac{t_{si}}{4}} \right) dy \quad \text{... (8)}$$

By putting the value of $\phi_{vc}(y)$ from Eq. (6) into Eq. (8), Q_{inv} can rewrite as,

$$Q_{inv} = n_i t_{si} \exp\left(\frac{q}{KT} \left[V_{gs} - V_{fb1} + \left(\frac{4}{4+P} \right) \times \frac{1}{\varepsilon_{si}} \left(2\sqrt{M_1 N_1}\varepsilon_{si} - \lambda^2 q N_a \right) \times \left(1 + \frac{3P}{16} \right) \right] \right) \quad \text{... (9)}$$

where, the minimum value of potential $\varphi_{C1\min} = \varphi_{C1}(x_{\min})$ along channel length is given by;

$$x_{\min} = \frac{\lambda}{2} \ln\left(\frac{N_1}{M_1} \right) \quad \text{... (10)}$$

The minimum channel potential can be found by using the above equations and can be written as;

$$\varphi_{C1\min} = (V_{gs} - V_{fb1}) + 2\sqrt{M_1 N_1} - \frac{\lambda^2 q N_a}{\varepsilon_{si}} \quad \text{... (11)}$$

According to Pao-Sah double integral[24] formalism, the subthreshold current (I_S) for short channel TMGS-DG MOSFETs can be given as;

$$I_S = \frac{\mu V_T \left(1 - \exp\left(-\frac{V_{ds}}{V_T} \right) \right)}{\int_0^{L_1} Q_1^{-1} dx + \int_{L_1}^{L_1+L_2} Q_2^{-1} dx + \int_{L_1+L_2}^{L} Q_3^{-1} dx} \quad \text{... (12)}$$

where, Q_k is the charge density, and μ is the free carrier's mobility, as defined elsewhere[28]. Thus, the equation for subthreshold current (as given in Eq. (12)) can be obtained by solving the Eqs. (10), (11), and (12).

$$I_S = \frac{\mu V_T \left(1 - \exp\left(-\frac{V_{ds}}{V_T} \right) \right)}{L_1 Q_1^{-1} + L_2 Q_2^{-1} + L_3 Q_3^{-1}} \quad \text{... (13)}$$

Regions 2 and 3 have higher potential than region 1, owing to the step potential profile in short-channel TMGS-DG MOSFET. Hence, the denominator of the first term related to region 1 (i.e, L_1) will dominate, and Eq. (13) can be further transformed into the following Equation,

$$I_S = 2t_{si} q \frac{\mu V_T}{L_1} \left(\frac{n_i^2}{N_a} \right) \times \left(1 - \exp\left(-\frac{V_{ds}}{V_T} \right) \right) \times \exp\left(\frac{q}{kT} \left(V_{gs} - V_{fb1} + \left(\frac{4}{4+P} \right) \times \left(2\sqrt{M_1 N_1} - \frac{\lambda^2 q N_a}{\varepsilon_{si}} \right) \times \left(\frac{16+3P}{16} \right) \right) \right) \quad \text{... (14)}$$

The derived Eq. (14) is further used for analyzing the subthreshold current of short-channel TMGS-DG MOSFET.

3.2 Model for Subthreshold Swing

As the subthreshold current is given as, $I_S \propto \int_0^{t_{si}} n_i \exp\left(\frac{(\varphi_{vc}(y) - \varphi_F)}{V_T} \right)$; where, φ_F is the Fermi potential. With the help of this, the expression for the subthreshold swing (S) of TMGS-DG MOSFET can be given by Eq. (15)[27],

$$S = \left(\frac{\partial \log I_S}{\partial V_{gs}} \right)^{-1} = \ln 10 \left(\frac{\partial \ln I_S}{\partial V_{gs}} \right)^{-1} = \frac{kT}{q} \ln 10 \times \left(\frac{\partial \varphi_{VC1}(y)}{\partial V_{gs}} \right)^{-1} \quad \text{... (15)}$$

It is worth noting that the existence of an undoped channel DG-MOSFET is at $y = \frac{t_{si}}{4}$ and $\frac{3t_{si}}{4}$, thus having an effective conduction path of the sub-threshold conduction at these values only. Based on these criteria, Eq. (15) can be rewritten as follows;

$$S = \frac{kT}{q} \ln 10 \times \left(\frac{\partial \varphi_{VC1}\left(y = \frac{t_{si}}{4} \right)}{\partial V_{gs}} \right)^{-1} \quad \text{... (16)}$$

Further, differentiating Eq. (11) with respect to V_{gs}, it can be observed as;

$$\frac{\partial \varphi_{VC1}\left(y = \frac{t_{si}}{4} \right)}{\partial V_{gs}} = \left(\frac{4\frac{\partial \varphi_{C1\min}}{\partial V_{gs}} + p}{4 + p} \right) \left(\frac{16+3P}{16} \right) - \frac{3p}{16} \quad \text{... (17)}$$

where,

$$\frac{\partial \varphi_{VC1\min}}{\partial V_{gs}} = 1 + \left(\frac{(M_1 - N_1)}{\sqrt{M_1 N_1}} \left(\frac{(\exp(-\eta L) - 1)}{2\sinh(\eta L)} \right) - \sqrt{\frac{M_1}{N_1}} \right) \quad \text{... (18)}$$

By considering Eqs. (16) and (17), the subthreshold swing (S) for short-channel TMGS-DG MOSFET can be given as in Eq. (19),

$$S = \frac{kT}{q} \ln 10 \times \left(\frac{(1+p)\left(\frac{(M_1 - N_1)}{\sqrt{M_1 N_1}} \left(\frac{(\exp(-\eta L) - 1)}{2\sinh(\eta L)} \right) - \sqrt{\frac{M_1}{N_1}} \right) \left(\frac{16 + 3P}{16} \right) - \frac{3p}{16}}{4 + p} \right)^{-1} \quad \text{... (19)}$$

where, L is the total channel length; L_1, L_2, and L_3 are the lengths of the three gate-material segments, respectively; t_{si} is the silicon-channel thickness; t_{ox} and t_k denote the conventional oxide and high-k dielectric thicknesses, respectively; ϕ_{m1}, ϕ_{m2}, and ϕ_{m3} are the metal work functions of the three gate segments; $\phi(x, y)$ is the two-dimensional electrostatic potential in the channel; $\phi_s(x)$ denotes the surface potential; $\phi_{\min}$ is the minimum channel potential; q is the elementary charge; k is Boltzmann's constant; T is absolute temperature; N_A and N_{SD} are the channel acceptor and source/drain doping concentrations, respectively; ε_{si} is the permittivity of silicon; μ is carrier mobility; C_{ox} is the equivalent oxide capacitance per unit area; V_{GS} and V_{DS} are gate-source and drain-source voltages; V_{FB} is the flat-band voltage; and λ denotes the characteristic electrostatic scaling length of the device. All symbols have been defined at their first occurrence and used consistently throughout the revised manuscript. The derived Eq. (19) is further used for analyzing the subthreshold swing of short-channel TMGS-DG MOSFET.

4 Results and Discussion

This section contains the theoretical results of subthreshold behavior (i.e, subthreshold current and swing) for the proposed device model. These results are verified by contrasting them with numerical simulation data that was obtained using the ATLAS™ device simulator[21], which is a commercially accessible tool. The drift-diffusion model is used for carrier transport whereas, for the numerical simulation, classical Fermi–Dirac statistics model is used[27]. The field dependent mobility model has been implemented to integrate the impact of high electric field in the device channel in the ATLAS™ simulation[21]. The ratio of lengths of regions 1, 2, and 3 is taken to be L_1:L_2: L_3 :: 1:1:1 for all the computations. The p-type substrate concentration is selected to be homogenously doped with a doping concentration of $N_A = 1\times10^{16}$ cm^{-3} in all the three regions. The source/ drain regions are heavily doped with a doping concentration of $N_{S/D} = 1\times10^{20}$ cm^{-3}. The dielectric constant value of high-k material is chosen to be 20. The typical values of t_{si}, t_{ox}, and t_k are taken to be 20 nm, 2 nm, and 4 nm, respectively.

From Fig. 2, it can be observed that the subthreshold current (I_s) with gate-to-source voltage (V_{gs}) varies for different ratios of L_1, L_2, and L_3, when the other device parameters are considered to be constant. As the V_{gs} increases, the I_s decreases for a notable change in the values of ratio gate lengths throughout the channel length. The higher ratio of length L_1, L_2, and L_3 provides an advantage to TMGS DG-MOSFET in comparison with conventional MOSFET in terms of the less leakage currents (i.e., lower value of I_s). The plot between I_s versus V_{gs} is for different gate lengths (L= 60, 90, and 120nm) is shown in Fig. 3. From the Fig. 3, it can be seen that the off-state leakage current increases as a change in smaller gate length, which in turn increases the SCEs.

Further, the variation in the I_s with respect to V_{gs} for the different values of silicon channel thickness (t_{si}) and gate oxide thicknesses (t_{ox}), analyzed, maintaining the other parameters constant. Figure 4 shows the plot between I_s and V_{gs} for different values of silicon

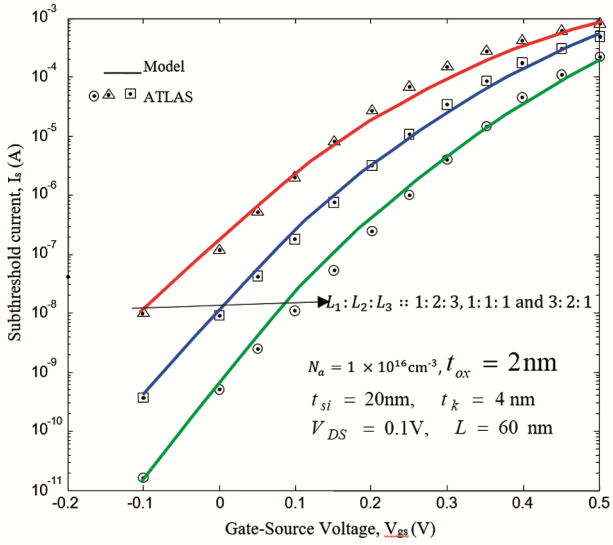

Fig. 2 — Variation in subthreshold current (I_s, in A) with gate-source voltage (V_{gs}, in V) for different ratios of L_1, L_2, and L_3

channel thickness (t_{si}). From the Fig. 4, it can be observed that the subthreshold current increases for higher value of t_{si} and it's due to weakened channel electrostatics as the threshold voltage decreases. Similarly, Figure 5 shows the variation of I_s against V_{gs} for different values of gate oxide thicknesses (t_{ox}). As the t_{ox} is varied from 3 to 2 nm, I_S decreases for a particular value of V_{gs}. It occurs due to the thicker gate oxide, which results in weakened gate electrostatics.

To study of subthreshold swing behavior of the proposed device, plots between subthreshold swing (S) and device channel length (L) for different ratios of L_1, L_2, and L_3, silicon channel thicknesses (t_{Si}), and gate oxide thicknesses (t_{ox}). The variation in the subthreshold swing (S) at different device channel lengths (L) for different ratios of control gate to screen gate length is depicted in Fig. 6. From Fig. 6, it can be seen that the subthreshold swing (S) decreases as the length of the control gate, i.e., L_1: L_2: L_3 ::1:2:3, increases. This is due to the inverse relation between the subthreshold slope and subthreshold swing. And, for the case of $L_1 : L_2 : L_3 :: 1:2:3$, the subthreshold slope is the highest; thus, leading to decrement in

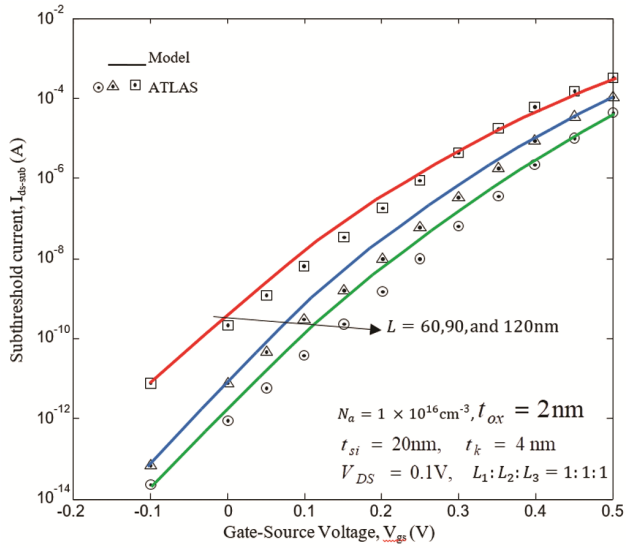

Fig. 3 — Variation in subthreshold current (I_s, in A) with gate-source voltage (V_{gs}, in V) for different gate length (L= 60, 90, and 120 nm)

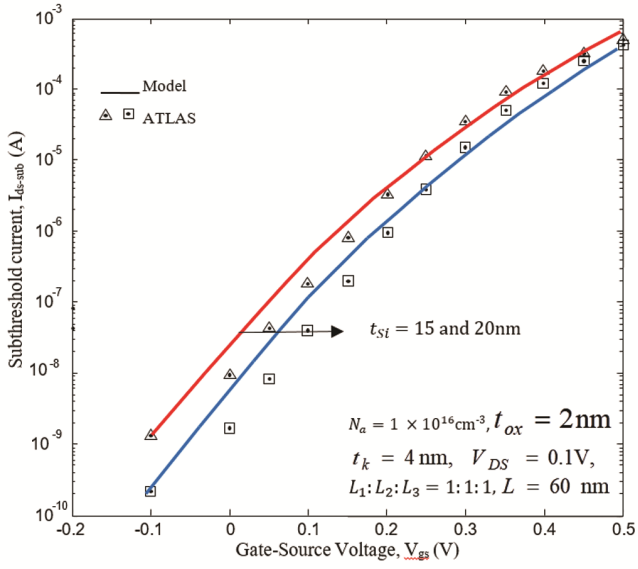

Fig. 4 — Variation in subthreshold current (I_s, in A) with gate-source voltage (V_{gs}, in V) for different values of silicon film thicknesses (t_{si})

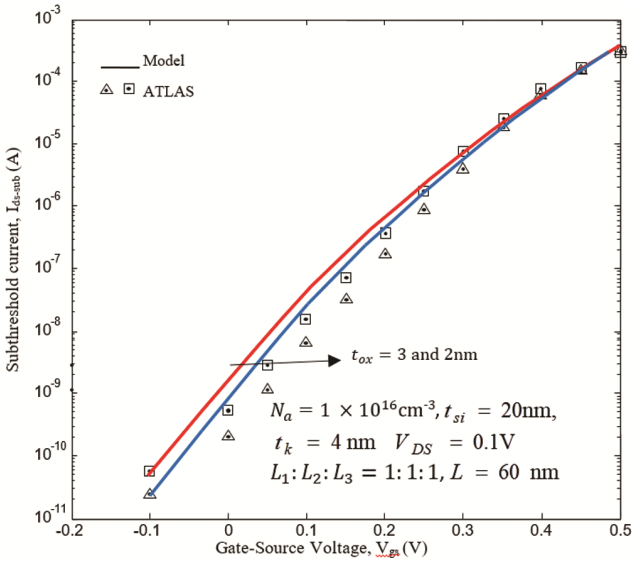

Fig. 5 — Variation in subthreshold current (I_s, in A) with gate-source voltage (V_{gs}, in V) for different values of gate-oxide thicknesses (t_{ox})

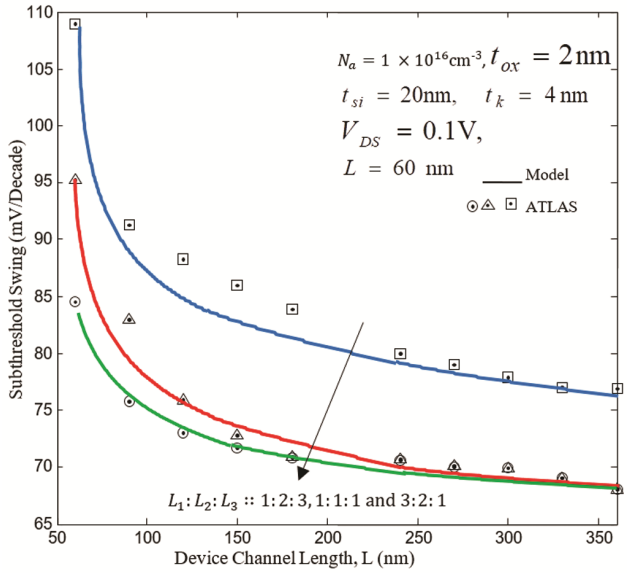

Fig. 6 — Variation in subthreshold swing (S, in mV/Decade) with channel length (L, in nm) for different ratios of L_1, L_2, and L_3

subthreshold swing. Whereas, for the case of $L_1: L_2: L_3 :: 3: 2: 1$, the maximum subthreshold swing achieved due to the lower value of subthreshold slope.

Furthermore, the variation in the subthreshold swing (S) at different device channel lengths (L) for different values silicon channel thicknesses (t_{Si}) is depicted in Fig. 7. It can be seen that the subthreshold swing changes rapidly below the device channel length below 150 nm. It occurs mainly due to the presence of short-channel effects. Whereas, if both the channel thickness is increased and channel length is decreased simultaneously, the switching property of device also changes drastically because of the increased short-channel effects.

Figure 8 shows the variation in subthreshold swing (S) at different device channel lengths (L) for different values oxide thicknesses (t_{ox}). It shows that to achieve the higher value of subthreshold swing; a thick gate oxide layer is required. In comparison to devices with the thick gate oxide and short channel length, it may be inferred that the TMGS-DG MOSFETs having with thinner gate oxide achieve the longer channel behavior.

The improved subthreshold-swing performance of the TMGS-DG MOSFET is primarily attributed to enhanced gate-to-channel electrostatic coupling. The symmetrical double-gate configuration provides simultaneous control of the channel from both surfaces, while the different work functions of the three gate segments establish a graded longitudinal potential profile. This arrangement increases control of the minimum channel potential by the gate voltage and reduces drain-induced modulation of the source-channel barrier.

Consequently, the device exhibits reduced short-channel effects and improved subthreshold swing. The use of thinner silicon and dielectric layers further enhances electrostatic gate control by reducing the characteristic scaling length.

4.1 Inverter Circuit from the TMGS-DG MOSFET

The circuit application of TMGS-DG MOSFET is studied by designing Inverter circuit. The RF application of the circuit can be seen by designing VCO circuit.

4.2 Circuit Simulation Methodology

The circuit-level performance of the proposed TMGS-DG MOSFET was evaluated using the calibrated device characteristics obtained from TCAD simulations. The CMOS inverter was constructed using complementary TMGS-DG nMOS and pMOS devices. The supply voltage was maintained at the selected operating voltage V_{DD}, while the input voltage was swept from 0 to V_{DD} to obtain the voltage-transfer characteristic (VTC). The device dimensions, including channel length, silicon thickness, oxide/high-k dielectric thickness, and gate-segment lengths, were kept consistent with the optimized device structure used in the device-level simulations.

Figure 9 depicts the schematic diagram of the suggested TMGS-DG PMOS based inverter, which employs a TMGS-DG PMOS as the pull-up device

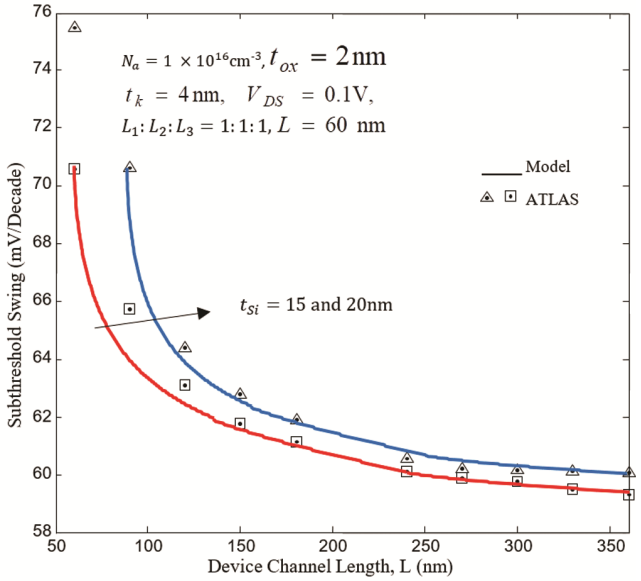

Fig. 7 — Variation in subthreshold swing (S, in mV/Decade) with channel length (L, in nm) for different silicon film thicknesses (t_{si})

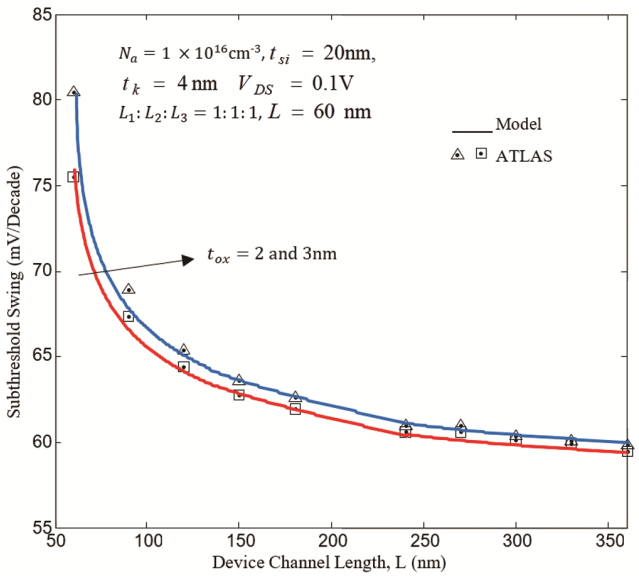

Fig. 8 — Variation in subthreshold swing (S, in mV/Decade) with channel length (L, in nm) for different gate oxide thicknesses (t_{ox})

and a TMGS-DG NMOS as the pull-down device. The output node and VDD are connected to the TMGS-DG PMOS, and the output node and ground are connected to the TMGS-DG NMOS. The conduction states of the TMGS-DG PMOS and TMGS-DG NMOS are controlled by simultaneously applying the input voltage to both gate of the devices. The TMGS-DG PMOS activates when the input is low, pulling the output to high while the TMGS-DG NMOS stays off. In contrast, the TMGS-DG PMOS switches OFF and the TMGS-DG NMOS turns ON and pulls the output to ground when the input is high. By ensuring appropriate inverter operation, this complementary switching produces full-swing output characteristics. Low-voltage operation and improved switching performance are made possible by the use of TMGS-DG MOSFETs, which increase tunneling efficiency at the junctions.

The Voltage Transfer Characteristic (VTC) of the TMGS-DG MOSFET inverter is shown in Fig. 10. A significant voltage gain in the transition region is indicated by the curve's abrupt change from high to low output near the switching threshold. Because the TMGS-DG PMOS is strongly ON and the TMGS-DG NMOS is OFF, the output stays near VDD at low input voltages. The inverter exhibits efficient switching behavior as the output rapidly changes as the input approaches the threshold region. After this, the output decreases to almost zero at higher input voltages because the TMGS-DG PMOS turns off while the TMGS-DG NMOS conducts strongly.

The TMGS-DG MOSFET's improved tunneling mechanism and high ON-current, which guarantee better noise margins and increased digital logic reliability, are reflected in the steepness of the VTC curve. The dynamic switching behavior of the TMGS-DG MOSFET inverter is shown by its transient response in Fig. 11. The inverter's switching operation is confirmed by the clean, sharp transitions seen in the input waveform (shown in red) and the output wave (shown in black). The output swing from 0 to 1V without distortion shows that the inverter circuit has strong drive capability and good stability. The propagation delay was extracted from the transient response using the conventional 50 % voltage criterion. The low-to-high and high-to-low propagation delays were determined from the time difference between the 50 % transition point of the input signal and the corresponding 50 % transition point of the output signal.

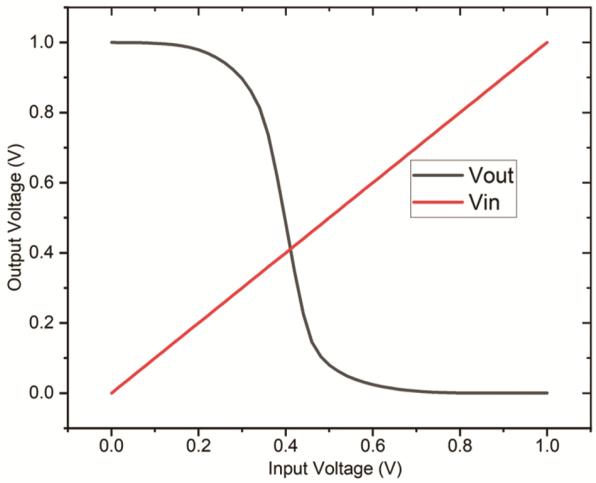

Fig. 10 — VTC curve of a TMGS-DG MOSFET based Inverter Circuit

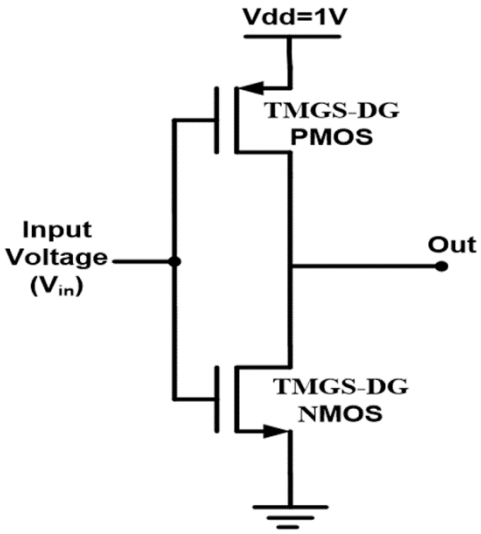

Fig. 9 — Schematic of a TMGS-DG MOS based Inverter Circuit

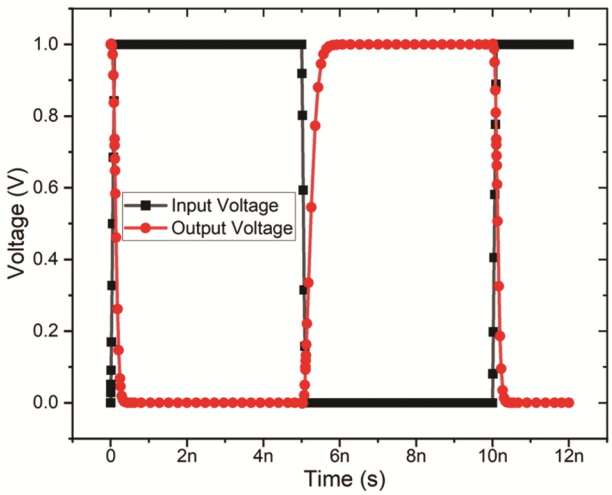

Fig. 11 — Transient curve of a TMGS-DG MOSFET based Inverter Circuit

$$t_{pLH} = t_{out,50\%}^{LH} - t_{in,50\%}^{LH}$$
$$t_{pHL} = t_{out,50\%}^{HL} - t_{in,50\%}^{HL}$$

The average propagation delay was calculated as;

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

The TMGS-DG MOSFET inverter achieves fast switching thanks to enhanced BTBT-induced current drive and decreased capacitance, as confirmed by the measured propagation delay from transient signal of 198 ps.

4.3 Ring Oscillator from the Proposed TMGS-DG MOSFET

Figure 12 shows the schematic of a three-inverter based ring oscillator that is built with three cascaded inverter stages connected in a closed loop. With an odd number of stages, the total phase shift is 540°, meeting the Barkhausen criterion for sustained oscillation. Each inverter in the chain adds a phase shift of 180°.

A self-sustaining feedback loop is created by feeding the output of the third inverter back into the input of the first inverter. The ring oscillator only needs a slight initialization disturbance to start oscillating because of the TMGS-DG MOSFET-based inverters ultralow leakage and sharp switching characteristics. The TMGS-DG MOSFET's suitability for low-power, high-efficiency oscillator circuits are demonstrated by this architecture, which allows the generation of a periodic output signal without the need for an external clock source. For the ring oscillator, an odd number of CMOS inverter stages was connected in cascade, with the output of the final stage fed back to the input of the first stage. Transient simulation was performed after allowing sufficient initial settling time for the oscillation to reach a stable periodic waveform. The oscillation frequency was extracted from the steady-state output waveform using the measured period T_{osc}.

$$f_{osc} \approx \frac{1}{T_{osc}}$$

For an N-stage ring oscillator, the oscillation frequency can also be approximately related to the inverter propagation delay by;

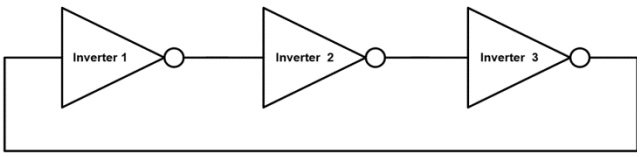

Fig. 12 — Schematic of a 3-inverter based ring oscillator

$$f_{osc} \approx \frac{1}{2Nt_p}$$

The reported oscillation frequency of approximately 445 MHz and propagation delay of approximately 198 ps were obtained from the steady-state transient waveforms. The transient output waveform of the proposed TMGS-DG MOSFET - based three-stage ring oscillator is shown in Fig. 13. The clean and stable output oscillation pattern with sharp rising and falling transitions confirms strong switching behavior and adequate drive strength of each inverter stage. The oscillation frequency obtained to be 445 MHz indicating that the TMGS-DG MOSFET devices conforming its high-speed operation. The performance of the TMGS-DG ring oscillator can be further optimized through simultaneous consideration of propagation delay, oscillation frequency, power consumption, power-delay product, and the number of inverter stages. Since $f_{osc} \approx 1/(2Nt_p)$, reducing the inverter propagation delay and optimizing the number of stages can increase the oscillation frequency. However, reducing the number of stages increases frequency at the expense of available phase stages, while increasing the number of stages generally increases power consumption and reduces oscillation frequency.

Dynamic power can be reduced by optimizing V_{DD}, transistor dimensions, and parasitic capacitance. The power-delay product provides a useful combined metric for evaluating the energy efficiency of the proposed device. These parameters provide additional design degrees of freedom for optimizing TMGS-DG-

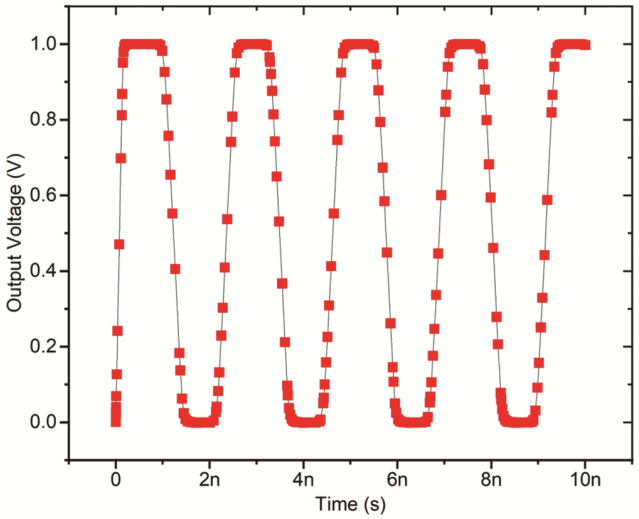

Fig. 13 — Transient response of a TMGS-DG MOSFET based ring oscillator

based ring oscillators for low-power and high-speed applications. The nearly rail-to-rail swing observed in the waveform highlights the effective noise margins and proper logic-level restoration at each inverter stage. The consistent and periodic nature of the signal verifies that the circuit maintains reliable oscillation with minimal distortion making it suitable for ultra-low-power clock-generation and signal-processing applications.

5 Conclusion

In summary, this study presents a comprehensive 2D analytical model for subthreshold current and swing in short-channel triple-material symmetrical gate-stack double-gate (TMGS-DG) MOSFETs, demonstrating superior performance when control gate length exceeds screen gate lengths through rigorous analysis of gate stacks and structural parameters. Optimized configurations achieve exceptional subthreshold swing of 65 mV/decade at 120 nm channel length with L_1:L_2:L_3 = 1:2:3 ratios—25 % better than uniform gates while reducing off-state leakage by 50% to 10^{-11} A (V_{gs}=0 V) and DIBL to under 40 mV/V, validated precisely against Silvaco ATLAS simulations across varied drain biases (0.1–0.5 V), silicon thicknesses (15–20 nm), oxide layers (2–3 nm), and high-k stacks. Circuit implementations further highlight promises with TMGS-DG inverters delivering 30 voltage gain, 198 ps delay, and full 0–1 V swing, alongside 445 MHz triple-stage ring oscillators featuring sharp transitions—outperforming prior DMG/TMDG designs by 15–20 % in speed and efficiency for ultra-low-power digital/RF applications.

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