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# Active Inductor-based Multistage DCO Design for Low Power VLSI Applications

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This paper investigates simulation-based analysis of 3-stage, 5-stage, and 7-stage digitally controlled oscillator (DCO) architectures implemented in 90 nm CMOS technology using the Cadence Virtuoso tool at a supply voltage of 1 V. The proposed DCO architectures are realised by cascading alternate delay stages in a closed-loop configuration to form a ring oscillator, where the output is fed back to the input to sustain oscillation. The delay stages comprise a CMOS inverter and a NAND gate–based inverter delay stage, combined with a PMOS switching network, MOS varactors and active inductors to achieve wide frequency tuning, high resolution, and low power operation. The results are analysed with varying control bits from 000 to 110 and voltage from 0.5 V to 1.0 V at different transistor widths (W = 1 µm, 1.5 µm, and 2 µm). For the 3-stage DCO, the oscillation frequency varies from 4.018 GHz to 0.517 GHz at W = 1 µm, 2.945 GHz to 1.822 GHz at W = 1.5 µm, and 2.309 GHz to 1.557 GHz at W = 2 µm, as the digital control bits are swept from 000 to 110, while power consumption decreases from 451.8 mW to 404.7 mW. Similarly, the 5-stage DCO exhibits a frequency tuning range of 1.832 GHz to 1.120 GHz at W = 1 µm, 1.405 GHz to 0.825 GHz at W = 1.5 µm, and 1.110 GHz to 0.655 GHz at W = 2 µm, while power consumption ranges from 451.6 mW to 404.3 mW. For the 7-stage DCO, the frequency tuning range is 1.188 GHz to 0.761 GHz at W = 1 µm, 0.873 GHz to 0.564 GHz at W = 1.5 µm, and 0.693 GHz to 0.448 GHz at W = 2 µm, with power consumption again decreasing from 451.6 mW to 404.3 mW. Similarly, the performance of the proposed DCO architectures is evaluated over a supply voltage range from 0.5 V to 1.0 V. The results determine that the DCO attains a wide frequency tuning range, high tuning resolution, and low power consumption through the combined operation of digitally controlled PMOS switching networks, voltage-controlled MOS varactors, and active inductors.

**Keywords:** DCO, Active inductor, CMOS-Inverter, Delay stage, MOS varactor, NAND gate

## 1 Introduction

In advanced electronic and communication systems, frequency synthesis plays an essential role in meeting the requirements for stable, accurate signal generation. There are various frequency-generating circuits; however, DCO is a key component among them. This is due to its various characteristics, such as scalability, compatibility with digital design, and the ability to achieve fine frequency resolution in CMOS technology[1-5]. A DCO is an oscillator in which the oscillation frequency of the output is regulated with the help of digital input signals, by removing the requirement for continuous analogue control voltages used in voltage-controlled oscillators (VCOs). This type of digital approach improves noise immunity, area consumption, linearity and design flexibility, making DCOs suitable for low-power communication systems and integration into System-on-Chip (SoC)[6-10]. Several applications of DCOs exist, like in Phase-Locked Loops (PLLs), clock generation circuits for wireless transceivers, frequency synthesisers, microprocessors and high-speed digital systems with the continuous scaling of CMOS technology. In digital signal processing circuits, the use of DCO enabled enhanced integration through fully digital implementation[11-15]. Digitally controlled oscillators have many advantages as compared to analogue controlled oscillators, like power consumption, area minimisation, phase noise, frequency tuning, etc. DCOs are used to improve key performance characteristics through various design topologies, such as LC-tank-based architectures, ring-oscillator-based structures, and hybrid configurations[16-20]. Furthermore, the integration of active-inductor and varactor-based techniques allows better control over power consumption, enhances frequency tuning capability, and contributes to the overall performance optimisation of the designed circuit[21-25].

There are two types of inductors commonly used in electronic circuits: passive and active. Passive inductors offer low noise and structural simplicity; however, they require a large silicon area and show poor quality factor

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(Q) in CMOS technologies. In contrast, active inductors offer significant advantages, including reduced area consumption, tunable inductance, and a higher effective Q, making them more suitable for integration in modern CMOS-based VLSI systems[26-27]. In this paper, a DCO circuit is designed using active inductor-based techniques, which are more advantageous than passive inductors. Techniques based on Active inductors are advantageous in DCO and CMOS-based VLSI applications because they use transistor-based circuits to mitigate the disadvantages of passive inductors. The oscillators architecture, designed with the integration of active inductors provides improved phase noise performance, reduced power consumption, enhanced frequency tunability and reduced silicon area consumption, making them highly suitable for modern high-performance integrated circuits. This paper also incorporates varactor-based tuning techniques. A varactor functions as a voltage-controlled capacitor whose capacitance varies with the applied bias voltage. These varactors are used for the fine and continuous tuning of an oscillator's output frequency, making them highly effective for achieving precise frequency control in DCO designs[28-29]. In CMOS-based VLSI circuits, Varactor-based tuning techniques are implemented using MOS devices, which allows the capacitance of the capacitor to vary with the applied bias voltage. This voltage-dependent capacitance enables precise, continuous control of the oscillator's output frequency without significantly increasing power consumption.

## 2 Materials and Methods

### 2.1 Architecture of the Proposed DCO Based on Delay Stages

The proposed DCO is implemented using two types of delay stages: a CMOS inverter based active inductor stage and a NAND-gate-based active inductor stage. The operation of both delay stages is controlled through a PMOS switching network, while a MOS varactor used in conjunction with the active inductor provides high resolution and fine-tuning capability. This combination permits effective regulation of the oscillation frequency and improves overall performance of the DCO architecture. In this work, 3-stage, 5-stage, and 7-stage DCO architectures are designed and simulated using 90 nm CMOS technology in the Cadence Virtuoso tool. The DCO architecture comprises of multiple such delay stages connected in a ring topology form in 3-stage, 5-stage, and 7-stage. An odd number of delay stages are used in the cascaded form and working on the basis of a feedback mechanism. The proposed ring oscillator follows the Barkhausen criterion, which states that when phase conditions and loop gain are fulfilled sustained oscillations occur. The oscillation frequency is expressed by Eq. (1). Where N denotes the number of stages and $t_{delay}$ delay per stage.

$$F_{osc} = \frac{1}{2N.\ t_{delay}} \quad \ldots (1)$$

The proposed DCO architecture incorporates multiple delay stages. Figure 1 illustrates two such stages the first is a CMOS-based inverter with an active-inductor DCO structure, and the second is a NAND-based inverter with an active-inductor DCO schematic. Both delay stages employ MOS varactors

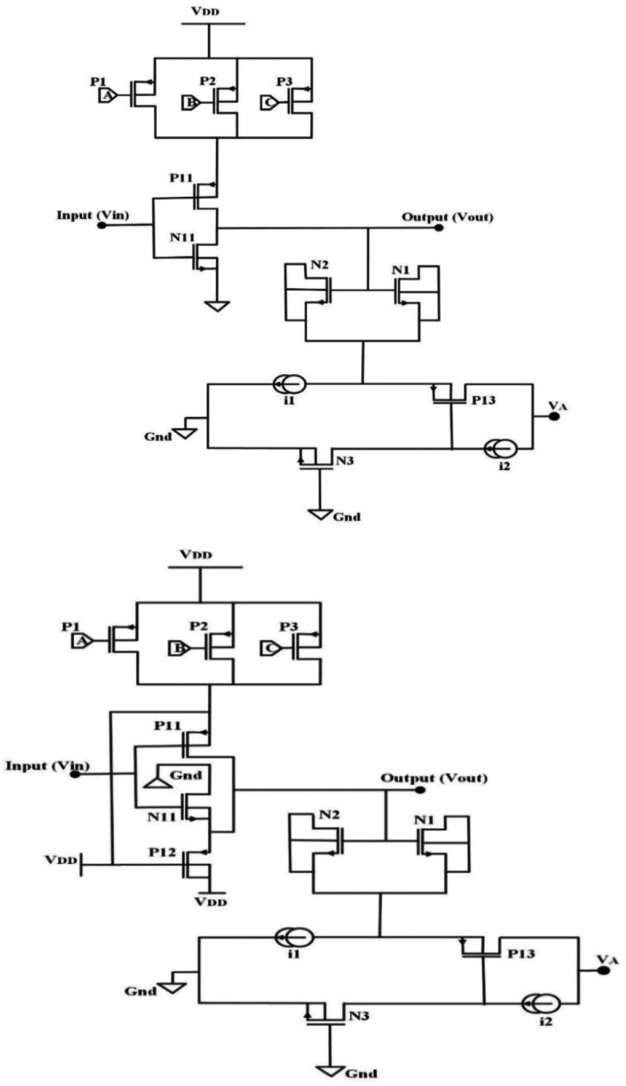


Fig. 1 — (a) First delay stage with CMOS inverter-based active inductor DCO; and (b) Second delay stage with NAND based inverter active inductor DCO

in combination with active inductors to achieve high resolution and improved tunability. In this design, an NMOS varactor is implemented by shorting the source, drain, and bulk terminals to form a single node, while the gate terminal behaves as the second node. These two terminals function like capacitor plates, and the resulting capacitance varies in a non-monotonic manner with respect to the applied bias, permitting fine frequency tuning within the oscillator.

The working principle of the CMOS inverter–based active inductor shown in Fig. 1 (a) delay stage depends on the collective operation of the PMOS switching network, NMOS MOS varactors, and the active inductor. Together, these elements provide high resolution, lower power consumption and wide tuning range. The transistors P11 and N11 form the pull-up and pull-down networks of the CMOS inverter, respectively. When the input signal Vin toggles, the inverter output Vout is produced through the charging and discharging action of these transistors. The oscillation period of the DCO is defined by the propagation delay presented by this inverter stage.

The PMOS switching network provides coarse tuning to the circuit through the transistors P1, P2, and P3. The PMOS transistors are binary weighted in the form of $2^0, 2^1, 2^2, ...$, and their operation is regulated by the corresponding digital control bits. This binary-weighted switching network provides coarse frequency tuning by changing the effective load capacitance of the delay stage. When a PMOS switch is turned ON, it increases the effective load at the output node, resulting in higher delay and, consequently, a lower oscillation frequency, as expressed in Eq. (1). Conversely, when the switch is turned OFF, the load decreases, reducing the delay and thereby increasing the oscillation frequency. Hence, the digitally controlled coarse-tuning network permits a wide tuning range in the proposed DCO architecture. The MOS varactor transistors N1 and N2 permits high-resolution tuning of the oscillation frequency. The lower portion of the circuit, comprising transistors P13 and N3 along with the current-dependent sources $i_1$and $i_2$, works as an active inductor. This active inductor arrangement achieves a high quality factor while significantly minimising silicon area compared to passive inductors. Furthermore, i1 and i2 current-dependent sources provide improved frequency stability and reduced power consumption to the proposed DCO architecture.

The second delay stage is a NAND-based inverter active-inductor DCO that comprises of PMOS switching network, MOS varactors, and an active-inductor section. The PMOS switching network allows coarse frequency tuning and offers a wide tuning range, while the MOS varactors offer fine frequency tuning with high resolution. In conjunction with the active inductor, this configuration improves frequency tunability while maintaining low power consumption.

Table 1 shows the width-to-length (W/L) ratios of the transistors used in the proposed 3-stage,5-stage and 7-stage DCO architectures. These dimensions are specified according to the transistors naming given in the first and second delay stages illustrated in Fig. 1 (a) and (b), respectively.

The block diagrams of the proposed 3-stage, 5-stage, and 7-stage DCO architectures are presented in Fig. 2. Where the delay elements are implemented using an odd number of inverter stages to confirm sustained oscillation.

## 3 Results and Discussion

The proposed three-stage DCO is designed by cascading three alternating delay stages in a closed-loop arrangement to produce sustained oscillations. The architecture consists of a combination of CMOS inverter–based and NAND gate–based delay stages, as shown in Fig. 3. Each stage integrates a PMOS switching network, MOS varactors, and an active-inductor block, which collectively control the oscillation frequency while enabling low-power operation and high tuning resolution. Two types of

Table 1 — shows the width-to-length (W/L) ratios of the transistors used in the 3-stage, 5-stage, and 7-stage DCO architectures

| Delay stages | MOSFET | Width | Length | W/L |
|---|---|---|---|---|
| PMOS switching network | P1 | 120nm | 100nm | 1.2 |
| | P2 | 240nm | 100nm | 2.4 |
| | P3 | 480nm | 100nm | 4.8 |
| CMOS inverter | P11 | 250nm | 100nm | 2.5 |
| | N11 | 120nm | 100nm | 1.2 |
| NAND-gate based inverter | P11 | 450nm | 100nm | 4.5 |
| | N11 | 180nm | 100nm | 1.8 |
| | P12 | 360nm | 100nm | 3.6 |
| MOS varactor | N1 | 1µm | 100nm | 10 |
| | N2 | 1µm | 100nm | 10 |
| Active inductor | P13 | 240nm | 100nm | 2.4 |
| | N3 | 120nm | 100nm | 1.2 |
| | i1 | 200µA | 100nm | 50 |
| | i2 | 200µA | 100nm | 50 |

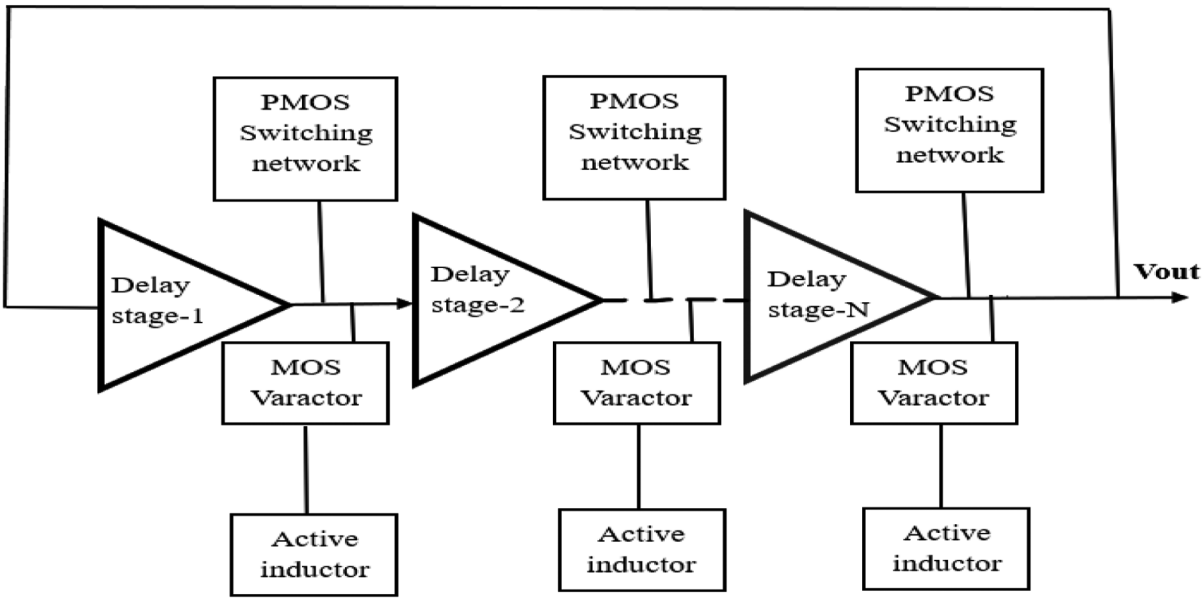


Fig. 2 — Block diagram of 3-stage, 5-stage and 7-stage DCO architecture

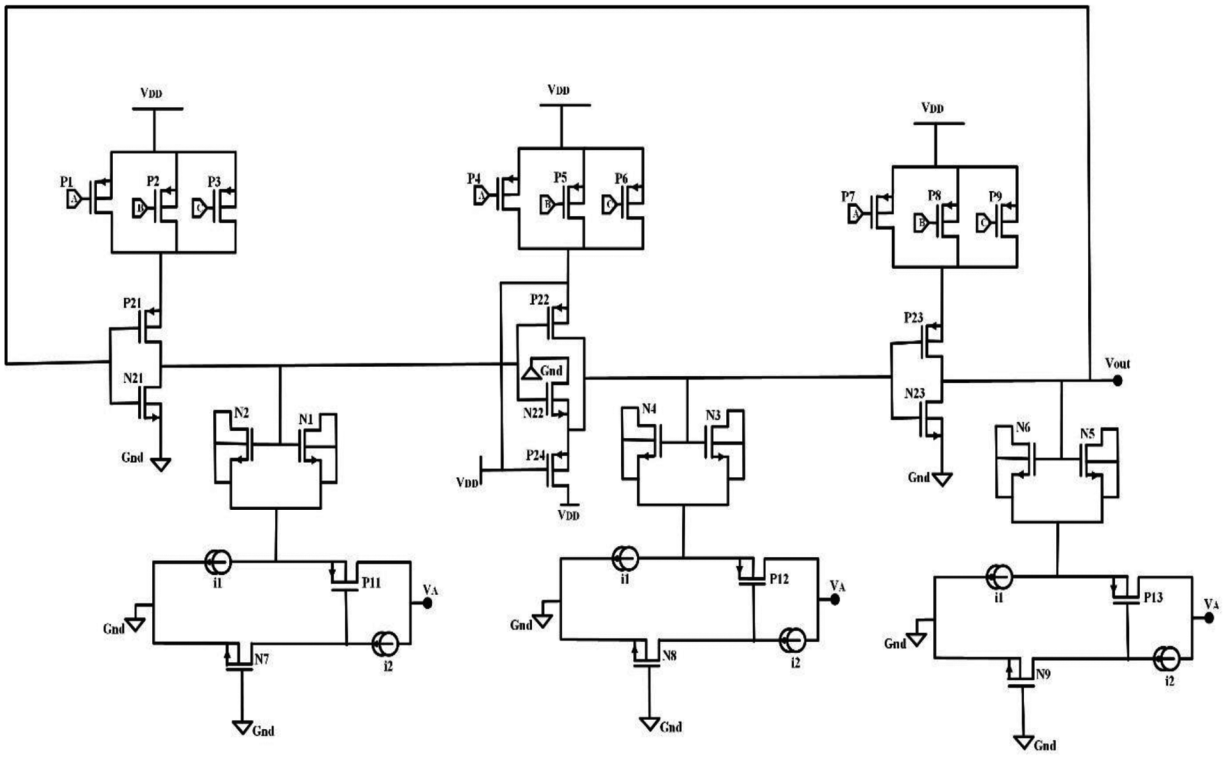


Fig. 3 — 3-Stage schematic of active inductor-based DCO

frequency tuning are working in the proposed design: coarse tuning and fine tuning.

The working principle of the proposed 3-stage DCO is defined wth the combination of various delay stages. These delay stages consist of PMOS switching networks (P1–P3, P4–P6, and P7–P9) which are binary weighted in the form of ($2^0$, $2^1$, $2^2$,…….) and controlled with the help of digital control bits. This PMOS switching network permits coarse frequency tuning by regulating the

Table 2 — Variation of power and frequency with various control bits at different widths

| Control bits | W=1µm | | W=1.5µm | | W=2µm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) |
| 000 | 451.8 | 4.018 | 451.8 | 2.945 | 451.8 | 2.309 |
| 001 | 450.3 | 3.986 | 450.3 | 2.585 | 450.3 | 2.231 |
| 010 | 448.2 | 3.871 | 448.2 | 2.342 | 448.2 | 2.222 |
| 011 | 445.3 | 3.660 | 445.3 | 2.284 | 445.3 | 2.088 |
| 100 | 439.8 | 3.499 | 439.8 | 2.229 | 439.8 | 1.814 |
| 101 | 430.6 | 3.403 | 430.6 | 2.085 | 430.6 | 1.744 |
| 110 | 404.7 | 0.517 | 404.7 | 1.822 | 404.7 | 1.557 |

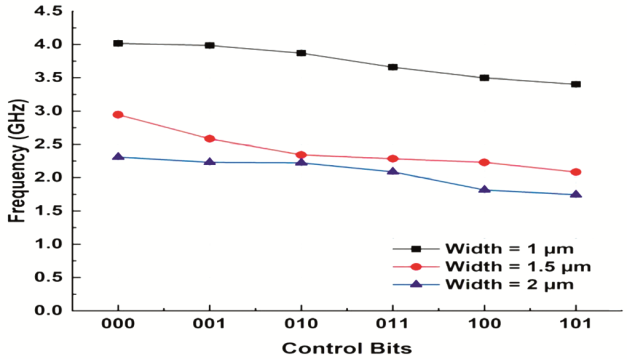


Fig. 4 — Variation of frequency vs control bits for 3-stage DCO

effective load and delay of each stage, thereby providing a wide tuning range for the proposed DCO. The total propagation delay of the three cascaded stages determines the DCO's oscillation period. The MOS varactors (N1–N2, N3–N4, and N5–N6) provide fine frequency tuning with high resolution. The capacitance of these varactors is controlled by the applied bias voltage, permitting specific adjustment of the oscillation frequency. These are connected at the output nodes of each stage. The lower section of each delay stage incorporates an active inductor realised using transistor pairs P11–N7, P12–N8, and P13–N9, together with current sources $i_1$and $i_2$. Compared to passive inductors, this active inductor occupies significantly less silicon area while providing a high effective quality factor. It improves frequency stability and tuning linearity and also reduces power consumption in the proposed DCO. With the combination of PMOS switching network, which uses coarse frequency tuning gives a wide frequency range, MOS varactors which provides fine frequency tuning gives high resolution and active inductors which provides high quality factor, the proposed 3-stage DCO achieves wide frequency tuning, high resolution, compact silicon area, and low power consumption, making it suitable for high-frequency and low-voltage CMOS VLSI applications.

Table 2 describes the variation of power consumption and oscillation frequency of the proposed 3-stage DCO for different digital control bits that vary from (000–110) and three transistor widths (W = 1 µm, 1.5 µm, and 2 µm).

The digital control bits are applied to the binary-weighted PMOS switching network, which uses coarse tuning to provide wide tuning of the oscillation frequency. As the control bits increase from 000 to 110, more PMOS switches are triggered, which enhances the effective load capacitance and resistance at the output of each delay stage. This results in a larger propagation delay, which, in turn, reduces the DCO's oscillation frequency. The oscillation frequency displays a monotonic decrement as the control bits increase from (000 to 110) for all transistor widths. For example, at W = 1 µm, the frequency decreases from 4.018 GHz to 0.517 GHz. A parallel decrease is observed for W = 1.5 µm and W = 2 µm, confirming the efficiency of the coarse-tuning mechanism. Table 2 also shows that the power consumption decreases gradually under the specified operating conditions, like at W = 1 µm, power reduces from 451.8 mW to 404.7 mW as the control bits increase, as shown in graph Fig. 4. This happens because lower oscillation frequencies reduce the switching activities in the delay stages, which leads to lower dynamic power dissipation. Furthermore, as the transistor width increases from 1 µm to 1.5 µm and 2 µm, the oscillation frequency decreases for a given control bit, while the power consumption remains nearly constant at a particular control bit. This behaviour occurs because wider transistor widths introduce higher parasitic capacitances, which increase the propagation delay of the delay stages and consequently reduce the oscillation frequency.

Table 3 — Variation of power and frequency with various control voltages at different widths

| Voltage ($V_{DD}$) | W=1μm | | W=1.5μm | | W=2μm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) |
| 0.5 | 217.4 | 0.373 | 217.4 | 0.352 | 217.4 | 0.238 |
| 0.6 | 267.3 | 0.933 | 267.3 | 1.009 | 267.3 | 0.748 |
| 0.7 | 315.1 | 1.911 | 315.1 | 1.694 | 315.1 | 1.136 |
| 0.8 | 361.2 | 2.498 | 361.2 | 2.202 | 361.2 | 1.719 |
| 1.0 | 451.8 | 4.018 | 451.8 | 2.945 | 451.8 | 2.309 |

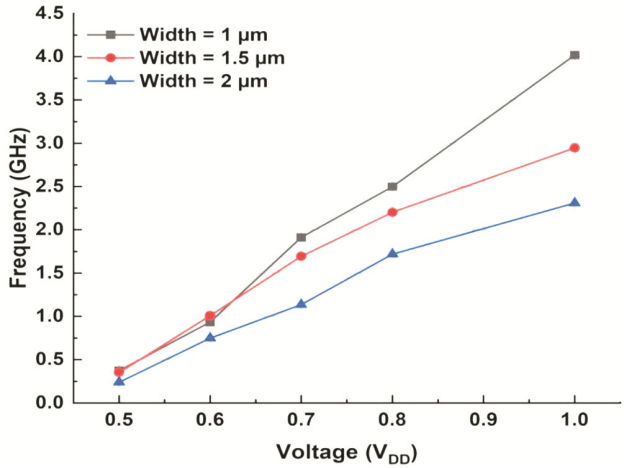


Fig. 5 — Variation of frequency vs voltage for 3-stage DCO

Table 3 demonstrates the variation in oscillation frequency and power consumption with changes in the supply voltage from 0.5 V to 1.0 V for three different transistor widths (W = 1 μm, 1.5 μm, and 2 μm).

As the supply voltage rises from 0.5 V to 1.0 V, both the power consumption and oscillation frequency increase for all transistor widths shown in Fig. 5. This behaviour is expected because a higher supply voltage increases the drive current of the transistors, permitting the inverter stages to charge and discharge the load capacitances more rapidly. Therefore, the propagation delay of each delay stage reduces, which leads to a higher oscillation frequency.

For instance, at W = 1 μm, power consumption rises from 217.4 mW to 451.8 mW, while the corresponding frequency rises from 0.373 GHz to 4.018 GHz. A parallel growing trend is detected for W = 1.5 μm and W = 2 μm. For a constant supply voltage, as the transistor widths increase (W = 1 μm, 1.5 μm, and 2 μm), the oscillation frequency decreases, while power consumption remains nearly constant. The value of Wider transistor widths introduces larger parasitic capacitances, which increases the delay of the inverter stages and thereby decreases the oscillation frequency. The output waveforms for a transistor width of 1 μm are presented in Fig. 6, while those for widths of 1.5 μm and 2 μm are shown in Figs. 7 and 8, respectively.

The proposed five-stage DCO is designed by cascading five alternating delay stages in a closed-loop arrangement to produce sustained oscillations. The architecture consists of a combination of CMOS inverter–based and NAND gate–based delay stages, shown in Fig. 7. The working of the 5-stage proposed DCO is the same as defined for the 3-stage DCO. Each stage comprises a PMOS switching network, MOS varactors, and an active-inductor block, which together regulate the oscillation frequency while enabling low-power operation and high tuning resolution. The five stage schematic of active inductor based DCO is shown in Fig. 9 which consists of five delay stages in alternate manner.

Table 4 presents the variation in power consumption and oscillation frequency of the proposed 5-stage DCO for different digital control bits (000–110) and three transistor widths (W = 1 μm, 1.5 μm, and 2 μm).

The 5-stage DCO shows the same results as the 3-stage DCO when control bits vary from (000 to 110) and transistor widths (W = 1 μm, 1.5 μm, and 2 μm) , power and frequency both decrease as control bits increase, as shown in Fig. 10.

Table 5 presents the effect of supply voltage variation, from 0.5 V to 1.0 V, on the power consumption and oscillation frequency of the proposed DCO for three different transistor widths (W = 1 μm, 1.5 μm, and 2 μm).

As the supply voltage increases from 0.5 V to 1.0 V, both the power consumption and oscillation frequency show the same results as 3-stage DCO as the increase for all transistor widths shown in the Fig. 11.

The output waveforms for a transistor width of 1 μm are presented in Fig. 12 , while those for widths of 1.5 μm and 2 μm are shown in Figs. 13 and 14, respectively.

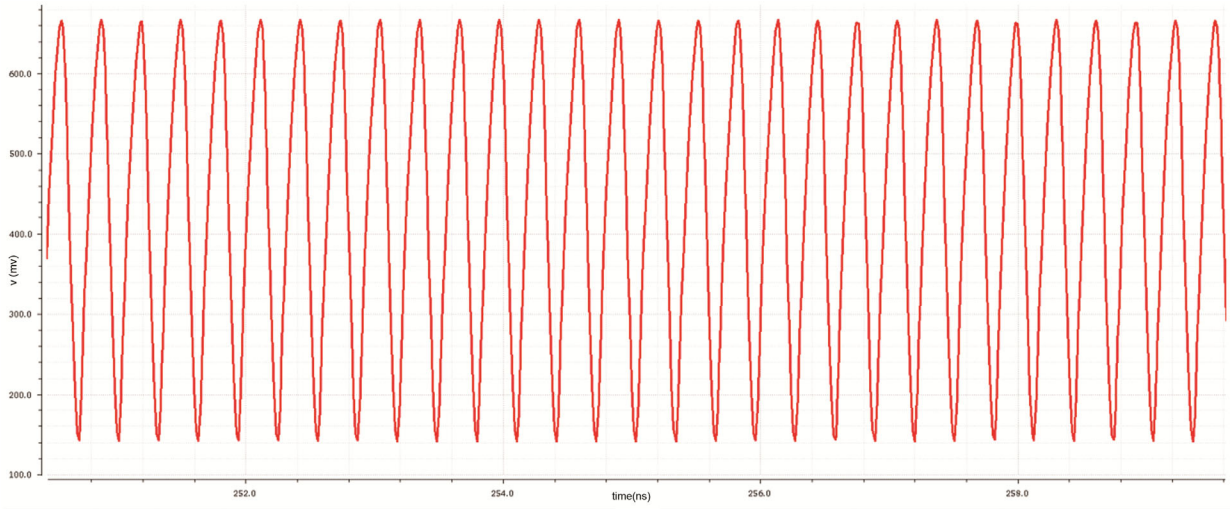


Fig. 6 — 3-Stage active inductor based DCO output for width 1000nm

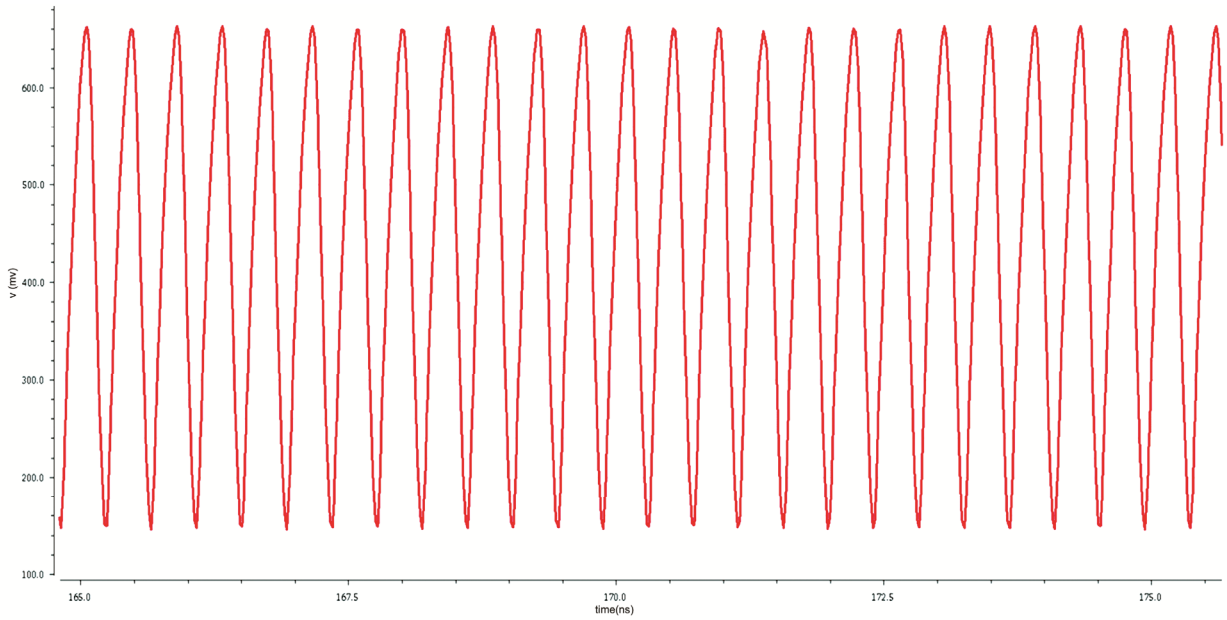


Fig. 7 — 3-Stage active inductor based DCO output for width 1500nm

The proposed seven-stage DCO is designed by cascading seven alternating delay stages in a closed-loop arrangement to produce sustained oscillations. The architecture consists of a combination of CMOS inverter–based and NAND gate–based delay stages, shown in Fig. 15. The working of the 7-stage proposed DCO is the same as defined for the 3-stage DCO. Each stage comprises a PMOS switching network, MOS varactors, and an active-inductor block, which together regulate the oscillation frequency while enabling low-power operation and high tuning resolution.

Table 6 presents the variation in power consumption and oscillation frequency of the proposed 7-stage DCO for different digital control bits (000–110) and three transistor widths (W = 1 µm, 1.5 µm, and 2 µm).

The 7-stage DCO shows the same results as the 3-stage DCO when control bits vary from (000 to 110) and transistor widths (W = 1 µm, 1.5 µm, and 2 µm), power and frequency both decrease as control bits increase, as shown in Fig. 16.

Table 7 summarizes the influence of supply voltage (VDD), ranging from 0.5 V to 1.0 V, on the power

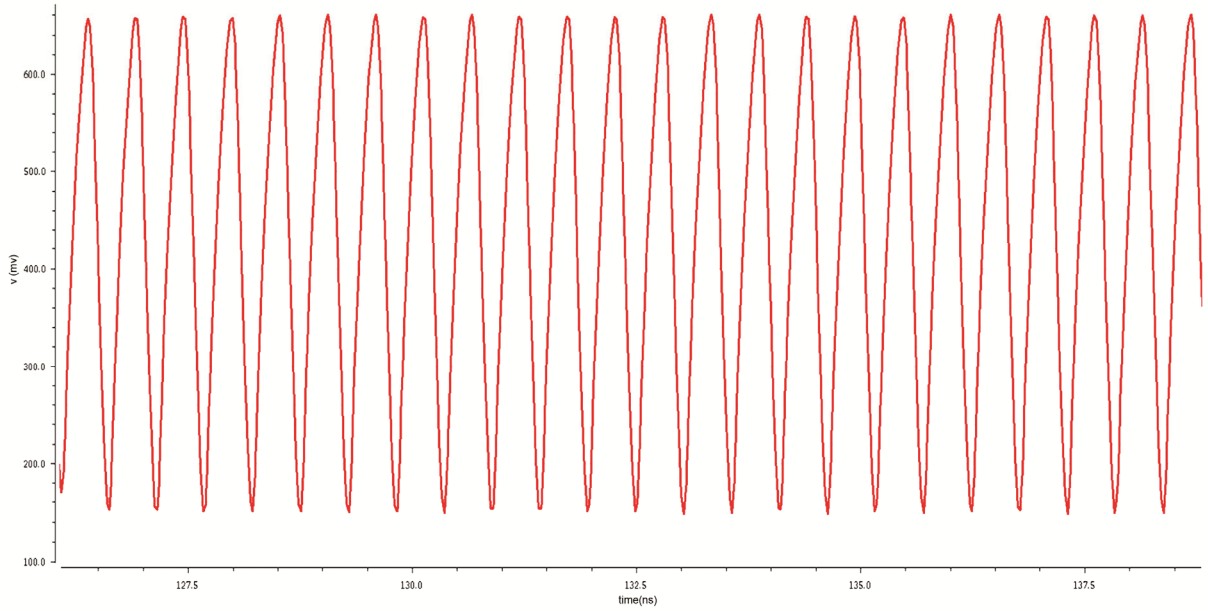


Fig. 8 — 3-Stage active inductor based DCO output for width 2000nm

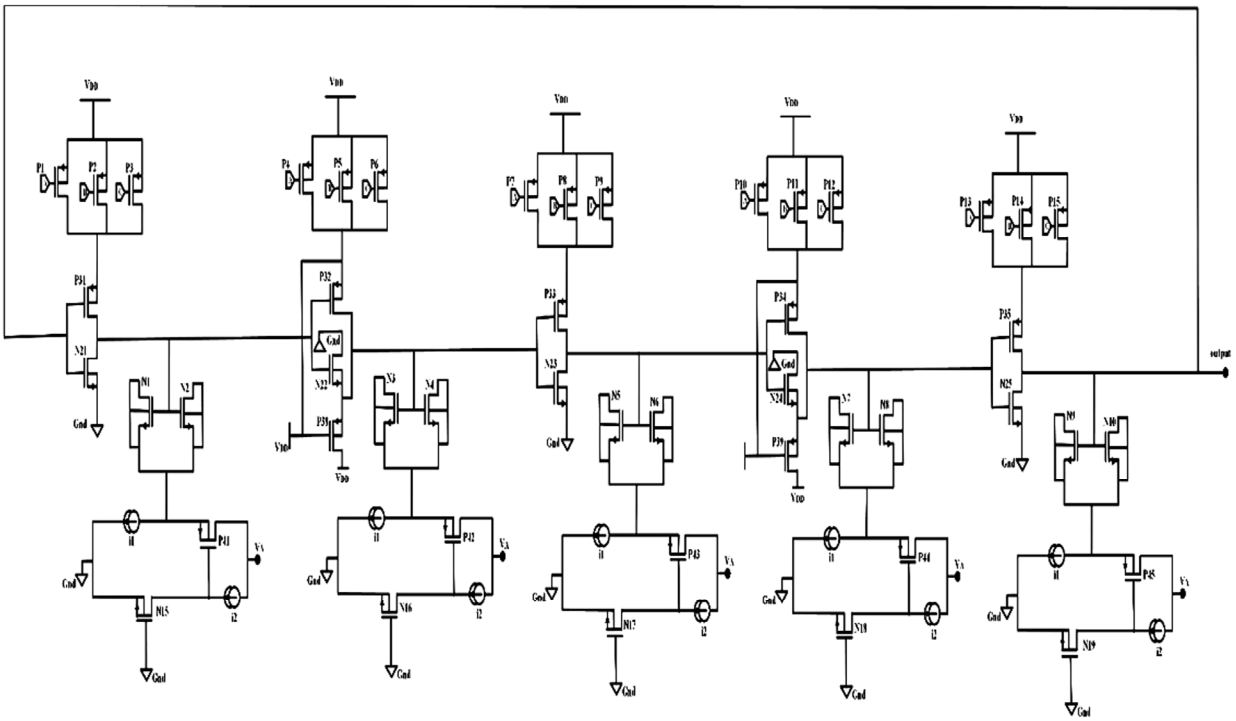


Fig. 9 — 5-Stage schematic of active inductor based DCO

consumption and oscillation frequency of the proposed 7-stage DCO at transistor widths of 1 µm, 1.5 µm, and 2 µm.

As the supply voltage increases from 0.5 V to 1.0 V, both the power consumption and oscillation frequency show the same results as 3-stage DCO as the increase for all transistor widths shown in Fig. 17.

The output waveforms for a transistor width of 1 µm are presented in Fig. 18, while those for widths of 1.5 µm and 2 µm are shown in Figs. 19 and 20, respectively.

Table 4 — Variation of power and frequency with various control bits at different widths

| Control bits | W=1µm | | W=1.5µm | | W=2µm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) |
| 000 | 451.6 | 1.832 | 451.6 | 1.405 | 451.6 | 1.110 |
| 001 | 450.2 | 1.672 | 450.2 | 1.228 | 450.2 | 1.058 |
| 010 | 448.0 | 1.636 | 448.0 | 1.208 | 448.0 | 0.996 |
| 011 | 445.0 | 1.601 | 445.0 | 1.182 | 445.0 | 0.937 |
| 100 | 439.5 | 1.535 | 439.5 | 1.134 | 439.5 | 0.902 |
| 101 | 430.1 | 1.424 | 430.1 | 1.103 | 430.1 | 0.834 |
| 110 | 404.3 | 1.120 | 404.3 | 0.825 | 404.3 | 0.655 |

Table 5 — Variation of power and frequency with various control voltages at different widths

| Voltage ($V_{DD}$) | W=1µm | | W=1.5µm | | W=2µm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (GHz) |
| 0.5 | 217.4 | 0.448 | 217.4 | 0.394 | 217.4 | 0.327 |
| 0.6 | 267.3 | 0.593 | 267.3 | 0.444 | 267.3 | 0.494 |
| 0.7 | 315.0 | 1.160 | 315.0 | 0.660 | 315.0 | 0.607 |
| 0.8 | 361.2 | 1.220 | 361.2 | 1.067 | 361.2 | 0.885 |
| 0.9 | 406.6 | 1.594 | 406.6 | 1.362 | 406.6 | 1.082 |
| 1.0 | 451.6 | 1.832 | 451.6 | 1.405 | 451.6 | 1.110 |

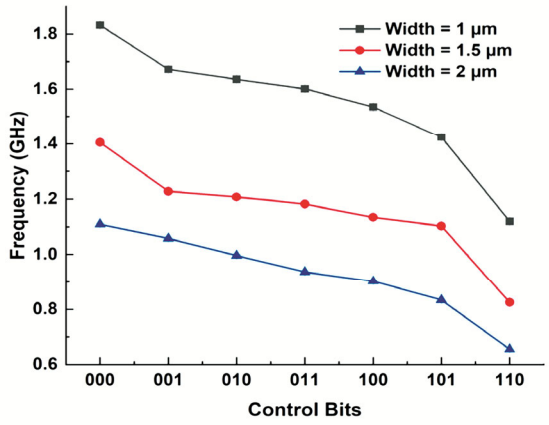


Fig. 10 — Variation of frequency vs control bits for 3-stage DCO

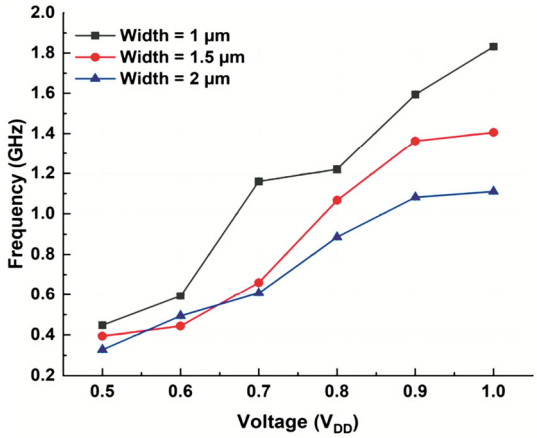


Fig. 11 — Variation of frequency of voltage

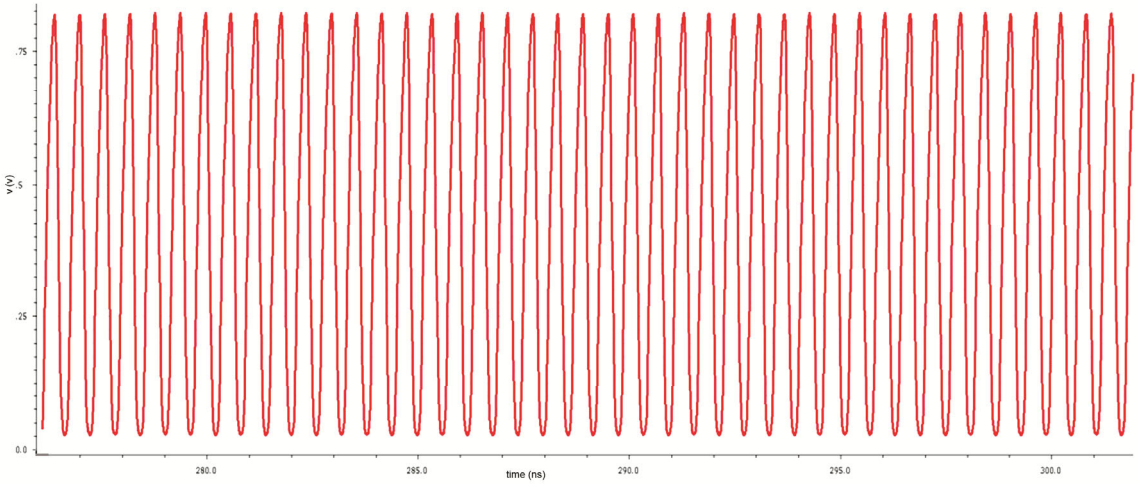


Fig. 12 — 5-Stage active inductor based DCO output for width 1000 nm

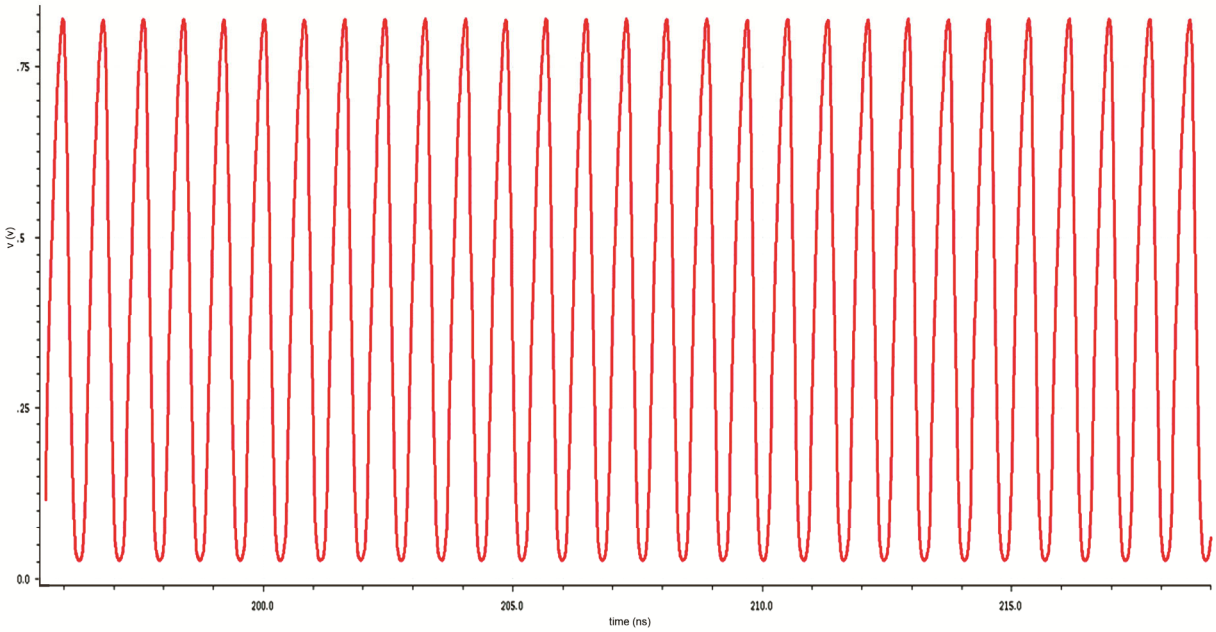


Fig. 13 — 5-Stage active inductor based DCO output for width 1500 nm

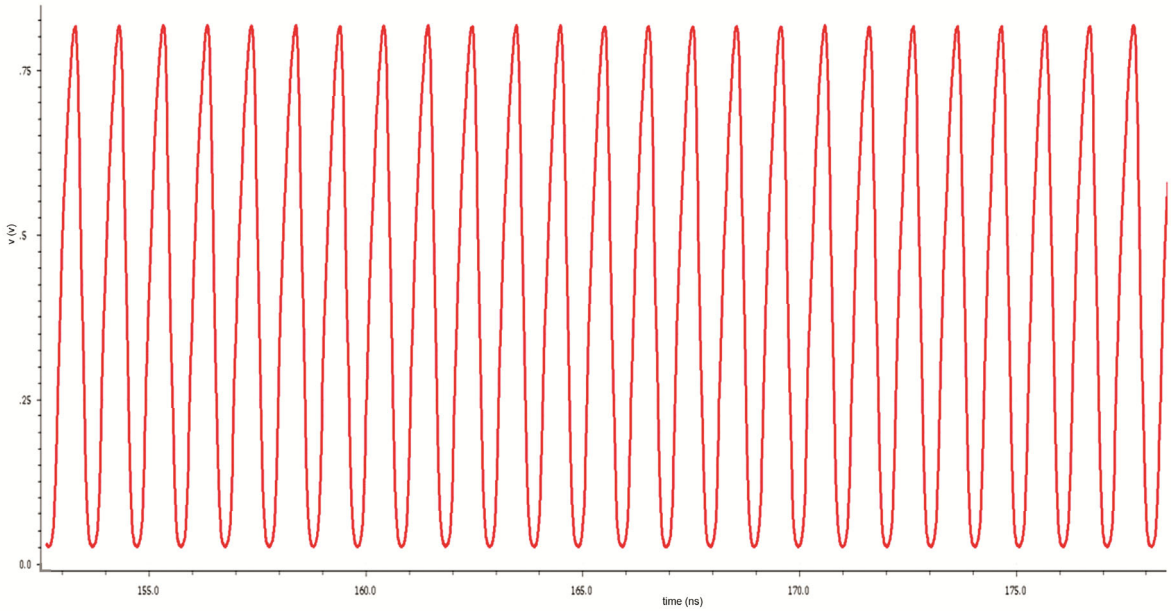


Fig. 14 — 5-Stage active inductor based DCO output for width 2000 nm

Table 6 — Variation of power and frequency with various control bits at different widths

| Control bits | W=1µm | | W=1.5µm | | W=2µm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (MHz) | Power (mW) | Frequency (MHz) |
| 000 | 451.6 | 1.188 | 451.6 | 873.9 | 451.6 | 693.2 |
| 001 | 450.2 | 1.171 | 450.2 | 865.3 | 450.2 | 685.4 |
| 010 | 448.0 | 1.152 | 448.0 | 859.1 | 448.0 | 674.3 |
| 011 | 445.0 | 1.123 | 445.0 | 829.7 | 445.0 | 659.0 |
| 100 | 439.5 | 1.071 | 439.5 | 793.2 | 439.5 | 629.8 |
| 101 | 430.1 | 0.989 | 430.1 | 732.0 | 430.1 | 581.5 |
| 110 | 404.3 | 0.761 | 404.3 | 564.1 | 404.3 | 448.3 |

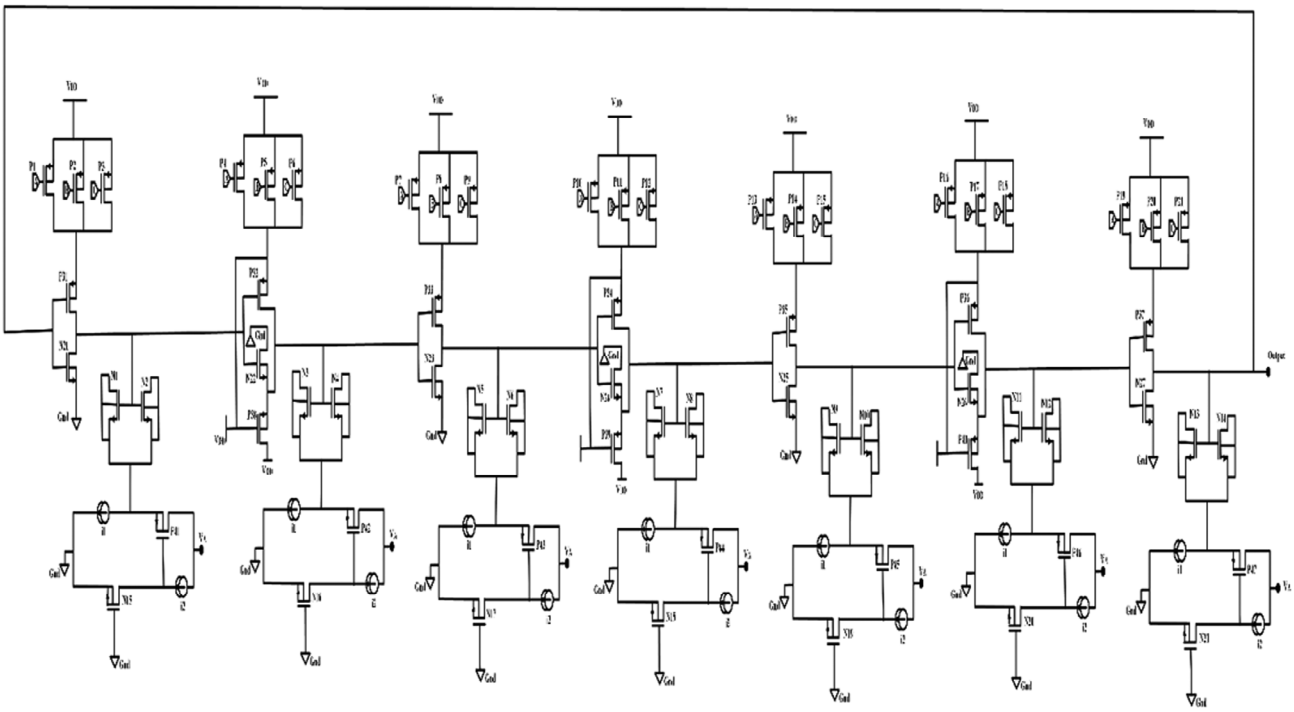

Fig. 15 — 7-Stage circuit of active inductor-based DCO

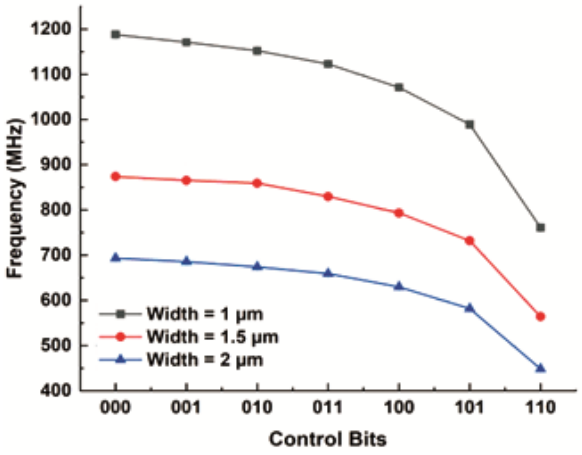


Fig. 16 — Variation of frequency vs control bits

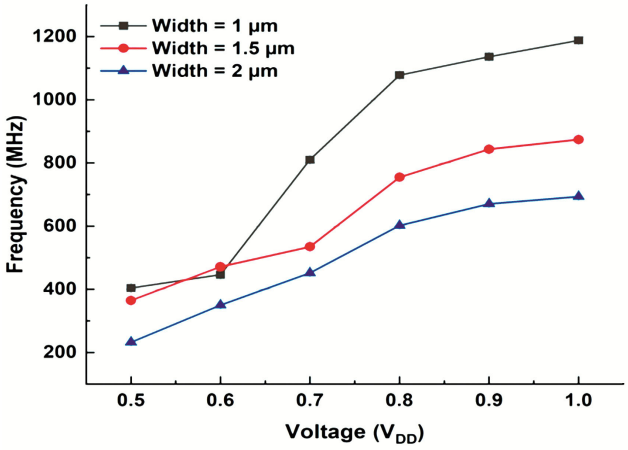


Fig. 17 — Variation of frequency vs voltage

Table 7 — Variation of power and frequency with various control voltages at different widths

| Voltage ($V_{DD}$) | W=1µm | | W=1.5µm | | W=2µm | |
|---|---|---|---|---|---|---|
| | Power (mW) | Frequency (GHz) | Power (mW) | Frequency (MHz) | Power (mW) | Frequency (MHz) |
| 0.5 | 217.4 | 0.404 | 217.4 | 364.5 | 217.4 | 232.4 |
| 0.6 | 267.3 | 0.446 | 267.3 | 471.6 | 267.3 | 349.5 |
| 0.7 | 315.0 | 0.810 | 315.0 | 534.5 | 315.0 | 451.6 |
| 0.8 | 361.2 | 1.078 | 361.2 | 754.5 | 361.2 | 601.7 |
| 0.9 | 406.6 | 1.136 | 406.6 | 843.2 | 406.6 | 670.0 |
| 1.0 | 451.6 | 1.188 | 451.6 | 873.9 | 451.6 | 693.2 |

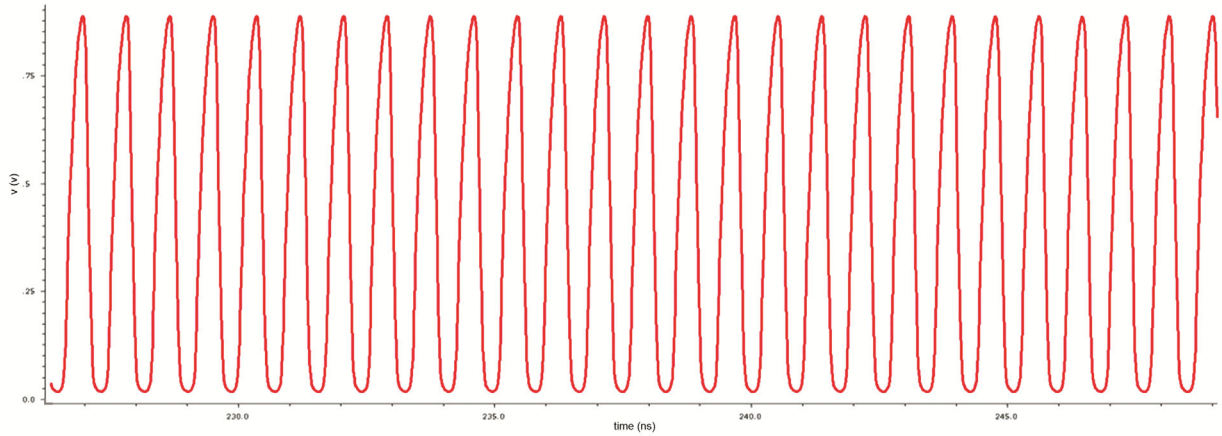


Fig. 18 — 7-Stage active inductor-based DCO output for width 1000 nm

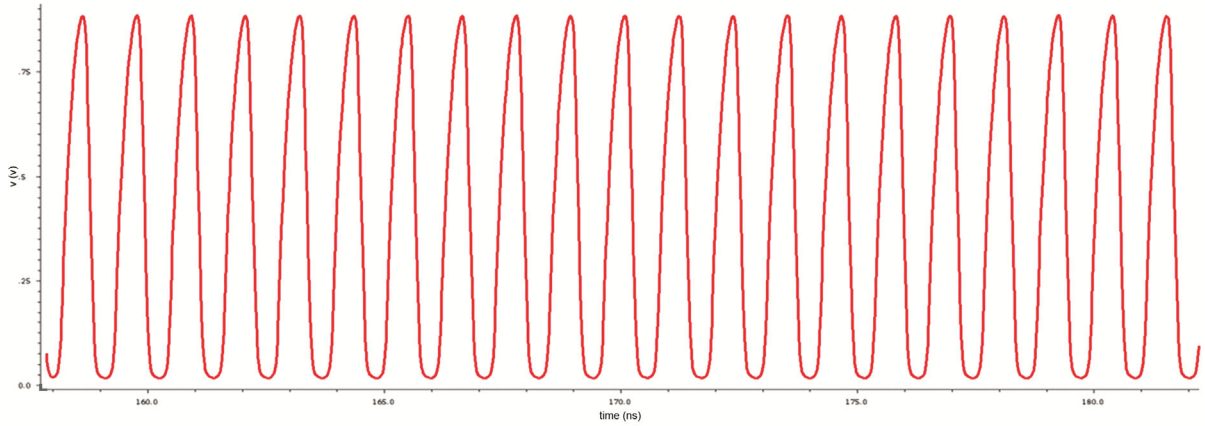


Fig. 19 — 7-Stage active inductor-based DCO output for a width 1500 nm

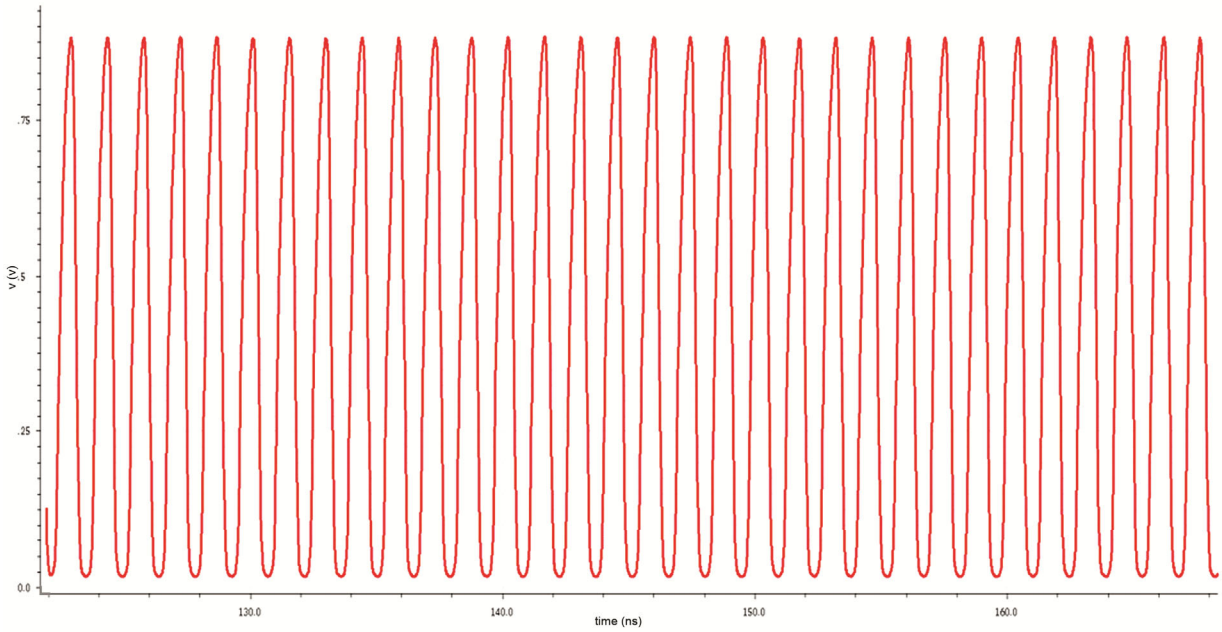


Fig. 20 — 7-Stage active inductor based DCO output for width 2000 nm

Table 8 — Comparative study of the proposed work with existing literature

| Ref. | DCO Architecture | Technology | Oscillation frequency | Reported power | Tuning range (%) | Key features |
|---|---|---|---|---|---|---|
| [4] | CMOS Ring DCO | 180 nm | 0.45–1.20 GHz | 520 mW | 90 | Narrow tuning range and high power |
| [26] | Varactor-based DCO | 130 nm | 0.80–2.10 GHz | 610 mW | 89 | Moderate tuning, high power |
| [27] | CMOS DCO | 90 nm | 1.10–2.75 GHz | 480 mW | 85 | Limited resolution |
| [28] | Active-Inductor DCO | 90 nm | 1.20–3.00 GHz | 470 mW | 85 | Restricted tuning span |
| [29] | Active-Inductor DCO | 65 nm | 3.2–6.5 GHz | 6.1 mW | 68 | Higher noise |
| Proposed 3-Stage DCO | CMOS inverter+ NAND-based inverter | 90 nm | 4.018-1.557 GHz | 451.8- 404.7 mW | 88 | Highest tuning range with improved resolution |
| Proposed 5-Stage DCO | CMOS inverter+ NAND-based inverter | 90 nm | 1.832-0.655 GHz | 451.6- 404.3 mW | 95 | Better stability and low-power operation |
| Proposed 7-Stage DCO | CMOS inverter+ NAND-based inverter | 90 nm | 1.188- 0.448 GHz | 451.6- 404.3 mW | 90 | Improved low-frequency stability with compact design |

The proposed 3-, 5-, and 7-stage DCOs illustrate enhanced performance features of the designed circuit, including improved frequency tuning capability and lower power consumption. Table 8 provides a comprehensive comparative analysis of the proposed work and various literature DCO designs and architectures, demonstrating the performance improvements achieved by the proposed DCO architecture. This proposed DCO architecture also have some limitations. The transistors count in the design is comparatively higher, increasing the overall circuit complexity. Furthermore, although binary-weighted PMOS transistors and MOS varactors significantly improve power consumption and frequency resolution, they also increase circuit area.

## 4 Conclusion

This paper presented a simulation-based investigation of 3-stage, 5-stage, and 7-stage digitally Controlled Oscillator circuit architectures, simulated in 90 nm CMOS using the Cadence Virtuoso tool at a supply voltage of 1 V. The proposed design comprises delay stages based on a CMOS inverter and a NAND gate-based inverter, utilising a PMOS switching network, MOS varactors and active inductors at three different transistor widths (W=1µm, W=1.5µm, W=2 µm). These circuit designs demonstrate that the combination of fine tuning via MOS varactors and coarse tuning through digitally controlled PMOS switches permits wide frequency tuning with high resolution while maintaining low power operation. For the 3-stage DCO, the power consumption varied from 451.8 mW to 404.7 mW with frequency ranging from 4.018 GHz to 0.517 GHz, depending on the control bits and transistor width. The 5-stage and 7-stage DCOs shown gradually lower frequency ranges with comparable power levels, offering enhanced stability for lower-frequency applications. In addition, supply voltage ranging from 0.5 V to 1.0 V shown predictable increase in both power consumption and frequency across all configurations. The proposed DCO architecture gives enhanced frequency tuning with high resolution while sustaining low power consumption, which makes them highly suitable for low power and high frequency tunning applications in modern VLSI technology.

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