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Comprehensive Analysis of Interleaved Boost and Totem-Pole PFC Converters with Various Low-Frequency Devices for Electric Vehicle Charging Applications

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The shift to electric vehicles (EVs) has raised the requirements of high-efficiency, high power density on-board chargers (OBCs) with the capacity to comply with tough standards of power quality like IEC 61000-3-2. The paper provides a comparative study on the advanced Power Factor Correction (PFC) topologies that comprise Boost PFC, Multi-Phase Interleaved Boost PFC, Bridgeless Totem-Pole PFC, and Interleaved Totem-Pole PFC Converters. The input current shaping, voltage regulation, efficiency, switching stress, and general performance of various types of low-frequency (LF) switching devices; Metal Oxide Semiconductor Field Effect Transistor (MOSFETs), diodes and Silicon Controlled Rectifiers (SCRs) are systematically compared. A mathematical modeling framework and Average Current Mode Control (ACMC) strategy with nested proportional integral (PI) loops are developed and tested with an elaborate MATLAB/Simulink simulation. Both closed and open-loop performances are examined and proved that Totem-Pole PFC are more efficient as its power factor comes around 0.99, its THD is <5 %, efficiency >95 % and output voltage ripple comes less than 2 % with all low frequency devices and minimal with SCR around 2 % THD, 98 % efficiency and less than 1 % output voltage ripple. The findings give a viable design consideration to on-board chargers of high-performance EV.

Keywords: Totem-pole PFC, Interleaved PFC, Average current mode control, Low frequency devices, Electric vehicle chargers, Total harmonic distortion, Power factor correction

1 Introduction

In power electronic systems of the modern era, power factor correction (PFC) converters are necessary to enhance the quality of power, minimize harmonic distortion, and comply with grid standards. Out of the numerous PFC topologies, the traditional boost PFC converter is a very popular topology because of its simplicity, reliability and high cost-effectiveness in low and medium power applications. Nevertheless, there has been an upward trend towards greater efficiency and power density in current applications (e.g. electric vehicle (EV) charging systems and industrial power supplies) that requires advanced converter topologies and control methods.

Recent progress in the wide bandgap semiconductor devices has seen a breakthrough in converter efficiency and high-frequency performance, in particular Gallium nitride (GaN) transistors. These trends have increased the pace of using more advanced topologies like totem-pole PFC converter that has less conduction loss, high efficiency and power density than the traditional bridge based converters. On the same note, the interleaved boost PFC converters have been proposed as a solution to the shortcomings of the traditional boost converters as they decrease the ripple of the input current, provide better thermal characteristics, and provide better system reliability.

Besides topology enhancement techniques, complex control strategies have been extensively studied in order to improve the converter performance. One of these techniques is the average current mode control (ACMC), which has been utilized widely since it has the ability to provide precise current shaping, stable operation and better dynamic performance. In addition, switching devices can be a decisive factor in converter performance, especially regarding efficiency, total harmonic distortion (THD), power factor and output voltage ripple.

Despite the many investigations conducted on the single PFC topologies and control strategies, there has been a lack of systematic comparison of boost PFC, interleaved boost PFC and totem-pole PFC converters operating under identical operating conditions. Specifically, the effect of various low-frequency switching devices, including MOSFETs, silicon-controlled rectifiers (SCRs), and diodes, on the work

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of converters has not been studied comprehensively in a single framework.

Thus, the paper will be a comparative study of three common forms of PFC topology, namely boost PFC, interleaved boost PFC and totem-pole PFC, which are constructed with various low-frequency switching devices. A regular control method is used whereby an average current mode control (ACMC) is used on the boost and interleaved boost converters whereas an improved ACMC method with zero-crossing point detection is used on the totem-pole converter to guarantee safe operation. The conduct of every topology is put in terms of important parameters, such as power factor, total harmonic distortion (THD), efficiency, and output voltage ripple, to offer realistic information on design of high-efficiency and low-distortion power electronic applications.

2 Literature Review

Power factor correction (PFC) converters have developed a great deal in terms of efficiency, power quality and power density in AC–DC conversion systems. A cost-effective boost converter topology with a combination of reverse-recovery reduction and power factor correction techniques was presented[1]. The approach is proposed to realize a conventional boost PFC stage with reduced diode reverse-recovery loss, which improves the conversion efficiency, and limits harmonic distortion during single-phase AC–DC conversion. A complete reference of gallium nitride (GaN) transistors, including device physics, characteristics, gate driving requirements and applications in high efficiency power conversion systems has done. The study pointed out the advantages of GaN devices over existing silicon-based devices for use in PFC and other power electronic applications, including switching frequency capability, switching loss, and overall performance[2]. A detailed review of totem-pole PFC converters for high power applications was presented. The work highlighted the benefits of using a bridgeless totem-pole topology over the traditional structure with its input diode bridge, such as the benefits in terms of conduction losses, efficiency and power quality. There were also discussions on the challenges in the practical implementation, control strategies, and suitability for high-power applications. In an analytical model for calculating switching losses in case of a GaN HEMT used in a totem-pole PFC converter was proposed[3]. Considering the device characteristics from the device datasheet, the model was able to accurately estimate the switching losses with continuous conduction mode (CCM) operation. Experimental tests showed that a single-phase totem-pole PFC converter with 650 V GaN cascade devices achieves maximum efficiencies of 99.26 % at 3.6 kW and 50 kHz[4]. Basic power electronics related concepts used in a PFC system were adequately explained. It discussed the operating modes of PFC converters, average current-mode control, inductor design consideration, loss mechanism in boost derived converter etc. and laid the foundation for the development of PFC technology[5]. The master-slave control design of high-power interleaved boost converter was studied. The study was focused on the current sharing and the stability of the multiphase converter configurations and showed that the proposed control strategy was able to decrease the current ripple level and enhance the dynamic performance[6]. In the average current-mode control approach for interleaved boost converter was discussed and modeled and implemented[7]. The results indicate that the performance of the total harmonic distortion (THD) is significantly improved with the use of phase interleaving and that the input current ripple is substantially reduced. The comparative analysis of bridge and bridgeless boost PFC AC–DC converters has been done. The results showed that the efficiency and conduction losses of the bridgeless topology are higher than the other topology because of the lesser number of semiconductor devices in the current path[8]. The Sliding Mode Control (SMC) for a single-phase interleaved totem-pole PFC converter was proposed for electric vehicle On-board Chargers (OBC). The controller exhibited good voltage regulation capabilities, a fast transient response, and effective harmonic mitigation with different operating scenarios[9]. A phase-shifting control method was used to obtain a soft-switching capability in an interleaved totem-pole bridgeless boost PFC converter. The presented approach minimized switching losses and enhanced efficiency of the converter for the entire operating range[10]. A bridgeless interleaved totem-pole PFC converter for plug-in electric vehicles was presented. The design targeted low input current ripple, low electromagnetic interference (EMI), and bidirectional power-flow, which would be ideal for vehicle-to-grid applications[11]. A reconfigurable variable turns ratio H–bridge ZCS/ZVS DC–DC

partial power converter for integrated onboard chargers was studied. The study focused on electricity vehicle application efficiency, flexibility and better charging performance[12]. A comparison of various low frequency devices of the totem-pole PFC converter is reported. The study compared diodes, MOSFETs and SCRs as input current shapers and voltage regulators. Progressive improvement was seen in the case of the diode-based implementation (approx 95 % efficiency, approx 5 % THD) to MOSFET based implementation (approx 97 % efficiency and 3 % THD) and then to SCR based implementation (nearly unity power factor (approx 0.995) and THD around 2 %)[13]. The comparison between interleaved boost PFC and totem-pole PFC converters for EVs was given in[14]. The results showed that interleaved-totem-pole (ITP) structures with SCRs for the low-frequency leg resulted in higher performance, which included a power factor of ~0.999, THD < 1 %, efficiency > 99 % and ripple < 5-6 %, thanks to the lower conduction paths and better ripple cancellation. The study of advanced control strategies for single-phase high efficiency PFC converters (bridgeless GaN) was explored in[15] and is another achievement towards high efficient PFC systems. Planar coupled inductors of the dual-phase interleaved GaN-based totem-pole PFC converter were optimized. Optimized inductor structures were proven to enhance magnetic design, efficiency and power density[16]. A single-stage bidirectional AC–DC conversion using high-frequency magnetic isolation with interleaved totem-pole zero-voltage-switching (ZVS) converter was proposed. The converter had high efficiency and suitability for bi-directional power conversion applications[17]. The authors proposed a buck PFC converter using interleaved boundary conduction mode (BCM), and showed that interleaved PFC can be used to enhance the converter performance and reduce current ripple[18]. A two-phase interleaved boost PFC converter is proposed using a variation-tolerant phase-shifting technique. The technique was found to make the converter more robust to changes in the parameters, improve current sharing, and to ensure stable operation when the converter was operated under different conditions[19]. An optimum design methodology for interleaved boost PFC converters was proposed. Frequency switching, boost inductance and output voltage were proposed as design parameters. The results demonstrated that proper selection of parameters can enhance the efficiency and reduce power losses[20]. A powerful adaptive control strategy for active power filters for power factor correction, harmonic compensation and load balancing of nonlinear loads has been developed[21]. The designed controller showed better harmonic suppression and stable operation under different load conditions that paved the way to use advanced control methods in modern PFC systems. One current-balancing method of interleaved boost PFC converter, which uses an auxiliary-winding coupled inductor, was proposed in[22]. The method allowed the converter phases to share the current equally, minimized circulating currents, and increased the overall reliability of the system, especially in high-power applications. A soft switching two switch resonant AC-DC converter with high power factor was proposed. The converter successfully showed the advantages of the soft-switching operation in the PFC systems in terms of reduced switching losses, increased efficiency, and reduced electromagnetic interference[23]. An active compensation based harmonic reduction method to reduce the power quality problem caused by electric vehicle charging system was presented[24]. The proposed technique successfully mitigated the harmonic distortion and enhanced the performance of the grid side, underlining the significance of harmonic mitigation measures for high power EV charging applications. Based on the literature review, it can be concluded that there is a clear progression in using PFC totem-pole designs, and in particular, those with interleaved PFC switching legs using WBG devices in the high-frequency switching legs and SCRs in the lower-frequency switching legs. They are considered as attractive solutions for high-power electric vehicle on-board chargers since they are known for their power quality compliance (IEC 61000-3-2), for their low harmonic distortion, and for their thermal performance, power density, and efficiency.

2.1 Motivation

Power factor correction (PFC) converters are an essential part of current power electronic devices, especially in the electric vehicle charger, data center and renewable energy interface fields. As regulatory requirements on the quality of power increase, there is a high demand to obtain high power factor, low total harmonic distortion (THD), and high efficiency at the same time. Even though conventional boost PFC converters are very popular because of their simplicity

and ease of control, their performance is frequently characterized by conduction losses and ripple of the input current, particularly at higher power levels. Interleaved boost PFC converters overcome some of these constraints by sharing current better and allowing less ripple, however, at the cost of further control complexity. Conversely, bridgeless totem-pole PFC converters have appeared as a highly useful device because of their bridgeless design, however, their operation is highly sensitive to the switching devices and appropriate control under zero-crossing situations. Moreover, the choice of low-frequency devices like MOSFETs, Silicon Controlled Rectifier (SCRs) and diodes are also important determiners of converter performance, and can affect performance, switching losses and harmonic responses. Nonetheless, there is still no apparent and systematic comparison of these devices during the various PFC topologies in the literature. Thus, the rationale of this work is to give a full and unbiased comparison of boost PFC, interleaved boost PFC, and totem-pole PFC converters under various low-frequency switching devices. Through assessing the main performance parameters including power factor, THD, efficiency and output voltage ripple under the same control strategies, this paper seeks to provide some practical information useful in choosing appropriate converter designs in the context of high performance.

3 PFC Topologies

3.1 Single-Stage Boost PFC (Conventional Boost + Diode Bridge)

Figure 1 is the conventional PFC topology where an AC input is rectified by a diode bridge and the resultant DC is fed to the boost converter to boost the voltage to the needed DC-bus. The boost switch is operated such that the input current is made to follow a sinusoidal reference (usually proportional to the instantaneous input voltage), normally via Average Current Mode Control (ACMC) or some other control mode. This topology rectifies AC via a diode bridge, followed by a boost converter (Fig. 1). It operates in Continuous Conduction Mode / Discontinuous conduction Mode / Critical Conduction Mode (CCM/DCM/C_rCM). In CCM, inductor current i_L follows:

$$\frac{di_L}{dt} = \frac{V_{in} - V_o(1-D)}{L} \quad \ldots (1)$$

where V_{in} is rectified input, V_o output voltage, D duty cycle, L inductance.

In CCM, the inductor current never falls to zero, lower ripple, better power quality, but larger inductance and higher losses. In DCM / C_rCM: simpler design, reduced inductance, but higher current ripple, higher THD, more stress on components[12]. Its implementation is simple, only one active switch is used and it can be very easily controlled. But here diode bridge is used which introduces conduction losses (about two diode drops during conduction), reducing efficiency especially at high power. The input current ripple and harmonic distortion are significant in lower cost designs, especially with DCM/CrCM[15].

3.2 Interleaved Boost PFC (Multi- Phase Boost)

Figure 2 shows multiple boost converter "legs" or phases are connected in parallel and each operating with a phase shift (e.g. for two phases 180°, for three phases 120°, for four phases 90°). All stages share the same output DC bus, each handles part of input current. For two phases:

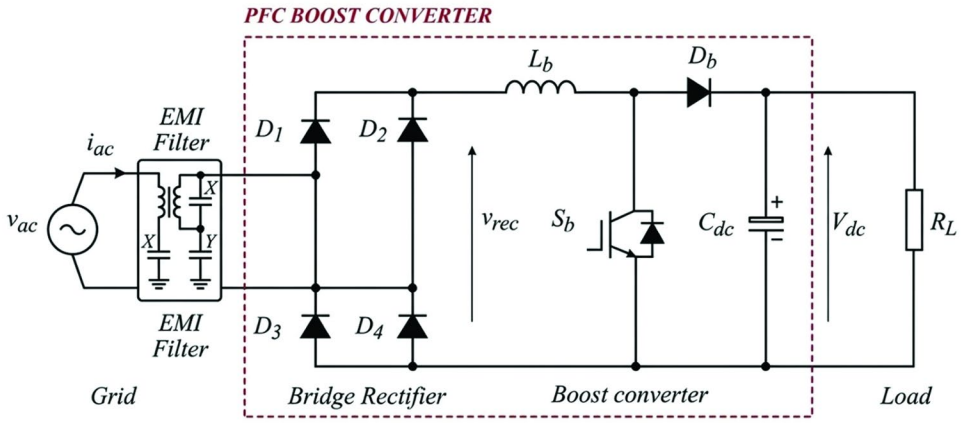

Fig. 1 — Single- Stage Boost PFC

$$\Delta i_{total} = \Delta i_{phase} \times (1-2D) f \ \ or \ D < 0.5 \quad \ldots (2)$$

where D = Duty cycle, f = frequency, Δi_{phase}= Phase Current, $\Delta i_{total} = Two\ phase\ current$

Interleaving cancelled ripple because phases are offset, the high-frequency ripple currents in different legs cancel each other partially when summed, reducing total input current ripple. Also each leg carries less current, so there is better heat spreading and smaller component stress. Due to reduced ripple input filter size is also small. Similar to single boost: CCM, DCM, CrCM. Typically, interleaving helps reduce ripple even in DCM/CrCM, but CCM operation still gives best quality. It Reduced input current ripple, lower THD, better efficiency under higher loads[14]. It also enables higher power without dramatically increasing size of magnetics or stressing a single switch. In Interleaving, more inductor, more switches are used so its control is also very complex to maintain phase balancing[16].

3.3 Bridgeless Boost PFC

The "bridgeless" concept removes the diode bridge that normally precedes a boost PFC as shown in Fig. 3. Instead, one uses MOSFETs or active switching devices to perform rectification + boost in fewer current-carrying elements. Depending on exact implementation, body diodes of MOSFETs may substitute for slow diodes, reducing conduction losses[16]. It can be used with DCM, CrCM, CCM but the performance improves with CCM. Critical Conduction Mode (CrCM) / Discontinuous mode might simplify implementation but at cost in THD. Body diode recovery modeled as:

$$Q_{rr} = \int I_{rr}(t)\, dt \quad \ldots (3)$$

where, $I_{rr} = Reverse\ recovery\ Current$, $Q_{rr} = Reverse\ recovery\ charge$

It lower conduction losses because fewer semiconductor drops; fewer diodes in conduction path. It has potential for higher efficiency, particularly at high power and if MOSFETs are well chosen then there is possibly smaller thermal stress. But more complex control / gate drive, especially to manage current flow during both half-cycles and avoid cross-conduction. Body diode reverse recovery (if used) may still introduce losses or switching challenges[17].

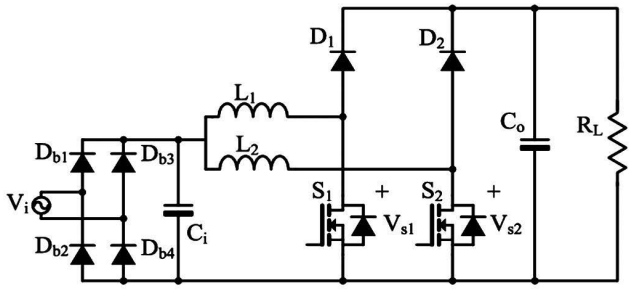

Fig. 2 — Interleaved Boost PFC

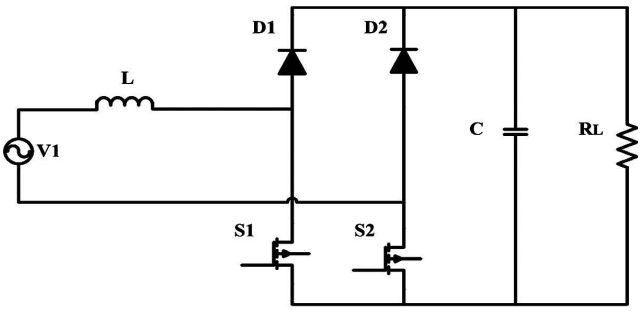

Fig. 3 — Bridgeless Boost PFC

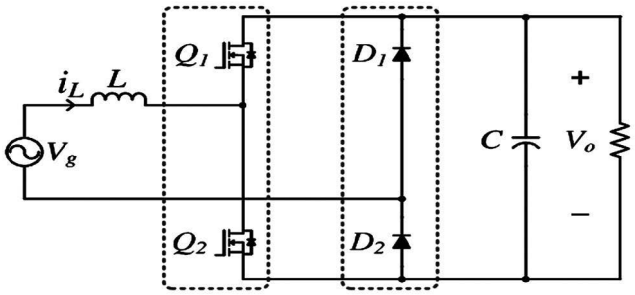

Fig. 4 — Totem-Pole PFC

3.4 Totem-Pole PFC (Bridgeless Totem-Pole)

The totem-pole PFC shown in Fig. 4 integrates active switching in place of the diode bridge, using two switching legs forming a "totem-pole" configuration; during one half-cycle one leg conducts, during the other half the complementary leg handles conduction. The boost function is merged with rectification, using MOSFETs or wide-bandgap switches. It operates best in Continuous Conduction Mode (CCM) for lowest ripple and best THD, but certain designs operate in CrCM/CRM (Critical or Critical-conduction / Boundary conduction) especially during light load. Some totem-pole bridgeless PFCs use triangular current mode or other specialized modulation methods for improved performance. It eliminates or greatly reduces diode bridge losses, especially the slow recovery diodes; conduction path has fewer voltage drops. LF leg uses diode/MOSFET/SCR.

For SCR

$$I_{holding} << I_L << I_{latching} \quad \ldots (4)$$

where, $I_{holding} = Holding\ current, I_{latching} = Latching\ current$

It also Improved power density because magnetics can be smaller when higher switching frequencies are allowed due to lower losses. But harder to achieve full zero voltage switching (ZVS) or soft-switching across full input/output ranges. And also, its control is more complex, gate must switch safely to avoid shoot-through body[18].

3.5 Interleaved Totem-Pole PFC

Figure 5 shows Interleaved Totem-Pole PFC. It Combines the benefits of both interleaving and totem-pole arrangement. Multiple totem pole legs (each with its own active switching branch) are operated phase-shifted. The goal is to further suppress ripple, distribute power & thermal load, and push efficiency higher. Typically, CCM for best performance; at light load either CrCM or boundary conduction is used. Often used in applications demanding high power (> a few kilowatts) where efficiency gains justify added complexity. It has very low input current ripple; THD approaches theoretical minima. It has excellent efficiency, especially when wide-bandgap devices are used; conduction and switching losses are low. It has better distribution of stress among devices; smaller inductors per leg (or smaller combined inductance) possible because of phase cancellation. Phase shift minimizes ripple:

$$\Delta i = \frac{V_{in} \times D \times (1-D)}{f_s \times L \times N} \quad \ldots (5)$$

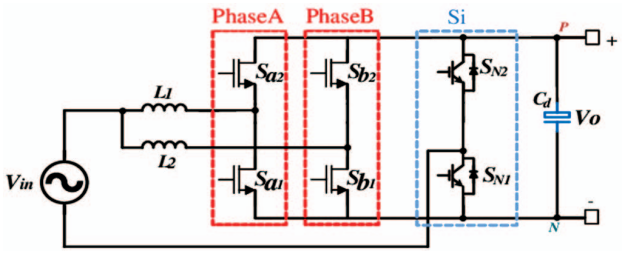

Fig. 5 — Interleaved Totem-Pole PFC

where N is phases, D = Duty cycle, L= Inductance, $\Delta i = current\ ripple, V_{in} = Input\ Voltage$

But it has more challenging layout and gate driver complexity[19].

4 Mathematical Modelling

4.1 Conventional Boost PFC

Inductor Voltage Equation

During ON State

$$V_L = V_{in} \quad \ldots (6)$$

where $V_L = Inductor\ voltage$

During OFF State

$$V_L = V_{in} - V_o \quad \ldots (7)$$

where $V_o = Output\ Voltage$

Applying Volt-Second Balance

$$D \times V_{in} + (1-D) \times \left(V_{in} - V_O\right) = 0 \quad \ldots (8)$$

On Solving

$$V_o = \frac{V_{in}}{1-D} \quad \ldots (9)$$

Inductor Design

$$L = \frac{V_{in} \times D}{f_s \times \Delta I_L} \quad \ldots (10)$$

where

$f_s = Switching\ frequency, \Delta I_L = Inductor\ Current\ Ripple$

4.2 Interleaved Boost PFC

For N phases

$$I_{phase} = \frac{I_{total}}{N} \quad \ldots (11)$$

Ripple reduction factor

$$\Delta I_{total} = \Delta I_{phase} \times \left[\frac{1}{N} \sum e^{\frac{j \times 2 \times \pi \times k}{N}}\right] \quad \ldots (12)$$

4.3 Bridgeless Boost PFC

In Conventional Boost, Current path includes 2 diode drops

Fig. 6 — Operation of all Topologies

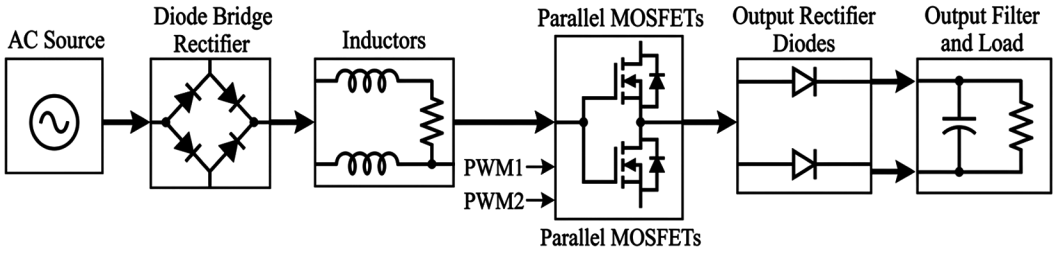

Fig. 7 — Simplified Block Diagram of Interleaved Boost PFC

$$P_{loss} = 2 \times V_d \times I \quad \ldots (13)$$

Where $V_d = Diode\ voltage\ drop$

But Bridgeless removes one diode drop

$$P_{loss} = V_d \times I \quad \ldots (14)$$

4.4 Totem-Pole PFC

Boost equation

$$V_o = \frac{V_{in}}{1 - D} \quad \ldots (15)$$

Conduction Loss

$$P_{cond} = I^2 \times R_{DS(on)} \quad \ldots (16)$$

where

$R_{DS(on)} = Drain - to - Source\ ON\ Resistance$

4.5 Frequency Device

Diode Model

Forward drop

$$V_f = 0.8 - 1V \quad \ldots (17)$$

Reverse recovery loss

$$P_{rr} = Q_{rr} \times f_s \times V_{dc} \quad \ldots (18)$$

MOSFET Model

$$P_{cond} = I^2 \times R_{DS(on)} \quad \ldots (19)$$

Switching loss

$$P_{sw} = \frac{1}{2} \times V \times I \times \left(t_r + t_f \right) \times f_s \quad \ldots (20)$$

where $t_r = Rise\ time,\ t_f = Fall\ time$

CR Model

Forward drop ≈ 1.2V … (21)

4.6 System Design and Control

The system targets 200-400 V AC input, 390-400 V DC output, 3.3 kW power. Components: EMI filter, HF IGBT/MOSFET, LF diode/MOSFET/SCR.

Control uses ACMC with outer voltage PI and inner current PI loops. Voltage loop transfer function:

$$G_v(s) = \frac{K_p \times s + K_i}{s} \times \frac{V_o}{C \times s + 1/R} \quad \ldots (22)$$

where $K_p = Proportional\ Gain\ of\ the\ controller$

$K_i = Integral\ Gain\ of\ the\ controller$

Current Loop

$$G_i(s) = \frac{1}{L \times S + R_L} \quad \ldots (23)$$

PI tuning: For voltage, Kp = 0.1, Ki=10; … (24)

current, Kp =5, Ki=500; … (25)

Soft-start with SCR precharge limits inrush

$$I_{inrush} = \frac{V_{in}}{R_{pre} + \omega \times L} \quad \ldots (26)$$

5 Experimental Model, Control Design and Simulation Parameter

The Fig. 7 is a two-phase interleaved boost Power Factor Correction (PFC) converter, which aims at transforming a single-phase AC source into a regulated DC load without compromising the power factor. The AC voltage input is then measured and fed through a diode bridge rectifier which then transforms it into pulsating DC. This unregulated direct current is subsequently inputted in the stages of boost converters. This front-end rectification is necessary to give a suitable DC input to the further power processing without compromising the information in the waveform required to correct the power factor. The interleaved boost converter is in the center of the system; this converter has two parallel branches of boost converters that are the same. Both branches consist of an inductor, a MOSFET switch, a diode, and an element of current sensing. These two converters are operated by different PWM signals

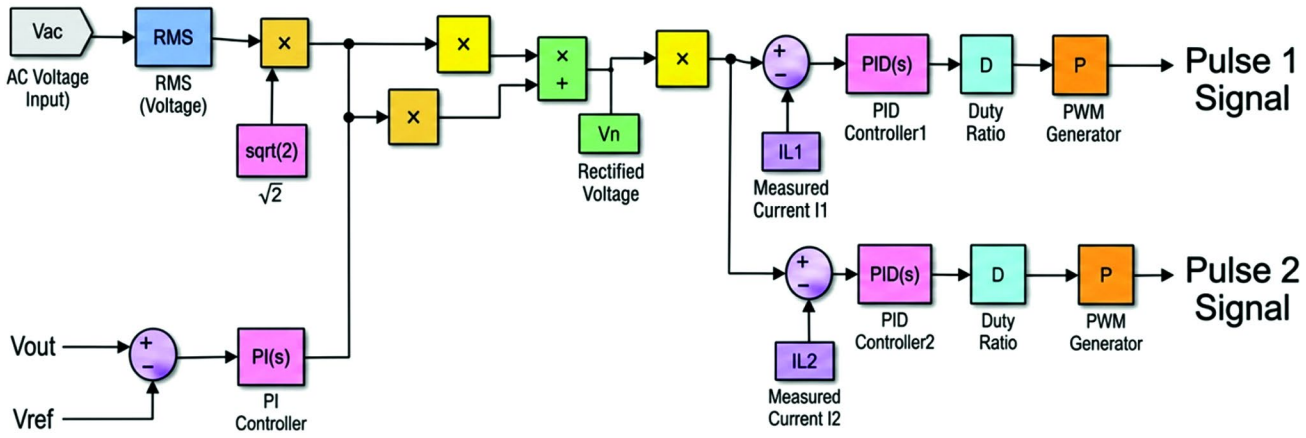

Fig. 8 — Controller Design of Interleaved Boost PFC

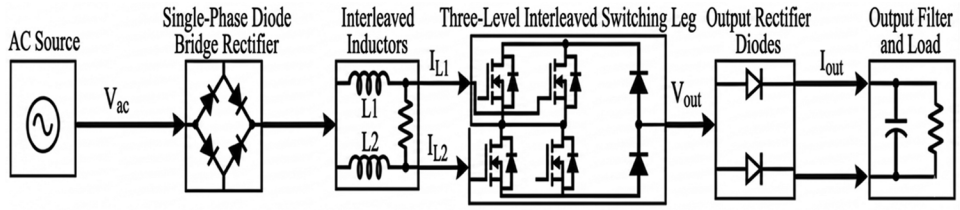

Fig. 9 — Simplified Block Diagram of Interleaved Totem-Pole PFC with diode as LF device

which are 180 degrees phased shifted. The advantages of this interleaving method include a very low input current ripple, high efficiency and spreading thermal stress throughout the components. The two inductive currents (IL1 and IL2) creates the total input current and yields a smoother output that closely resembles the input voltage. On the output stage, a capacitor will be used to smooth the DC voltage that has been boosted and provide a constant voltage to the load. Output voltage (Vout) and the current (Iout) are constantly measured to provide feedback and performance monitored. The model also has additional measurement blocks that monitor diode currents, switching behavior of MOSFETs, and inductor currents that are handy in studying.

The model uses an average current mode control strategy as a controller Figure 8, which is very common in the applications of PFC. Its main objective is to control the output voltage to a required reference value (usually 400 V) and is to ensure that the input current waveform is wave shaped on the same basis as the input voltage. This two-fold goal provides not only voltage regulation but also almost unity operation of the power factor. Here, the control process starts with the measurement of input AC voltage which is put through RMS block to find its effective value. This value is scaled (by the square root of two) to get the maximum voltage which is employed to produce a reference waveform. At the same time, the reference voltage is compared with the output voltage and the error is fed on a PI controller. These outer voltage loop define the value of power required to be drawn out of the source and creates a control signal which is proportional to the necessary current amplitude. A reference current waveform is produced using this control signal and it is multiplied with the normalized input voltage. This makes the reference current to be of the same shape as that of the input voltage, which is critical in the establishment of power factor correction. The reference current is further divided evenly across the two interleaved phases.

In Fig. 9 is a bridgeless, totem-pole power factor correction (PFC) converter with the topology being a common topology in high-efficiency AC-DC conversion, such as server power supplies and EV chargers. The AC input (Vac) is initially worked with inductors (IL1, IL2) which form the current input. The circuit consists of a totem-pole configuration of switches (MOSFETs/IGBTs) and diodes instead of a conventional diode bridge and, therefore, has lower conduction loss and higher efficiency, particularly at high power levels. The Pulse Width Modulation (PWM) signals (PWM1-PWM4) that comprise a high

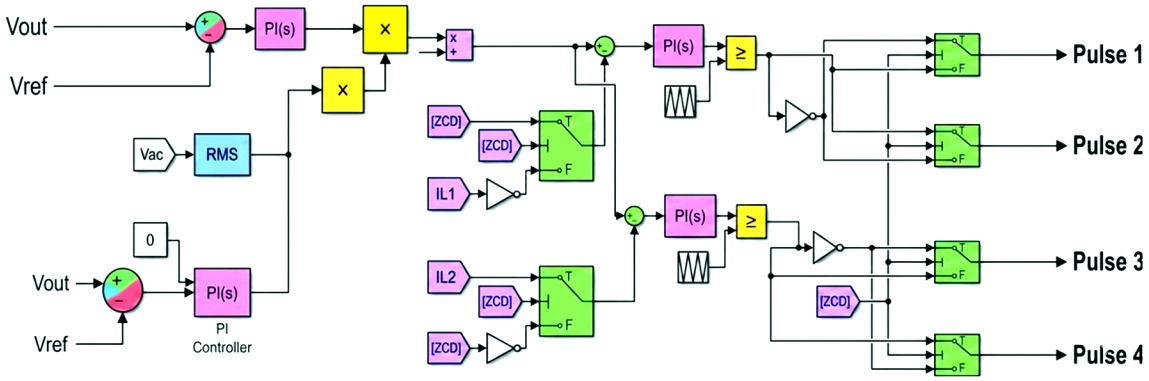

Fig. 10 — Controller Design of Totem-Pole PFC with Diode as LF device

frequency leg and a low frequency leg push the switching network. At any point in half a cycle of the AC input, one side of the system is operating in synchronous rectification mode and the other in high frequency switching mode. Storing and releasing energy by the inductors under a controlled manner is done to achieve a sinusoidal input current that is synchronized with the input voltage waveform in order to achieve a power factor of close to unity. The continuous rectified voltage is smoothed in the output (reverse) DC-link capacitor to create a constant DC signal (Vout ≈ 399 V as indicated). Power quality is measured using such performance metrics as Total Harmonic Distortion (THD ≈ 5.3 %) and Power Factor (PF ≈ 0.998). The low THD shows that the input current has lower harmonic content and the almost-unity PF shows that the current waveform is being shaped. Other measurement blocks are used to measure the inputs of the system, the currents of the inductor, as well as the voltage/current of the output to give a whole picture of the behavior of the system during steady state conditions.

It has a two-loop controller approach that is an outer voltage loop and an inner current loop to control the output voltage and a sinusoidal input current as shown in Fig. 10. The outer loop controls the measured voltage (Vout) against a reference voltage (Vref = 400 V). The fault is fed into a PI controller and an output current magnitude of the reference is produced. The extent of the input current required to sustain the desired DC output voltage is dependent on this. To make the input current an AC voltage waveform, the controller multiplies this current value with a normalized one of the input voltage (Vac). This generates a sinusoidal current reference in phase with the line voltage, which is necessary to high value power factor. Normalization and scaling are performed to RMS and absolute value blocks to make sure that they work under different conditions of inputs. The inner current control loop is a regulation of the inductor currents (IL1 and IL2). The inductor currents are compared to their respective references and the error is sent to PI controllers to produce PWM switching duty cycles. Zero Current Detection (ZCD) logic is provided to allow the detection of when the current flowing the inductor crosses zero, allowing appropriate mode switching and more efficient operation (especially at discontinuous or boundary conduction mode transitions). Lastly, comparator blocks and carrier signals create PWM pulses, which are rationally transmitted into the four switches (PWM1–PWM4). The correct operation is guaranteed with the help of logic gates and switching conditions in positive and negative half-cycles of the AC input. This synchronized control system enables the converter to have a controlled DC output, less harmonics, and a high efficiency and close to unity power factor.

Table 1 — Simulation parameters

Parameter	Symbol	Value
AC Input Voltage	V_{in}	230V RMS
Line Frequency	f_{line}	50Hz
Output DC Voltage	V_{dc}	400V
Rated Power	P_{out}	3.3kW
Switching Frequency	f_s	100kHz
Inductor Value	L	220µH
DC Link Capacitor	C	1000µF
Current Ripple	ΔI_L	20%
Sampling Time	T_s	0.5µs

The Table 1 provides information on the major design and operating parameters used to simulate the different Power Factor Correction (PFC) topologies explained in the previous graphs. The system has a universal AC

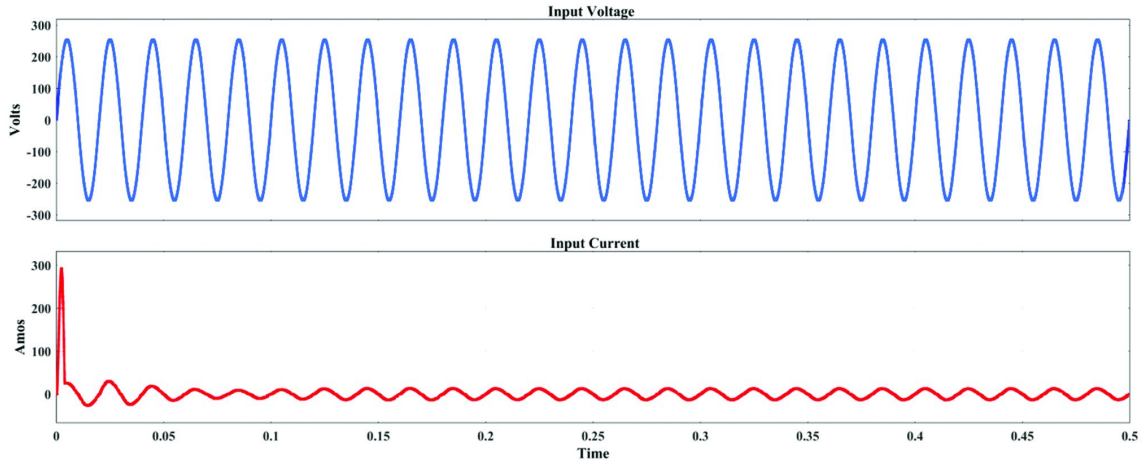

Fig. 11 — Input Voltage and Input Current Waveforms

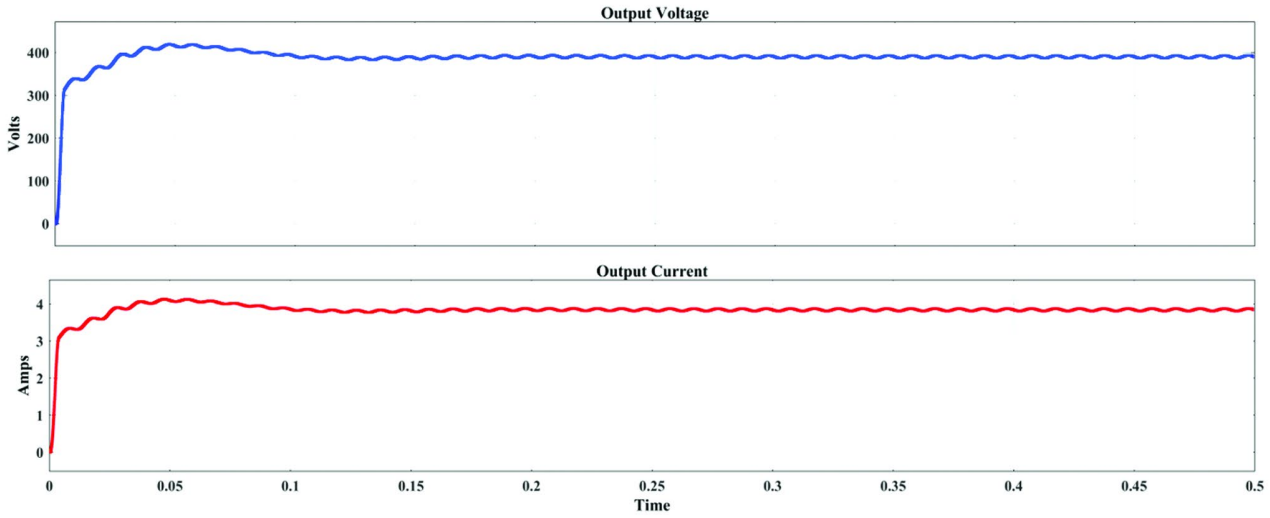

Fig. 12 — Output Voltage and Output Current Waveforms

input voltage of 230V RMS, line frequency of 50 Hz and a regulated DC output of 400 V at 3.3 kW. The switching frequency is 100 kHz, the value of the inductor is 220 µH, the value of the DC link capacitor is 1000 µF, and the allowed ripple of the inductor current is 20 %. The simulation has a sampling time of 0.5 µs. These parameters are applied to a typical high power, single-phase PFC converter system and will serve as a common metric for comparing the performance of the Boost, Interleaved Boost and various Topologies of Totem-Pole in terms of Power Factor, THD, Efficiency and Output Ripple.

6 Simulation Results

6.1 Boost PFC

Input voltage (blue) is a sine waveform with peak value of about 325 V (230 V RMS). The input current (red) has been shown to be similar in shape and phase to the voltage waveform in Fig. 11, which proves successful power factor correction. Graphical analysis reveals minimal distortion of the existing waveform, indicating that the overall harmonic distortion (THD) is approximately 10-15 % which meets requirements such as IEC 61000-3-2 of low-power equipment. The present amplitude is proportional to the load, indicating sinusoidal shaping of the ACMC inner loop.

The Fig. 12 shows the Output Current and Voltage Waveforms of Boost PFC. The output voltage (blue) increases smoothly when it is starting up and reaches a steady value of 400 V with a ripple of less than 2 percent (about 4 V peak-to-peak) satisfying a strong regulation by the outer PI voltage loop. The output current (red) stabilizes at about 3 A (as is expected of a 1.2 kW load in this simulation run) and the ripple is

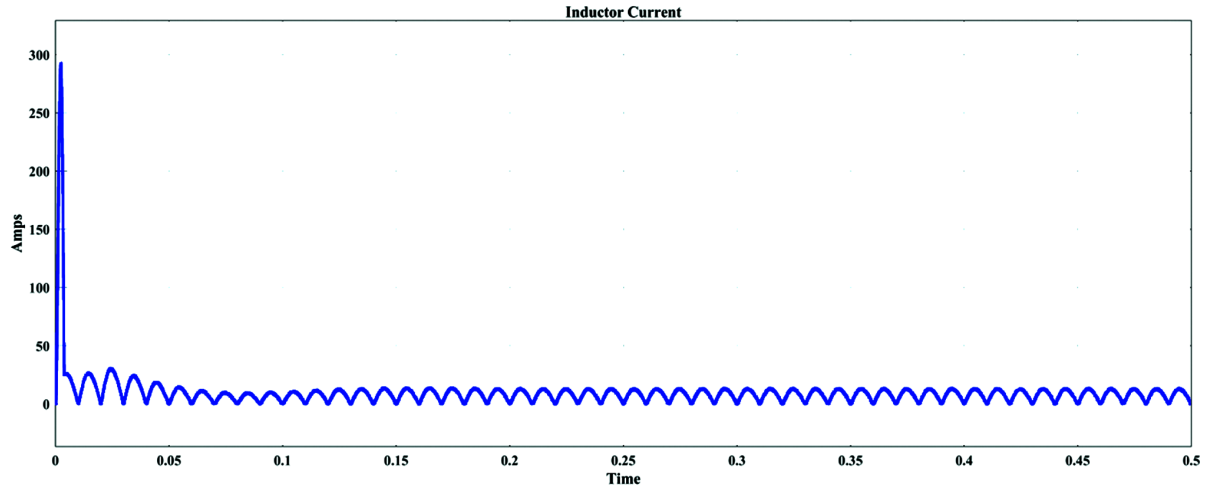

Fig. 13 — Inductor Current

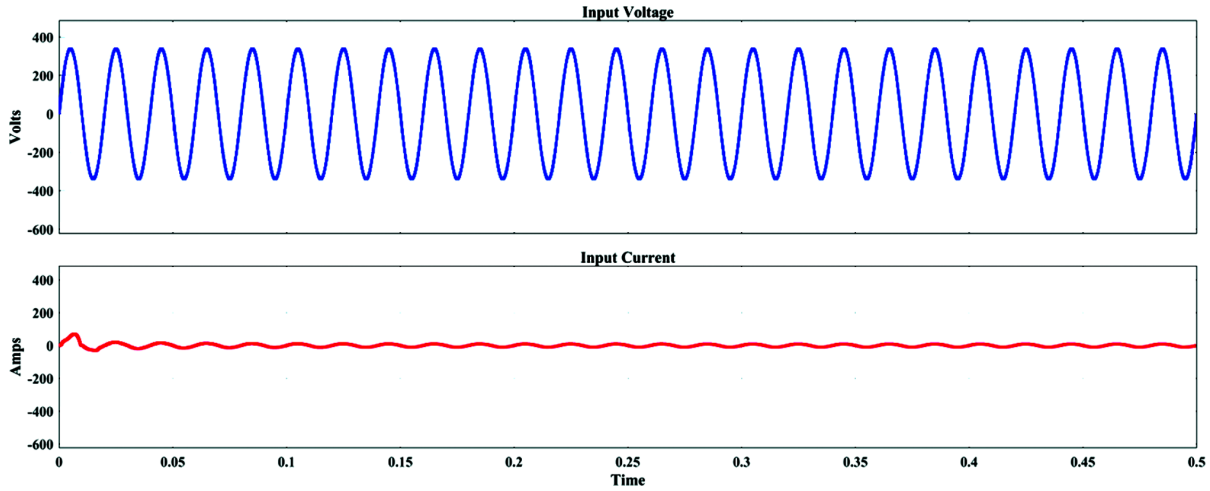

Fig. 14 — Input Voltage and Input Current Waveforms

Table 2 — Observed parameters of boost PFC

Parameter	Observed Value
Power Factor (PF)	≈0.95 - 0.98
Total Harmonic Distortion (THD)	≈ 10 - 15%
Efficiency	≈ 95%
Output Voltage Ripple	< 2% (+4V at 400V)
Input Current Ripple	High (~20 – 30%)
Inductor Current Mode	CCM
Startup Transient	Settling < 0.1s

also low. This constant DC response proves the boost performance and power transfer efficiency with temporary settling time of less than 0.1 s, which is appropriate to EV charging transients.

In Fig. 13, the inductor current waveform shows operation in continuous conduction mode (CCM), with the current never dropping to zero.

The results of the boost PFC (conventional Boost PFC) simulation under the above conditions are summarized in Table 2, Its power factor is in the range of 0.95-0.98, its Total Harmonic Distortion (THD) is in the range of 10-15 % and the efficiency is approximately 95 %. The output voltage ripple is less than 2 % (+4V on the 400V DC bus) and the input current ripple is comparatively high (20-30 %). The converter works in Continuous Conduction Mode (CCM) and the start-up transient is less than 0, 1 sec. These values are the best performance for the most basic topology and are good but not optimal for the power quality and efficiency that were compared in the study to the more sophisticated interleaved and totem-pole topologies.

6.2 Interleaved Boost PFC

The Fig. 14 shows the Input Current and Voltage Waveforms of Interleaved Boost PFC. The input

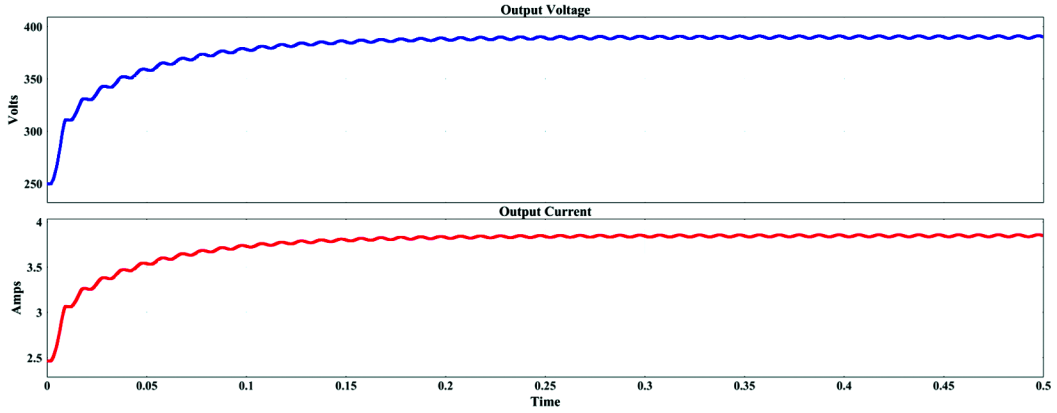

Fig. 15 — Output Voltage and Output Current Waveforms

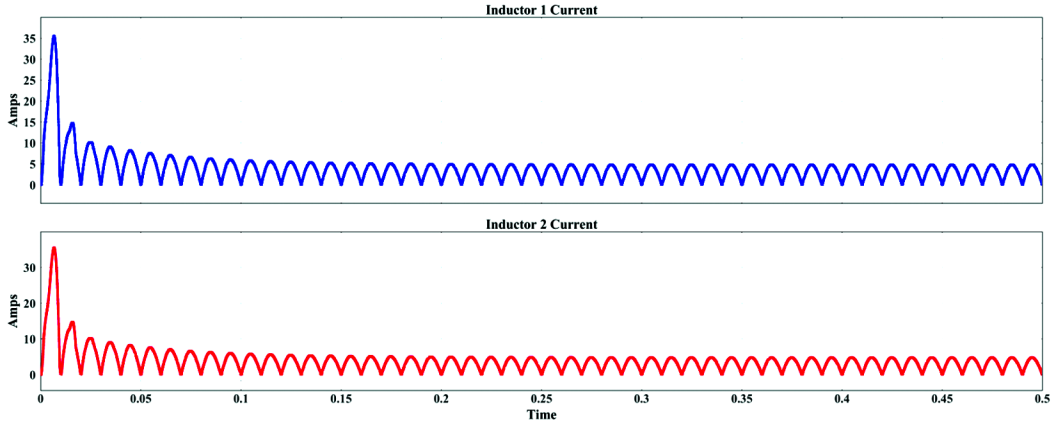

Fig. 16 — Inductor's Current

voltage (blue) has a clean sinusoidal waveform with the highest amplitude of about ±325 V, which is equivalent to a 230 V RMS (Root Mean Square) grid supply. Close phase and shape tracking of the input current (red) with minimum distortion is an indication of an effective power factor correction. Compared to the single-stage case, the present waveform is less discontinuous and the high-frequency ripple is lower because of the interleaving.

The Fig. 15 shows the Output Current and Voltage Waveforms of Interleaved Boost PFC. The output voltage (blue) increases at the start of the transient and it levels off to 400 V with a small ripple of between 2 to 3 V (0.5 to 1 percent peak-to-peak), demonstrating outstanding ability of the outer PI voltage loop to regulate. The output current (red) stabilizes at about 3.9 A (in agreement with a 1.5kW load segment in this run), and has the same low ripple and settling time of less than 0.2 s.

The currents in the inductors of the two phases are illustrated in Fig. 16, the upper one (blue) of phase 1 and the bottom (red) of phase 2. Every phase of current works in continuous conduction mode (CCM). The 180 ° phase difference is also clear with the ripple peaks of a given phase coinciding with the dales of the other creating effective cancellation of the overall input current.

Table 3 — Observed parameters of interleaved boost PFC

Parameter	Observed Value
Power Factor (PF)	>0.98
Total Harmonic Distortion (THD)	≈ 5 – 10 %
Efficiency	≈ 96.8 %
Output Voltage Ripple	< 0.5 % (+2V at 400V)
Input Current Ripple	<10 %
Startup Transient	Settling < 0.1s

Table 3 shows the observed parameters of the Interleaved Boost PFC topology. This brings the power factor to >0.98 and Total Harmonic Distortion (THD) to around 5-10 %. The efficiency is reduced to about 96.8 %, and the voltage ripple of the output is reduced to less than 0.5 % (400V DC bus voltage ripple of +2V). In addition, the transient response of the input current is well-regulated at <10 %, and the start-up

transient response is less than 0.1 seconds. This design can be appropriate for applications where the power quality, ripple rejection and efficiency gains of the interleaved operation of several boost converters are advantageous, but the complexity is not.

6.3 Totem-Pole PFC with LF Devices

The Fig. 17 shows the Input Current and Voltage Waveforms of Totem-Pole PFC with diode in LF leg. The input voltage (blue) is a normal sinusoidal waveform with peaks of ±325 V. The voltage is followed by the input current (red) with significant distortion and ripple especially around zero-crossings caused by the reverse recovery effects of the diodes (Qrr≈100nC).

As in the case with the diode, the input voltage (blue) is sinusoidal in nature. The tracking of the input current (red) is improved with lower distortion than that of the diode as shown in Figure 18 and is an advantage of synchronous rectification and reduced on-resistance (Rds(on)=0.05/s).

There is no change in the input voltage (blue) as shown in Fig. 19 but the SCR set-up generates the least distortion input current (red) and is characterized by little distortion at zero-crossings because of natural commutation and minimal reverse recovery (tq =50-100us).

The output (blue) reaches a steady state with a voltage of 400 V in a short-lived temporary ripple of less than 2 % (maximum). Output current (red) is steady at the point of about 3.3 A as shown in Fig. 20, and the LF losses cause a slight rise in ripple, which is indicative of the inefficiency of the diode in high power applications.

The output voltage (blue) and the current (red) are adjusted to 380-400 V and approximately 3.6A respectively with less than 1 % ripple as shown in Fig. 21. The MOSFET reduces the losses to attain additional settling and stability, which suits EV dynamic loads.

In Fig. 22, voltage (blue) and current (red) regulation is outstanding: (400 V) ripple = 0.3 A and precharge of the SCR decreases the startup overshoot

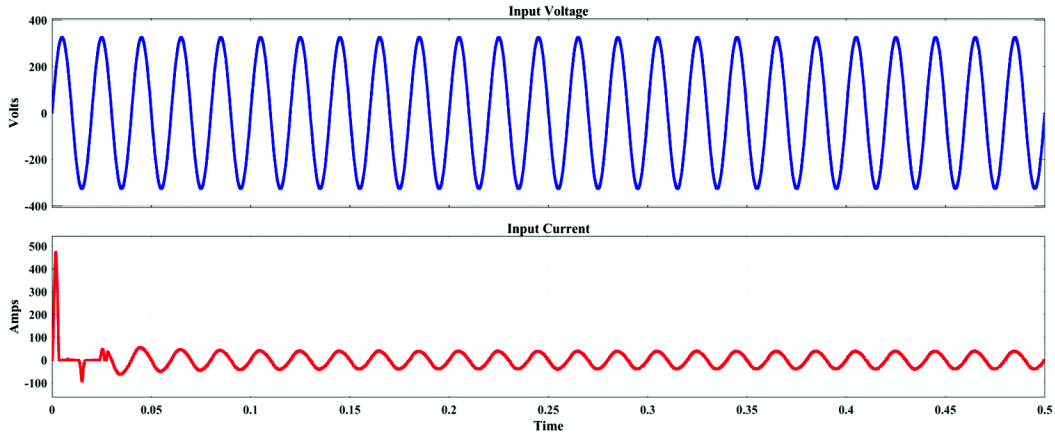

Fig. 17 — Input Voltage and Input Current with Diode in LF leg

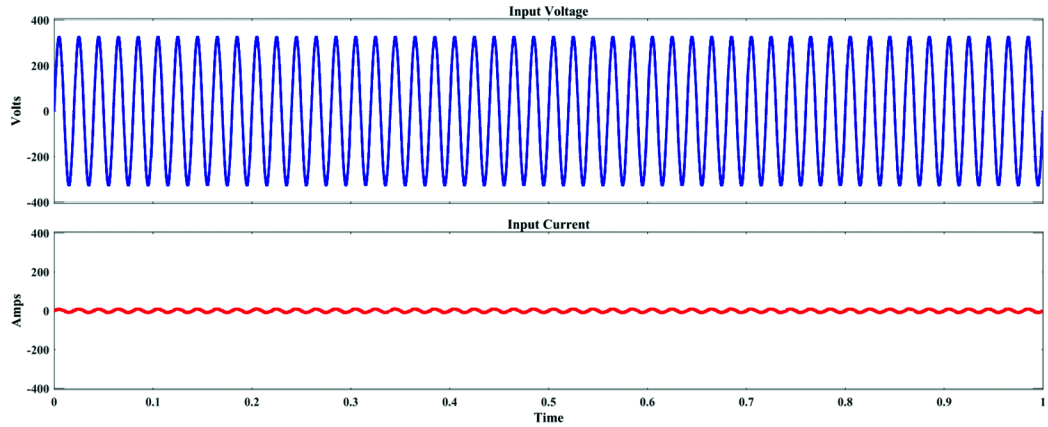

Fig. 18 — Input Voltage and Input Current with Mosfet in LF leg

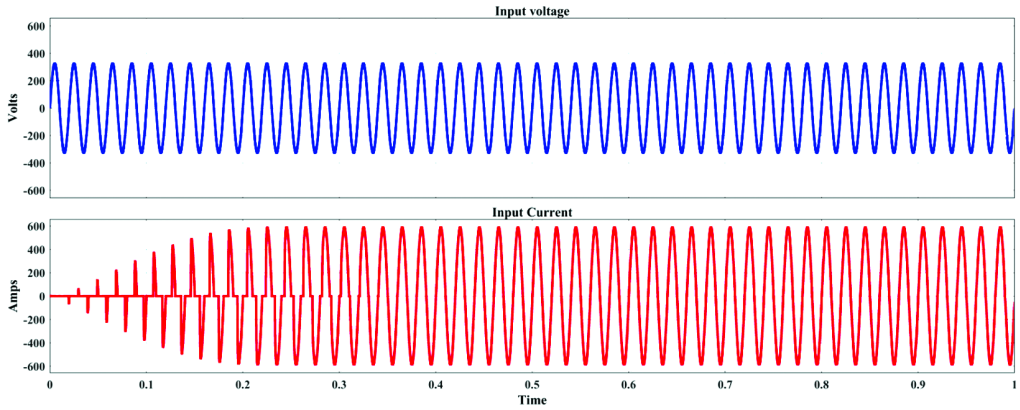

Fig. 19 — Input Voltage and Input Current with SCR in LF leg

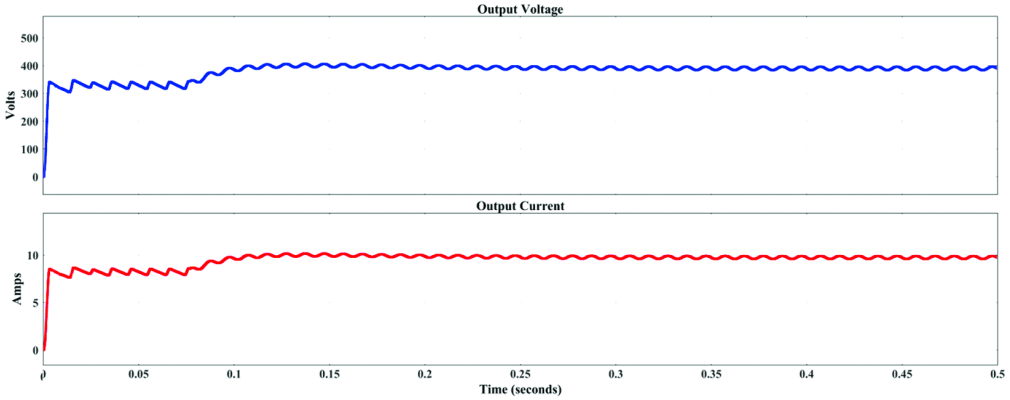

Fig. 20 — Output Voltage and Output Current with Diode in LF leg

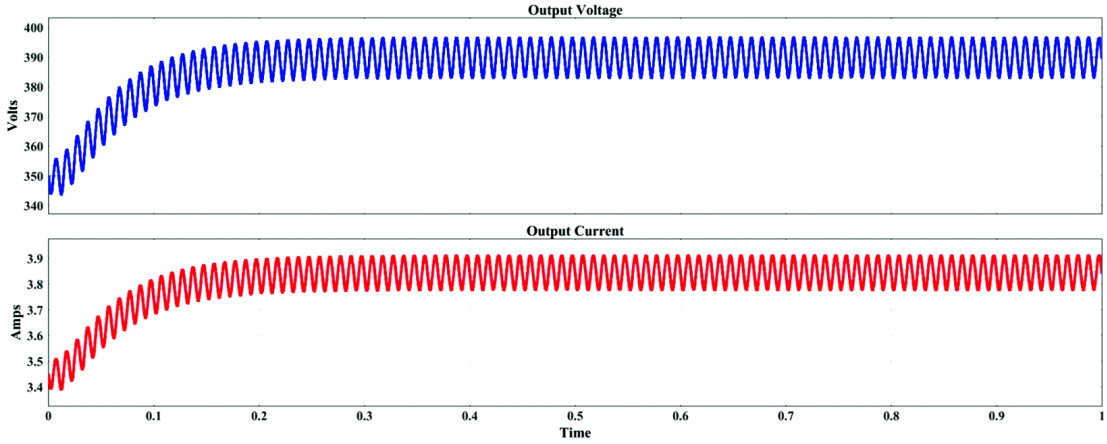

Fig. 21 — Output Voltage and Output Current with Mosfet in LF leg

which is expected to coincide with efficiency enhancement.

In Fig. 23, shows initially charging the capacitor, the load currents of the inductors 1 (blue) and 2 (red) display regulated ramp-up with limited peaks (almost 30 A) and demonstrates the practicality of SCR soft-start in eliminating inrush (by half of diode).

At steady state, triangular waveforms appear on the currents at 100 kHz, the averages are in the direction of the input reference and the average ripple (under 8 percent) is a measure of the CCM and low stress operation shown in Fig. 24. These results imply that the SCR has the strength of reducing the recovery

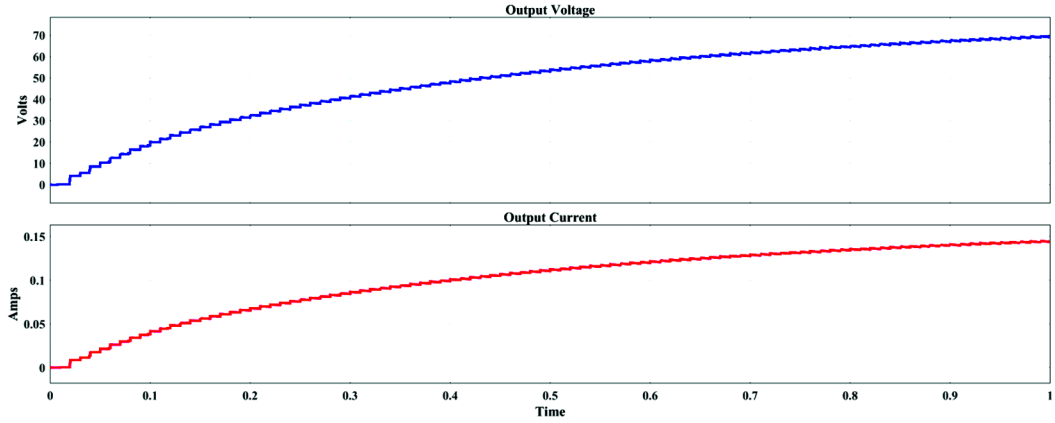

Fig. 22 — Output Voltage and Output Current with SCR in LF leg

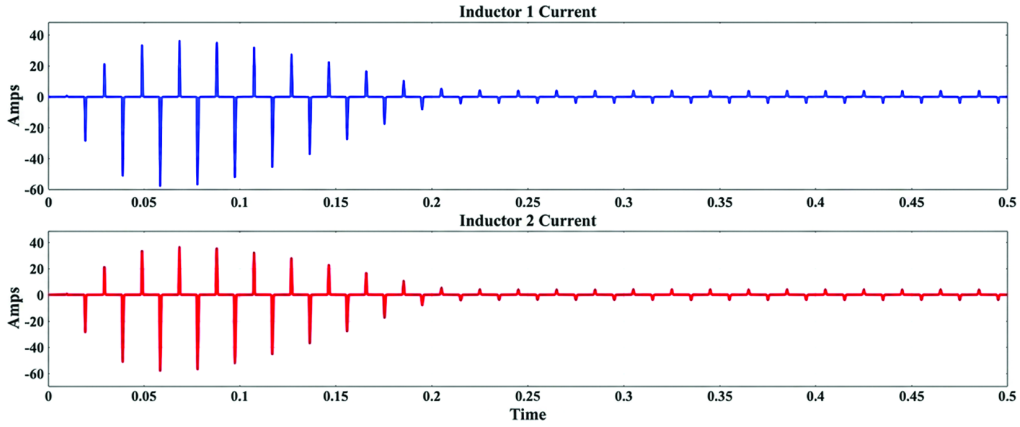

Fig. 23 — Inductors Current with SCR in Low Frequency Leg during capacitor charging

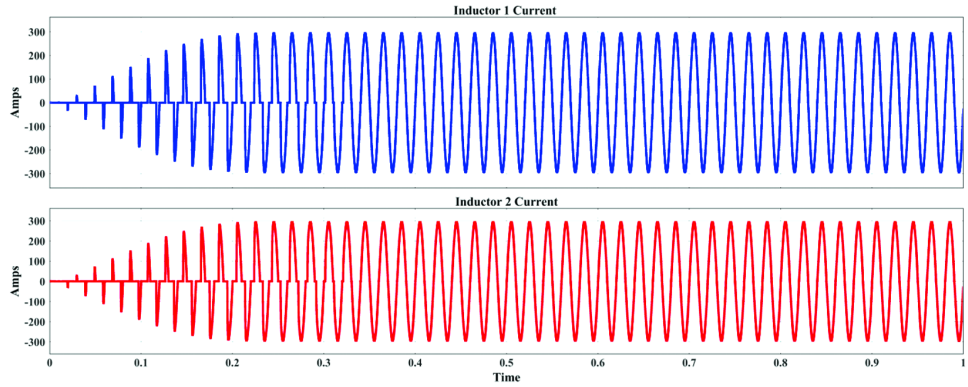

Fig. 24 — Inductors Current with SCR in Low Frequency Leg when capacitor gets charged

losses, THD and equal MOSFET efficiency of the old models[13]. Further extensions of these to apply to EVs are interleaved totem-pole extensions (discussed below).

Table 4 shows Comparative Performance of Totem-Pole PFC with Different LF Devices compares the performance of the Totem-Pole PFC topology by using different low frequency (LF) devices such as Diode, MOSFET and SCR. The Diode version has a power factor of 0.98, a THD of about 5 %, a high switching stress, and an output voltage ripple of less than 2 % and an efficiency of 95 % approximately. The MOSFET version enhances the results by having a power factor of 0.99, THD of approximately 3 %, a

Table 4 — Comparative performance of Totem-Pole PFC with different LF devices

LF Device	Power Factor (PF)	THD (%)	Efficiency (%)	Switching Stress	Output Voltage Ripple
Diode	0.98	≈5	≈95	High	<2%
MOSFET	0.99	≈3	≈97	Medium	<1%
SCR	0.995	≈2	≈98	Low	<1%

97 % efficiency, medium switching stress, and ripple less than 1%. Overall, the SCR configuration offers the highest power factor (0.995), THD (≈2 %), efficiency (98 %), low switching stress and low output voltage ripple (<1 %). This comparison shows the incremental benefits of substituting MOSFETs for diodes and then SCRs for MOSFETs in totem-pole configurations leading to improved efficiency, lower harmonics and reduced stress with excellent power quality.

7 Comparative Analysis

The graph in Fig. 25 shows the power factor (PF) of six power factor topologies, and PF is a measure of the efficiency of the AC power conversion into useful work (ideal value of 1.0). The losses are higher for the conventional Boost PFC and thus shows the least performance at ~ 0.96. With ripple reduction, the Interleaved Boost PFC gets a great lift to ~0.99. The variants of the Totem-Pole PFC (MOSFET) and (SCR) recover to ~0.99, being more efficient as they do not need the bridge, while the Totem-Pole PFC (Diode) dip slightly to ~0.98. The best performance is obtained by the Interleaved Totem-Pole PFC (SCR), with a close to perfect unity PF of ~1.00. As a whole, the graph shows a general trend of performance improvement, as topologies evolve from simple boost to more complex and interleaved bridgeless designs, which allow for more efficient operation, reduced harmonics, and improved power quality for modern systems.

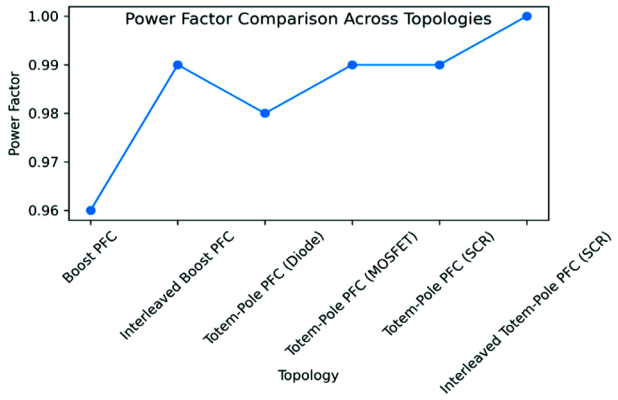

Fig. 25 — Power Factor Comparison

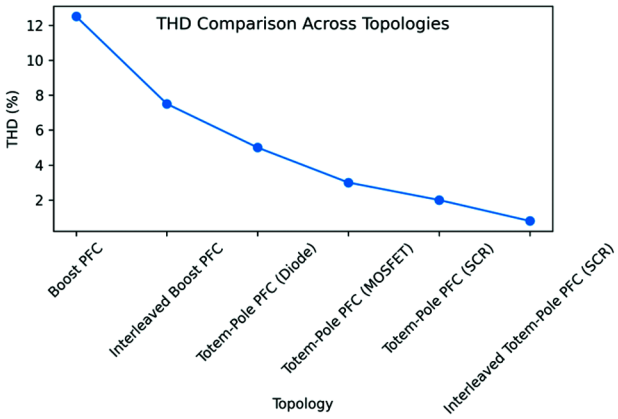

Fig. 26 — THD Comparison

The graph in Fig. 26 "THD Comparison Across Topologies" presents the Total Harmonic Distortion (THD) performance of the same six PFC topologies as presented above, with lower THD percentages being better with a reduction of the harmonic content injected into the AC grid. The conventional Boost PFC, which is designed to be simple and has higher current distortion, has the worst harmonic performance at 12 % or above. The ripple cancellation achieves a remarkable ripple reduction for the

Interleaved Boost PFC around 7.5 %. The benefits of a bridgeless design and more effective switching devices continue to decrease THD, now at approximately 5 % for the Totem-Pole PFC (Diode), about 3 % for the Totem-Pole PFC (MOSFET), and around 2 % for the Totem-Pole PFC (SCR). The optimal performance is obtained from the Interleaved Totem-Pole PFC (SCR) with performance around 1 %, close to the ideal harmonic suppression. In summary, the graph shows a clear downward slope, indicating that the benefits of topologies with advanced interleaved structures in terms of power quality are quite significant, allowing for easier compliance with harmonic standards and better support for high-efficiency applications such as data center systems and EV charging.

Figure 27, titled "Efficiency Comparison Across Topologies," shows the efficiency results of the 6

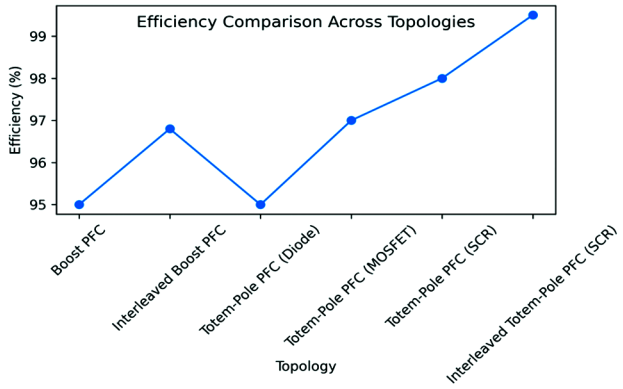

Fig. 27 — Efficiency Comparison

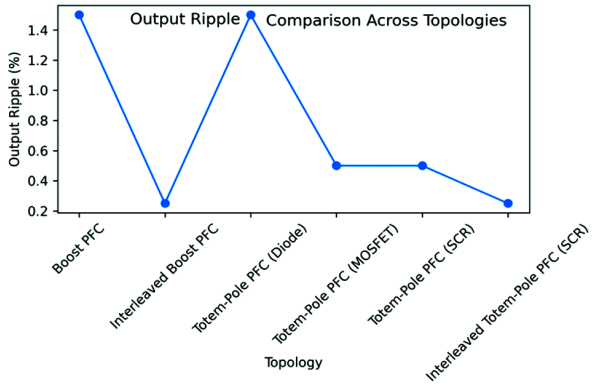

Fig. 28 — Output Ripple Comparison

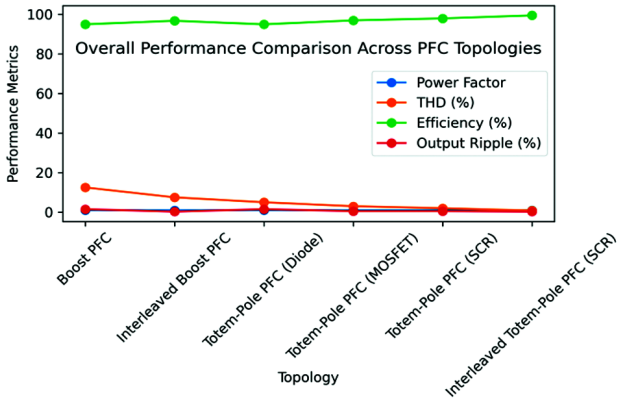

Fig. 29 — Overall Performance Comparison

PFC topologies, with the percentage showing how efficient the whole system can be in terms of reducing losses in the system. The conventional Boost PFC begins around 95 %, which is the lowest efficiency as it has higher conduction and switching losses. Ripple reduction and current sharing are realized to achieve an improvement of the Interleaved Boost PFC to nearly 96.8 %. There is a noticeable drop in efficiency at 95 % at the Totem-Pole PFC (Diode) where the diode reverse recovery losses, and then increasing with the Totem-Pole PFC (MOSFET) at ~97 % with synchronous rectification. It keeps climbing up to ~98 % for the Totem-Pole PFC (SCR) and to ~99.4 % for the Interleaved Totem-Pole PFC (SCR); with the combination of bridgeless design, interleaving and the low-loss SCR devices. Overall, the graph shows an increasing trend of efficiency at the more advanced topologies, revealing that the newer interleaved bridgeless designs have lower losses, better thermal efficiency, and higher power density for use in server PSUs, EV chargers, and other applications.

The graph Output Ripple Comparison Across Topologies in Fig. 28, shows the comparison of output voltage ripple percentage for the six PFC topologies, with lower ripple percentages representing a more stable output voltage with less need for large output capacitors. The ripple of the conventional Boost PFC is high about 1.45 %. The Interleaved Boost PFC produces a tight ripple of only ~0.25 % thanks to the use of phase-shifted operation and ripple cancellation. Interestingly, the Totem-Pole PFC (Diode) spikes up to ~1.45 %, probably because of diode switching characteristics, before decreasing to ~0.5 % with Totem-Pole PFC (MOSFET) and a similar value for the Totem-Pole PFC (SCR) with improved synchronous and low-loss switching. The most efficient performances are obtained by the SCRs (Interleaved Totem-Pole PFC): with an interleaving benefit and also with a bridgeless efficient design, about 0.25 % is obtained. Overall, the plot shows that using interleaving is critical to reduce output ripple, and the more sophisticated topologies can provide much smoother output DC than can the more basic topologies, leading to more reliable system operation and reduced size and cost of filtering components in high-performance power supplies.

The results of the overall performance for the six PFC topologies are plotted in a single graph as shown in Fig. 29, where four important performances such as Power Factor (blue), THD (orange), Efficiency (green), and Output Ripple (red) are compared. The results of the conventional Boost PFC are the worst among all the three with a low power factor (~96 %), high THD (~12 %), low efficiency (~95 %), and high output ripple. As the topologies evolve, significant enhancements become apparent: The Interleaved Boost PFC not only achieves a higher efficiency, but also significantly lowers THD and ripple. There is some compromise in some parameters for the Totem-Pole PFC (Diode), but the variants coming after, the

Table 5 — Overall comparative performance across topologies

Topology	LF Devices	PF	THD (%)	Efficiency (%)	Output Ripple (%)
Boost PFC	NA	0.95-0.98	10-15	≈95	<2
Interleaved Boost PFC	NA	>0.99	5-10	≈96.8	<0.5
Totem-Pole PFC	Diode	0.98	≈5	≈95	<2
Totem-Pole PFC	MOSFET	0.99	≈3	≈97	<1
Totem-Pole PFC	SCR	0.995	≈2	≈98	<1
Interleaved Totem-Pole PFC	SCR	0.999	<1 – 0.5	>99	<0.5

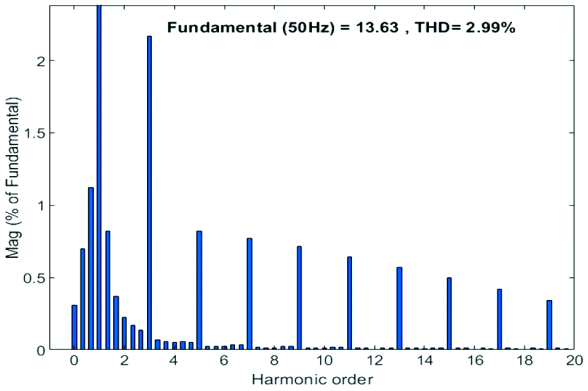

Fig. 30 — THD analysis of Totem-Pole PFC

MOSFET and SCR, make progress. The Interleaved Totem-Pole PFC (SCR) has the most optimal performance characteristics, having a power factor very close to unity (PF~100 %), a THD of almost zero (THD~1 %), a peak efficiency of almost 100 % (PF~99.5 %) and the lowest output ripple (OR~0.25 %). In conclusion, the graph shows a clear trend towards better power quality, efficiency, and stability for advanced interleaved bridgeless topologies, which are suitable for high-performance and high-density power conversion applications.

After analyzing all the PFC topologies, indicates that the Totem-Pole PFC, achieves minimum THD around 3 % as shown on Fig. 30.

8 Conclusion

The steady rise of comparative performance as illustrated in Table 5 results demonstrate the obvious development of traditional single-stage boost PFC converters to the modern bridgeless and interleaving topologies with the optimized low-frequency (LF) devices. The single-stage boost PFC has the worst THD around 10-15 % and the lowest efficiency ~95 %, as it has diode bridge losses and large input current ripple 20-30 %. 2-4 phase Interleaved boost converters also achieve lower ripple 5-10 %, THD 5-10 %, and better efficiency up to 96.8-97.5 % which is also applicable in medium power EV charging systems. The bridgeless totem- pole PFC is also better as it removes the diode bridge losses. Diode-based LF designs and MOSFET-based LF legs are more moderate and high-efficiency between 95-98 % and low THD between 3-5 % and low-ripple between 8-15% LF devices, respectively. The best performance has been found with the interleaved totem-pole PFC with an SCR in the LF leg, with PF = 0.999, THD ~1-0.5 %, efficiency ~99 % and ripple = about 5-6 %, which is suitable in high-power (>3 kW) Level 2 EV onboard chargers. Although the totem-pole PFC with SCR in the LF leg has performance benefits but it has more complexity, due to use of more component its design cost is also high and it provides high efficiency only at low-medium power load. At high power, there are thermal management issue exist, research are needs to be done on this. Future work will extend by simulating the whole schematic which include EMI filter, power stage, gate driver, controller design, and with current, voltage and temperature sensing in LTspice or Simplis and will Validate the proposed model with hardware testing on a OPAL-RT platform.

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