Indian Journal of Pure & Applied Physics
Vol. 64, June 2026, pp. 674-681
DOI: 10.56042/ijpap.v64i6.29233

Enhanced RF Performance Using Trench-Based Junctionless FET: Design and Analytical Study

Manoj Singh Adhikari[a], Raju Patel[b*], Chandramauleshwar Roy[b], Yogesh Kumar Verma[c] & Manoj Kumar Shukla[d]

[a]Department of Computer Science and Engineering, Graphic Era Hill University, Haldwani, Uttarakhand 263 139, India

[b]School of Electronics Engineering, Vellore Institute of Technology, Chennai 600 127, India

[c]School of Electronics & Electrical Engineering, Lovely Professional University, Phagwara, Punjab 144 411, India

[d]Department of Robotics and Automation, Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune 412 115, India

Received: 28th February 2026; accepted: 20th April 2026

To enhance the analog/RF performance, a dual-channel trench based junctionless FET (JLT) is being proposed. The planned structure's gate is set in a vertical trench, with two channels cut out on either side of it. HJLT and MJLT, the heavily and moderate doped drain concentrations for the suggested device, are explored correspondingly. The devices' performance parameters are assessed and contrasted with respect to drain current (I_D), unity-gain cut-off frequency (f_t), transconductance (g_m), and maximal oscillation frequency (f_{max}) in a TCAD tool (ATLAS) through 2D numerical simulations. As a result, the suggested topology makes sense for analog and radio frequency applications. At 20 nm gate length, the proposed HJLT is shown to provide f_{max}, f_T, and peak g_m of, 2300 GHz, 580 GHz, and 2710 μS/μm respectively. As a result, the suggested topology makes sense for analog and radio frequency applications.

Keywords: Dual-channel, Junctionless FET, Cut-off frequency, Transconductance

1 Introduction

JLFETs are easier to fabricate and function better than conventional FETs, they have been the subject of extensive research over the past ten years[1-9]. Nevertheless, because of their somewhat doped source/drain (S/D) regions, JLFETs have a high S/D resistance which decreases the value of ON-state current, hence slow down the device's speed[10-12]. JLFETs consist of strongly doped regions of S/D have been offered as a solution to this problem[13-18]. These devices are known as pseudo-junctionless transistors because high-low doping junctions are formed at the interfaces of drain-channel and source-channel regions. Furthermore, when compared to inversion-mode FETs, JLFETs show improved durability against the hot carrier effect, reduced ON-resistance, and higher mobility [10, 19].

In today's era maximum of the research for JLFETs has focused on low power digital circuits[10, 16, 20–26], several studies[7, 15, 17, 27-30] show that JLFETs are also suitable for analog/RF applications. Upon examining a bulk conventional JLFET, the measured frequency (f_t @ 52 GHz) and the peak transconductance (g_m @ 350 μS/μm) at 20 nm gate length (L_G) was reported[31]. The analog/RF performance were observed[30] for double-gate (DG) JLFETs to achieve a f_t of 51 GHz, a maximum g_m value is 162 μS/μm, and the obtained maximum oscillation frequency (f_{max}) value is 35 GHz. A new DG-JLFET introduced[29] to get the value of f_{max} is 214 GHz, g_m is 197 μS/μm, and f_t is 92 GHz. A DG-JLFET was reported[32], and it was observed that device's RF characteristics are superior for an optimized doped channel in contrast to an extremely doped channel. In order to enhance the DG-JLFET's RF performance with strongly doped S/D sections so adjusted the spacer area width and doping of the channel[27]. At 20 nm length, the achieved f_{max} of 450 GHz, maximum g_m value is 530 μS/μm, and obtained frequency f_t is 240 GHz.

In this work, a novel JLFET structure is introduced to enhance analog and RF performance. The proposed JLFET features a single gate positioned within a vertical trench, with dual channels situated on either side of the gate. The trench gate structure enhances gate control by increasing the gate-channel interface area and providing stronger electrostatic coupling. The dual-channel trench-gate structure improves electrostatic control of the gate over the channel by surrounding the channel more effectively. The trench

*Corresponding author: E-mail: raju.patel@vit.ac.in

gate allows the gate electric field to control the channel from multiple sides, which enhances carrier modulation and suppresses short-channel effects compared to a conventional single-channel junctionless FET[1, 3]. The device is investigated under both moderate and heavy drain doping conditions, leading to two variants: the moderately doped drain dual-channel JLFET (MJLT) and the heavily doped drain dual-channel JLFET (HJLT). Using dual-material (high work-function) gates improves electrostatic control and enhances transconductance. Optimization of spacer width and use of high-k spacers reduces parasitic capacitances, thereby improving cut-off frequency[33-34]. Proper selection of channel doping enhances mobility and balances g_m, improving RF efficiency. Techniques such as heavily doped source/drain regions and optimized contacts reduce series resistance, significantly improving f_t and $f_{max.}$ Reducing gate length improves RF performance; however, this must be balanced with short-channel effects. High-k gate oxides improve gate capacitance control and reduce leakage, enhancing high-frequency response. Although trench structures can increase fabrication complexity slightly, they significantly improve device performance, which can justify the additional fabrication effort. Using the TCAD simulator (ATLAS)[35] for 2D simulations, the RF as well as analog performance parameters of both variants were analyzed and compared. The HJLT demonstrates a peak value of transconductance is 2710 μS/μm, a cutoff frequency is 580 GHz, and an oscillation frequency value is 2300 GHz at 20 nm gate length, which acts as a more capable candidate for RF and analog applications.

2 Device Structure

Figure 1 depicts the proposed JLFET which is realized on silicon-on-insulator (SOI) in a 2D cross-sectional view. The structure's gate is set in a vertically placed trench, with heavily doped channels of N^+-type situated on either side of it. The drain connection is obtained from the device's N^+/N^{++} Si-region that is positioned above the buried oxide layer known as BOX, and the source contacts are positioned on uppermost of the channels. The channel thickness (t_c) is decided thin enough with M1 has a metal gate work function of 4.9 eV, whereas M2 has a work function of 4.5 eV i. e. the electric field (E_F) of a gate permeates the whole thickness as well as the volume depletion is obtained under the OFF state. Under the ON state both channels are driven simultaneously by an applied positive gate voltage (V_{GS}) from complete depletion region to fractional depletion region and at the end reached to the flat-band state. The superiority of ohmic contact edges is deteriorated at the S/D channel, although a lesser doped area of channel can be readily depleted at small field intensity[9]. Hence, improved ohmic contact at S/D conductors necessitates a highly doped channel. Hence, the device's drain current (I_{DS}) increases and the series resistance decreases.

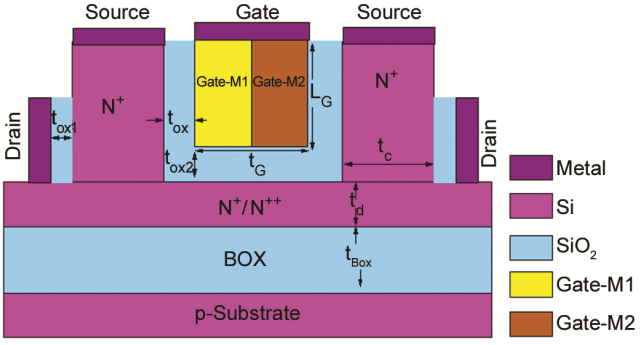

Fig. 1 — Structure of the proposed JLT

In MJLT, the drain layer doping is the same as the channel doping. The MJLT's increased parasitic series resistance for channels with moderate doping restricts I_{DS}, which ultimately lowers RF and analog performance. Higher drain doping concentration reduces series resistance and improves carrier injection efficiency. This increases the I_D, g_m, and improves high-frequency parameters such as f_t and f_{max}. The heavily doped drain reduces resistive losses by increasing the number of charge carriers. So enhance the current flow, higher g_m, and consequently higher f_t. To find the solution for this, the drain layer of HJLT is heavily doped (10^{20} cm^{-3}). With the proposed method decreases the value of series resistance of drain, which results in improved RF and analog parameters, and higher I_{DS} in comparison to the MJLT. In addition, the HJLT differs from a lateral JLFET with high-low doping junctions at the interfaces of source and drain channel by having just one high-low doping junction at the drain-channel interface. Furthermore, the channel's extension alongside the oxide thickness (t_{ox2}) blocks the N^{++} drain layer from approaching the gate edge, which lowers the parasitic capacitance and improves RF performance[28, 30]. Increasing t_{ox2} reduces fringing electric fields and parasitic capacitances around the gate. This reduction improves high-frequency performance and increases the f_{max}. Table 1 contains a list of all the structural characteristics of both devices.

Table 1 — Device parameters for the study

Parameters	Unit	Values
N^+ drain region doping (MJLT)	cm^{-3}	10^{19}
N^{++} drain region doping (HJLT)	cm^{-3}	10^{20}
Gate length (L_G)	nm	20-60
Width of Gate (t_G)	nm	5
Channel thickness (t_c)	nm	5
BOX thickness (t_{BOX})	nm	400
Drain thickness (t_d)	nm	10
Oxide thickness (t_{ox})	nm	1
Oxide thickness (t_{ox2})	nm	5
Oxide thickness (t_{ox1})	nm	20
Channel doping (N^+)	cm^{-3}	10^{19}

To enhance the suggested DCJLTs' RF performance, these parameters are optimized. The effects of varying the gate length (L_G) and channel doping (N_D) on device performance are investigated.

The device simulator (ATLAS) is used for the study of 2D simulations[35], the suggested devices are analyzed by calling on the right models to produce behavior that is extremely similar to that of a real device. Including mobility models, quantum confinement models, bandgap narrowing models, and Shockley–Read–Hall recombination models. These models are required to accurately describe carrier transport, recombination mechanisms, and quantum effects in nanoscale devices. To explain the carrier generation and recombination phenomenon, the Shockley-Read-Hall model is used. Concentration and field dependent mobility are computed using the Lombardi (CVT) model. The consequence of high doping concentration is included in the FermiDirac model by activating it. High doping effects on a semiconductor's bandgap are taken into account by the bandgap narrowing (BGN) model. Furthermore, the quantum confinement of carriers is simulated by using the quantum model. The experimental data of a JLFET was used to calibrate the aforementioned simulation models. As illustrated in Fig. 2, using ATLAS simulator JLFET is realised, and the transfer characteristic of experimental data is compared against the simulation result. It is noted that there is a good fit between the measured data and the simulated curve. Additionally, the fabrication chart detailing the sequential process steps, in concordance with the fabrication methodologies reported in[36–38], is provided in Fig. 3.

3 Simulation Results

The resistance of a JLFET, a voltage-controlled resistor, is determined by the difference in the work

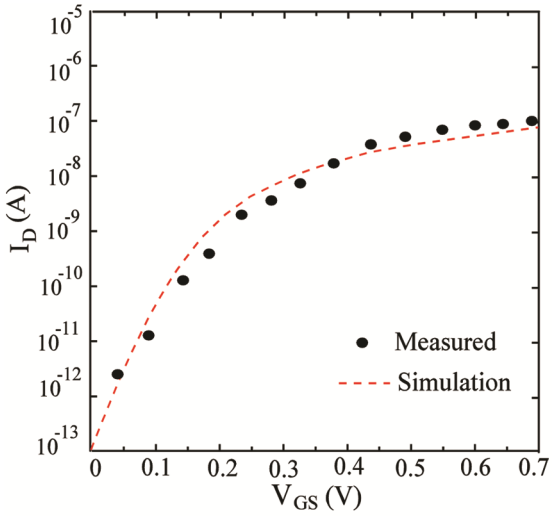

Fig. 2 — Calibration of simulation with experimental JLFET[6]

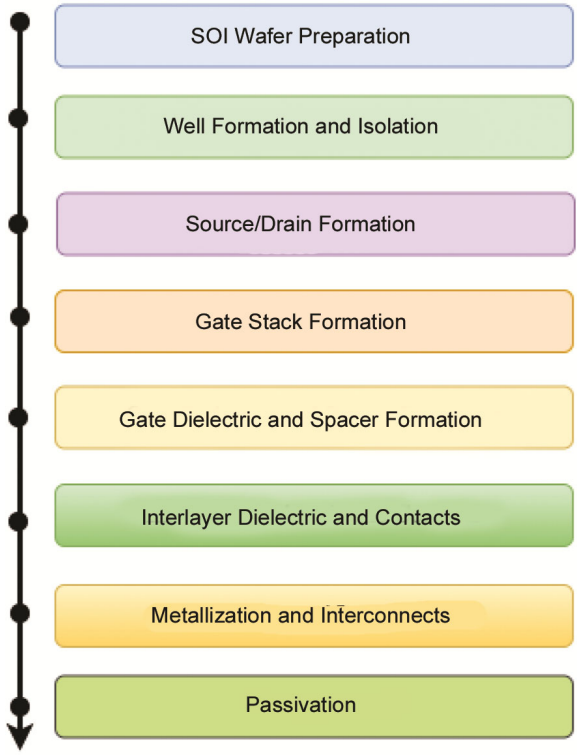

Fig. 3 — Fabrication steps for the proposed device

function (W_f) between the semiconductor channel and the gate electrode. It takes a large enough gate metal W_f to completely deplete the channel in the off-state. A positive V_{GS} is applied to an n-channel JLFET in order to partially deplete or fully neutralize the channel[11]. The proposed structures' channel depletion can be comprehended through the utilization of energy band diagrams and potential contours in both the ON and OFF states. The potential contour in the

drain layer and channel of the MJLT and HJLT at V_{DS}=0 V and V_{GS}=0 V (OFF-state) is shown in Fig. 4. It is evident that the full depletion condition during OFF state is indicated by the variation in potential in the channels of MJLT and HJLT. This is further supported by the energy band profiles of the MJLT and HJLT, which are shown in Fig. 5 at a cutline M (as seen in Figure 4) in the channel's center along its thickness when the device is in the off-state. Inside the drain layer the potential is almost constant, indicating that this area is not completely depleted. It is significant to observed that the additional controlling of the gate electrode in the channel occurs due to the effective gate length ($L_{eff} = L_G+t_{ox2}$) in the proposed structures is greater than the physical gate length (L_G). Furthermore, greater depletion spreading towards the drain side in the MJLT at lesser doping increases L_{eff}, whereas in the HJLT, due to the high doping of drain region, it is limited to L_G+t_{ox2}. This strengthens the HJLT structure's scalability. The HJLT exhibit lower L_{eff} compared to the MJLT. This is due to the heavily doped drain region reduces the depletion region extension near the drain side, which effectively shortens the channel length. A shorter effective channel reduces gate capacitance (C_{GG}) and improves carrier transport speed, resulting in better RF performance.

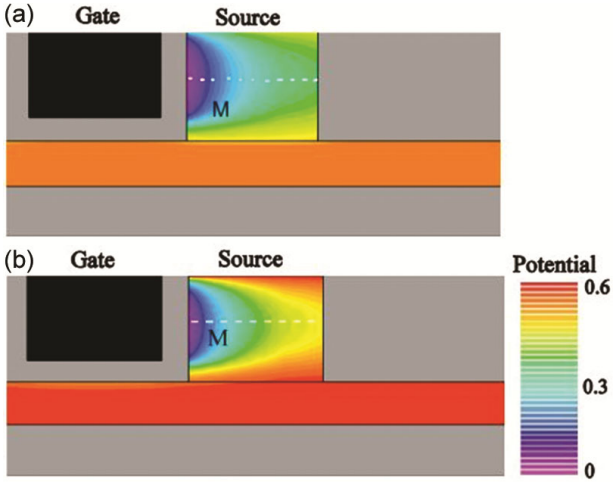

Fig. 4 — Potential contour in (a) MJLT (b) HJLT devices in OFF-state

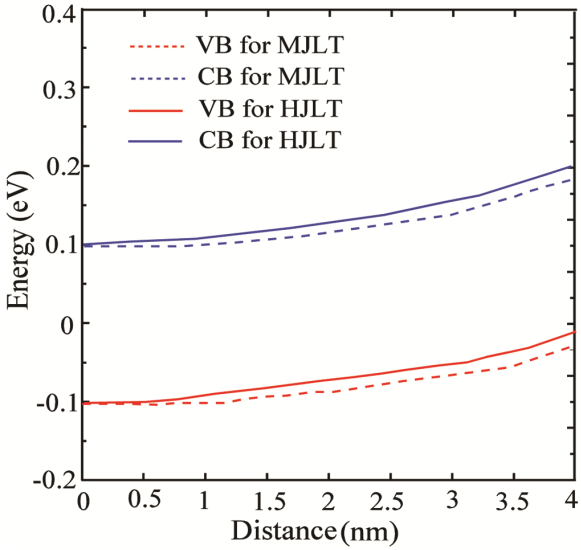

Fig. 5 — Energy band diagram of MJLT and HJLT devices along a cutline M (depicted in Figure 4) in OFF-state

The potential variation along the drain layer and channel for MJLT and HJLT devices under ON-state biasing conditions (V_{DS} = V_{GS} = 1 V) is depicted in Fig. 6. The almost flat-band state of the MJLT and HJLT is indicated by the observation of nearly constant channel potential. The energy band profile in Fig. 7 is shown at a cutline N (depicted in Figure 6) under ON-state conditions further supports this.

The proposed devices RF and analog performance parameters are assessed in terms of I_{DS}, g_m, total capacitance (C_T), f_t, and f_{max}. The output characteristics of the MJLT and HJLT at various V_{GS} values are displayed in Fig. 8. I_{DS} is observed to increase linearly with low drain bias (V_{DS}) and to saturate at large V_{DS} as a result of channel pinch-off brought on by induced drain side depletion. Because of the HJLT's heavily doped drain layer, which reduces series resistance, it exhibits higher I_{DS} than the MJLT. Furthermore, when compared to the MJLT, the HJLT shows better flatness of output characteristics at higher V_{GS} and a lower pinch-off

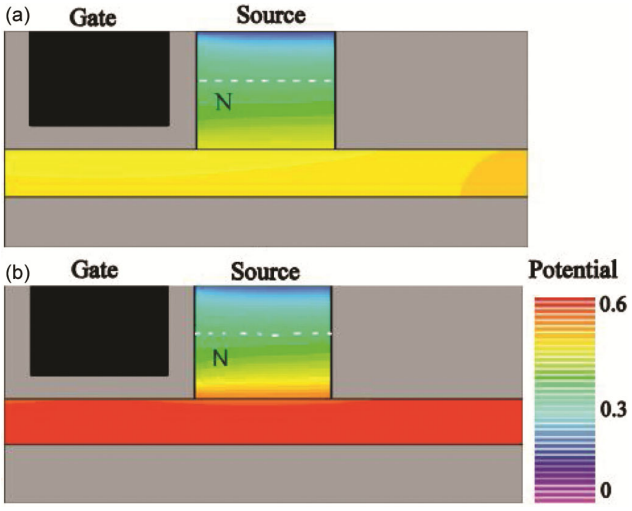

Fig. 6 — Potential distribution contour of (a) MJLT (b) HJLT Devices in ON-state

voltage. When the device is used as a small signal amplifier, this might be advantageous.

Figure 9 displays the transfer characteristics of the suggested devices. The figure makes it clear that the HJLT has higher I_{OFF} and I_{ON} currents than the MJLT. Transconductance is a crucial factor in assessing the device's performance in terms of RF and analog characteristics. Thus, Fig. 10 plots the g_m of the suggested devices. Both devices display high g_m values across a broad range of V_{GS}. The peak g_m of HJLT and MJLT are obtained to be 2710 μS/μm and 2611 μS/μm, respectively, at an L_G of 20 nm. Because I_{DS} is higher in the HJLT than in the MJLT, it offers a higher g_m. g_m represents the ability of the gate voltage to control the drain current. Higher g_m leads to higher current gain and improved high-frequency response. Since f_t is directly proportional to g_m, increasing g_m enhances RF performance.

The variation of g_m for MJLT and HJLT with L_G is shown in Fig. 10. Due to decreased gate control over I_{DS} and increased channel resistance, it is observed that g_m deteriorates as L_G increases. However, because

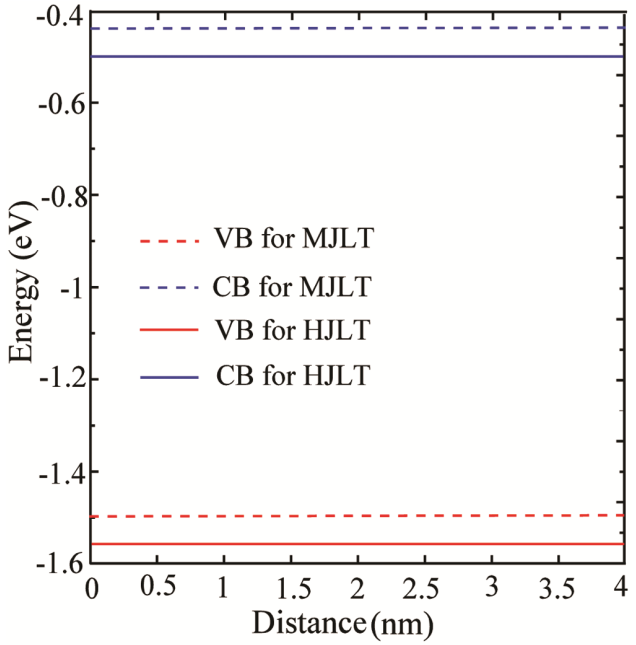

Fig. 7 — Energy band profiles of MJLT and HJLT Devices along a cutline N (depicted in Figure 6) in ON-state

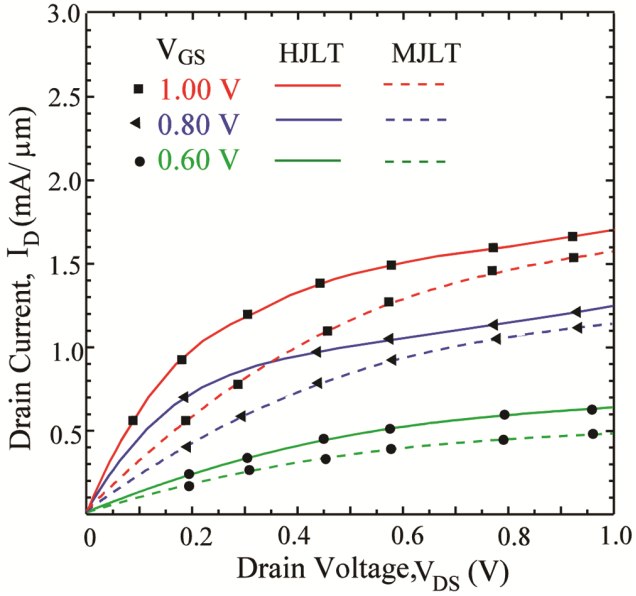

Fig. 8 — Output characteristics of MJLT and HJLT Devices

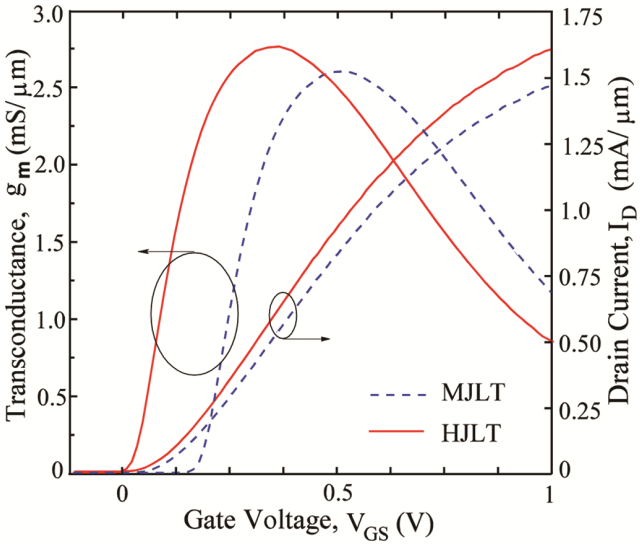

Fig. 9 — Transfer and Transconductance characteristics MJLT and HJLT Devices

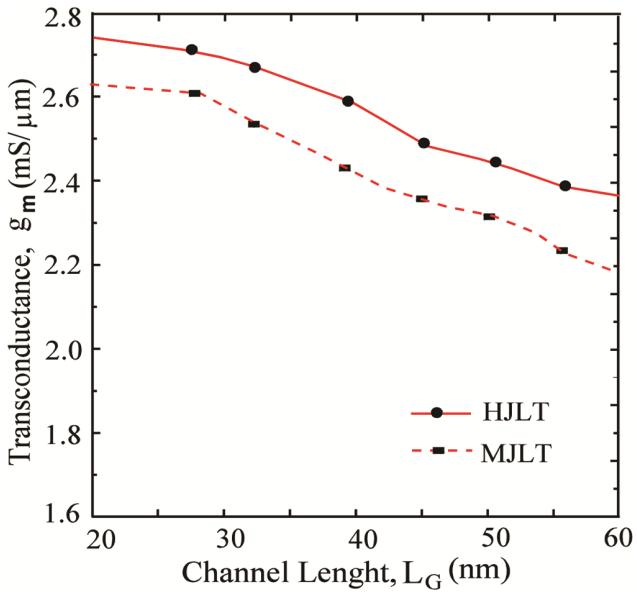

Fig. 10 — Variation of g_m of MJLT and HJLT with L_G

there is a greater decrease in I_{DS} than in g_m improves as L_G increases. For all L_G values, the HJLT shows a higher g_m than the MJLT.

The influence of N_d on the gain (g_m) of MJLT and HJLT devices is presented in Fig. 11. Both structures offer optimal control over the channel electrostatics and a notable enhancement in gain with rise in N_D as a result of higher drain current. The best control of the gate in this case implies that the dimensions of the device are optimized for channel doping of 1×10^{19} cm^{-3} in order to get the peak value of transconductance, since the proposed structure is intended for suitable analog and RF applications. Additionally, the HJLT shows superior g_m at higher N_d than the MJLT due to a greater increase in I_{DS} than in g_m. This is because the increase in series resistance has resulted in a significantly lower I_{DS} of MJLT.

The f_t and f_{max}, which are found using the following equations, are two crucial parameters for assessing a device's analog/RF performance.

$$f_t = \frac{g_m}{2\pi C_T} \quad \ldots (1)$$

$$f_{max} = \frac{g_m}{2\pi C_{GS}\sqrt{4(R_G + R_C + R_S)(g_m(\frac{C_{GS}}{C_{GD}}))}} \quad \ldots (2)$$

where C_{GS}, C_{GD}, C_T stand for gate-to-source capacitance, gate-to-drain capacitance, and total gate capacitance respectively. Source, Gate and channel resistances are denoted by the letters R_S, R_G and R_C, respectively. Higher g_m and lower C_T are what the device should offer in order to improve f_t. Figure 12 shows the C_T plot for the suggested structures. Utilizing AC simulations at 1 MHz frequency and a V_{DS} of 1 V, C_T is extracted for the devices. Because the channel's depletion region gradually decreases, it is observed that the C_T of HJLT and MJLT increases with V_{GS} up to 0.5 V and 0.55 V, respectively. As V_{GS} increases further, carriers build up in the channel, causing C_T to trend downward. When comparing the two devices maximum g_m points, V_{GS} of 0.8 V, the MJLT yields a significantly higher C_T than the HJLT. Because MJLT has a lower drain concentration than HJLT, it has a longer effective channel length, which accounts for its higher C_T.

The variation of unilateral power gain and short circuit current gain with frequency for MJLT and HJLT devices is presented in Fig. 13. The f_t and f_{max} are found at the intersection of @ 0 dB and the unilateral power gain with the x-axis, respectively. The gate material resistance (R_G) in this investigation is 86.7 Ω-μm. For MJLT and HJLT, the corresponding values of f_t are determined to be 415 and 580 GHz. The improvement in cut-off frequency f_t is mainly due to reductions in gate capacitance (C_{GG}) Lower capacitance values allow faster switching and higher operating frequency. C_{GG} for HJLT is 0.74 fF/μm and for MJLT 1.01 fF/μm. Stated differently, HJLT provides a 39.7 % improvement in f_t over MJLT. This increase in f_t is explained by HJLT's lower C_T and higher g_m. A 76.9 % improvement in f_{max} for HJLT is achieved when the values of f_{max} for MJLT and HJLT are found to be 1301

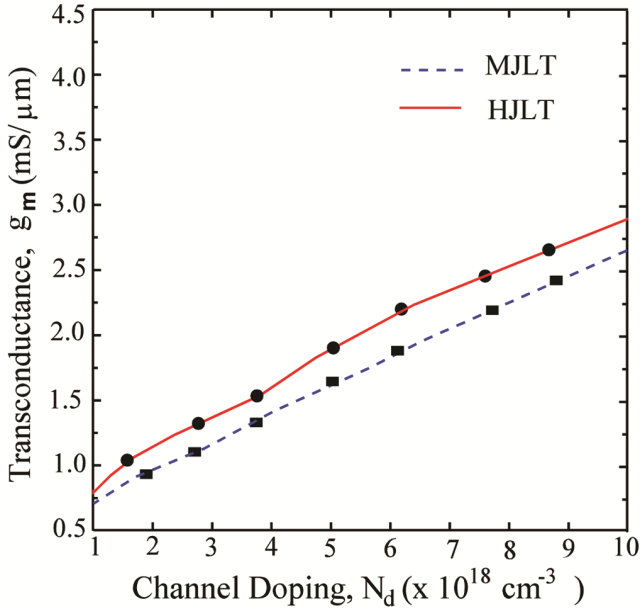

Fig. 11 — Impact of N_d on g_m of MJLT and HJLT Devices

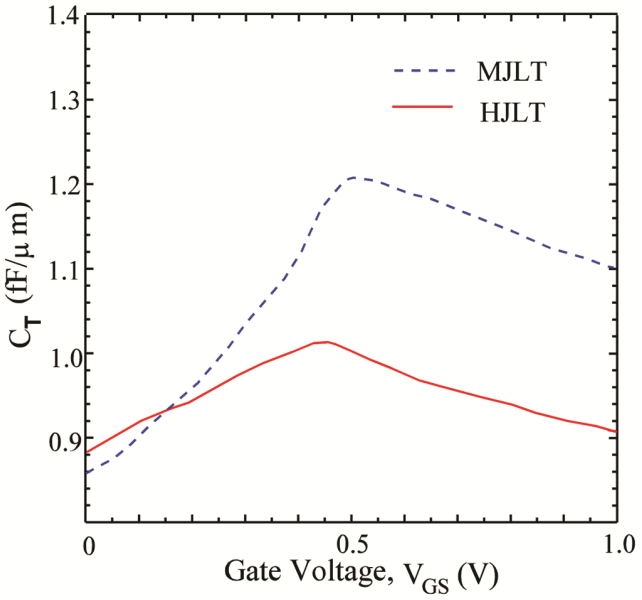

Fig. 12 — Variation of C_T with V_{GS} of MJLT and HJLT Devices

and 2300 GHz, respectively. The main parasitic elements include gate resistance, drain resistance, and gate-to-drain capacitance. The HJLT reduces these parasitic effects through improved channel conduction and reduced drain resistance due to heavy doping, which enhances f_{max}.

Plotting of f_{max} and f_t with L_G is shown in Fig. 14. The figure displays that for both devices, f_t decreases with L_G. This is because, with L_G, g_m decreases, and C_T rises. Similarly, for both structures, f_{max} decreases for higher values of L_G due to rise in parasitic resistances and a decrease in f_t. As L_G increases, carrier transit time through the channel becomes longer and channel resistance increases. So the higher capacitance and slower carrier transport, which reduces f_t and f_{max}. The impact of N_d on f_{max} and f_t for MJLT and HJLT is shown in Fig. 15. Because of the greater increase in g_m compared to C_T, so that f_t increases with N_D for MJLT and HJLT devices. In addition, the HJLT exhibits a growing tendency of f_{max} in relation to N_D because parasitic resistances are reduced more than capacitances are increased. However, the f_{max} of MJLT improves after declining to an N_D of 4×10^{18} cm^{-3}. This is because, at lower N_d, the rise in C_T predominates over the decline in parasitic resistances. For higher value of N_d (more than 4×10^{18} cm^{-3}), the increase in C_T is outweighed by the reduction in parasitic resistances.

The performance of the suggested structures is compared with comparable devices that have already been listed in Table 2. The proposed device consists

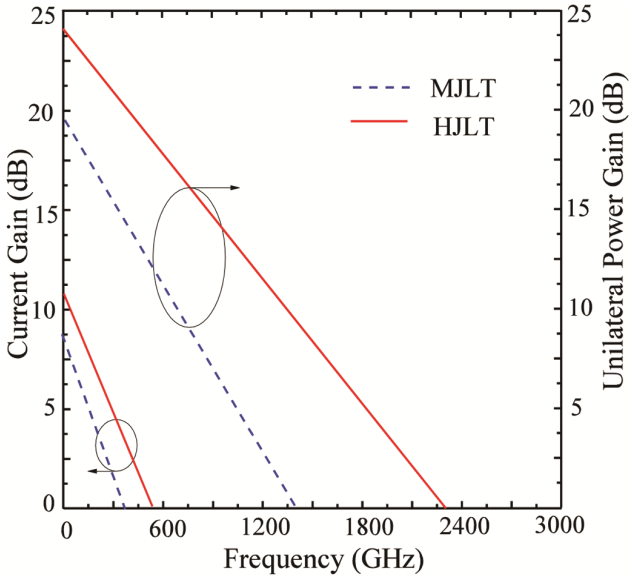

Fig. 13 — Dependence of f_t and f_{max} for MJLT and HJLT Devices

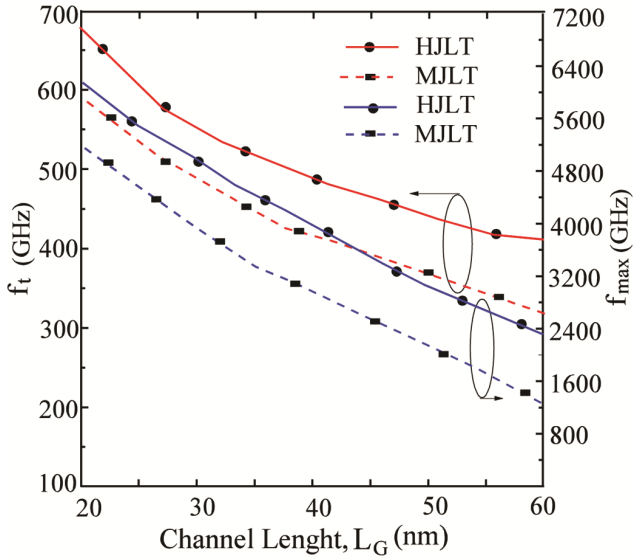

Fig. 14 — Plotting of f_t and f_{max} with L_G of MJLT and HJLT Devices

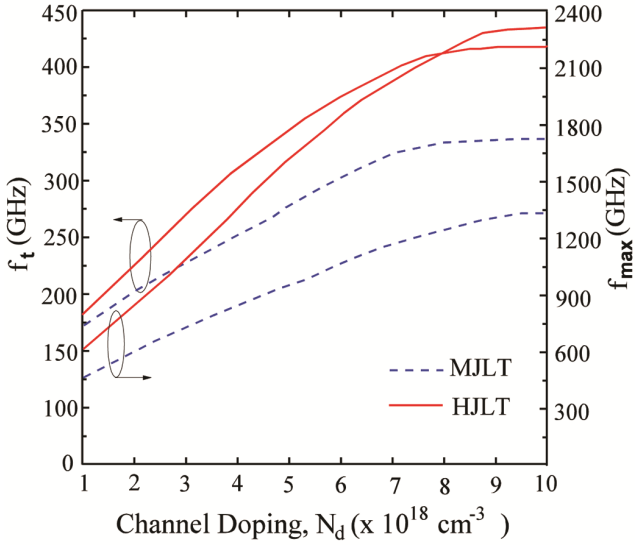

Fig. 15 — Effect of N_d on f_{max} and f_t of MJLT and HJLT Devices

Table 2 — Comparative performance analysis of different devices

Parameters	DG- JLT[27]	ULP-DG JLT[29]	DG-JLT[30]	HDD-DCJLT[1]	MJLT (This work)	HJLT (This work)
L_G (nm)	20	20	20	20	20	20
f_t (GHz)	240	92	51	548	415	580
g_m (μS/μm)	530	197	162	2304	2611	2710
f_{max} (GHz)	450	214	35	830	1301	2300

of a dual-channel conduction path, trench gate architecture, and a heavily doped drain region. These innovations improve gate control, reduce series resistance, and enhance carrier transport, leading to higher g_m, f_t, and f_{max}. Both suggested devices show a notable improvement in g_m, f_t, and f_{max}. The HJLT achieves a 5.1 times higher g_m, a 2.4 times improvement in f_t, and a 5.1 times enhancement in f_{max} in comparison to DG-JLT[27]. Considering this, the HJLT might be a better option for high-frequency and mixed-signal applications.

4 Conclusion

For analog and radio frequency applications, a novel JLFET structure (dual-channel trench-gate) has been introduced. The suggested device has been investigated with heavily doped (HJLT) and moderately doped (MJLT) drain regions using 2D simulations. Because the drain series resistance is lower in the HJLT than in the MJLT, it exhibits higher I_{DS} and g_m. C_T decreases as a result of HJLT's lower L_{eff}. When compared to MJLT, HJLT exhibits a significantly improved f_t and f_{max} due to its higher g_m and lower C_T. Furthermore, when compared to previously published JLFETs, the HJLT is shown to attain better RF (f_t, f_{max}) and analog (g_m) performance. A higher f_{max} means the device is suitable for high-frequency and RF communication applications. Thus, for analog/RF circuits, the suggested HJLT is a better option.

References

1 Garg A, Singh Y & Singh B, *Silicon*, 33 (2020) 65.
2 Lee C-W, Ferain I, Afzalian A, Yan R, Akhavan ND, Razavi P & Colinge J-P *Solid-State Electron*, 54 (2) (2010) 97.
3 Goel A, Rewari S & Gupta R S, *Micro Nanostruct*, 198 (2025) 208050.
4 Singh A P, Baghel, R K, Tirkey S & Kumar A, *Micro Nanostruct*, 205 (2025) 208187.
5 Colinge J-P, Kranti A, Yan R, Lee C-W, Ferain I, Yu R, Akhavan ND & Razavi P, *Solid-State Electron*, 33 (2011) 65.
6 Colinge J P, Lee C W, Afzalian A, Akhavan N D, Yan R, Ferain I, Razavi P, O'Neill B, Blake A, White M, Kelleher A M, Mccarthy B & Murphy R, *Nat Nanotechnol*, 5 (2010) 225.
7 Doria R T, Pavanello M A, Trevisoli R D, De Souza M, Lee C, Ferain I, Akhavan N D, Yan R, Razavi P, Yu R, Kranti A & Colinge J, *IEEE Trans Electron Devices*, 58 (8) (2011) 2511.
8 Garg A, Gola D, Singh B & Singh Y, *Physica Scripta*, 100 (3) (2025) 035029.
9 Gogoi M P, Saha R & Baishya S, *Physica Scripta*, 100 (3) (2025) 035021.
10 Sahay S & Kumar M J, *Junctionless Field-Effect Transistors: Design, Modeling and Simulation*, (John Wiley & Sons) 2019, p. 125.
11 Colinge J P, Lee C W, Dehdashti A N, Yan R, Ferain I, Razavi P, Kranti A & Yu R, *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*, (Heidelberg: Springer) 2011, p. 187.
12 Sarkar A, Das A K, De S & Sarkar C K, *Microelectron J*, 43 (11) (2012) 873.
13 Cho S, Kim K R, Park B & Kang I M, *IEEE Trans Electron Devices*, 58 (5) (2011) 1388.
14 Kim T K, Kim D H, Yoon Y G, Moon J M, Hwang B W, Moon D, Lee G S, Lee D W, Yoo D E, Hwang HC, Kim JS, Choi Y, Cho B J & Lee S, *IEEE Electron Device Letters*, 34 (12) (2013) 1479.
15 Jin X, Xi L, Wu M, Chuai R, Lee J-H & Lee J-H, *Solid State Electron*, 79 (2013) 206.
16 Holtij T, Graef M, Hain F M, Kloes A & Iniguez B, *IEEE Trans Electron Devices*, 61 (2) (2014) 288.
17 Chebaki E, Djeffal F, Ferhati H & Bentrcia T, *Superlattices and Microstructures*, 92 (2016) 80.
18 Bansal A K, Kumar M, Gupta C, Hook T B & Dixit A, *IEEE Trans Electron Devices*, 65 (8) (2018) 3548.
19 Rios R, Cappellani A, Armstrong M, Budrevich A, Gomez H, Pai R, Rahhal-orabi N & Kuhn K, *IEEE Electron Device Letters*, 32 (9) (2011) 1170.
20 Holtij T, Schwarz M, Kloes A & Iniguez B, *Solid-State Electronics*, 90 (2013) 107.
21 Singh B, Gola D, Singh K, Goel E, Kumar S & Jit S, *IEEE Trans Electron Devices*, 63 (6) (2016) 2299.
22 Singh B, Gola D, Singh K, Goel E, Kumar S & Jit S, *IEEE Trans Electron Devices*, 64 (3) (2017) 901.
23 Larki F, Dehzangi A, Islam M S, Ali S H, Abedini A & Majlis B Y, *Silicon*, 10 (2018) 1305.
24 Manikandan S, Balamurugan NB & Nirmal D, *Silicon*, 12 (2020) 2053.
25 Bavir M, Abbasi A & Orouji A A, *Silicon*, 12 (2019) 1593.
26 Darwin S & Arun Samuel T S, *Silicon*, 12 (2020) 393.
27 Ghosh D & Kranti A, *Semicond Sci Technol*, 30 (2015) 015002.
28 Garg A, Singh B & Singh Y, *AEU - Int J Electron Commun*, 118 (2020) 153140.
29 Ghosh D, Parihar M S, Armstrong G A & Kranti A, *IEEE Electron Device Letters*, 33 (10) (2012) 1477.
30 Sirohi A, Sahu C & Singh J, *IEEE Access*, 7 (2019) 141810.
31 Garike R & Patil G C IET Circuits, *Devices & Systems*, 13 (2018) 45.
32 Parihar M S & Kranti A, *Semiconductor Sci Technol*, 29 (7) (2014) 075006.
33 Kusuma R & Talari V K H R, *Silicon*, 14 (2022) 10301.
34 Raju V, Suresh E, Shashikanth B, Jagadeesh B, Srinivas A, Kumar T Ch A & Kumar N M, *Silicon*, 14 (2022) 10775.
35 ATLAS user's manual: Device simulation software *Silvaco Int Santa Clara CA* (2016).
36 Itoh T, Mauze A, Zhang Y & Speck J S, *Appl Phys Lett*, 117 (15) (2020) 152105.
37 Long W, Ou H, Kuo J M & Chin K K, *IEEE Trans Electron Devices*, 46 (5) (1999) 865.
38 Goyal P & Kaur H, *Silicon,* 15 (2023) 1597.