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Polar Resistors Asymmetric Semiconductor Structures as Linear Resistors with Different Resistances for Opposite Polarities

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Passive, two-terminal resistors, with linear current voltage relationships, but exhibiting different resistances for opposite polarities are introduced in this paper. Such resistors change their resistance when current direction through them changes. These are named polar resistors. Such polar resistance is observed in asymmetric semiconductor INI structures, where I is an abbreviation for intrinsic, and N is for n-type doped. Polar resistance is not material specific. Both Silicon and Gallium Arsenide polar resistors were simulated in this work. In a three-layered INI structure, for certain thicknesses of the intrinsic layers, it is observed that for positive voltage, voltage drops significantly across one intrinsic layer, and for negative voltage, voltage drops significantly across the other intrinsic layer. With different I-layer thicknesses polar resistance is achieved. A background mobile electronic concentration of 10^{11}/cc and 10^{12}/cc were assumed for Si, due to background doping, and 10^{7}/cc and 10^{8}/cc were assumed for GaAs. Metallic ohmic contacts to semiconductor intrinsic layers are difficult to fabricate. So doped n-type CdS and SnO_2 were used as contact enabling layers to Si and GaAs respectively. This implies the structure is NININ; i.e. N-CdS/I-Si/N-Si/I-Si/N-CdS and N-SnO_2/I-GaAs/N-GaAs/I-GaAs/N-SnO_2. In such devices, between -1V and +1V, polar resistance is observed and a rectification ratio up to 10 are demonstrated. The roles of the middle N layer and the n-type contact enabling layers are also discussed.

Keywords: Polar resistance, Polarity-dependent resistance, Semiconductor INI structures, Semiconductor NININ structures

1 Introduction

Ohm's Law depicts linear resistors and the proportionality of current and voltage. On reversing the voltage polarity across standard resistors the current reverses its direction but the resistance of the resistor does not change. The graph of current-voltage is a straight line in the first and third quadrant passing through the origin. A fundamental inquiry remains regarding whether the resistance can change when polarity (or, the current direction) changes. After an extensive search of the literature, no reports were found of a (piecewise) linear, two-terminal and passive electronic component whose resistance alters with polarity. This paper reports the simulation of such a device. Such resistors are named polar resistors. For these devices, the graph of current vs. voltage is two straight lines joining at the origin. The straight line in the first quadrant shows forward conduction and has a slope different from that of the other straight line in the third quadrant which shows reverse conduction. Figure 1 compares the current voltage curves (IV s) of a polar resistor with those of normal resistors and diodes.

A resistor conducts equally in both directions. A diode[1] conducts only in one direction. A polar resistor conducts in both directions but unequally. A polar resistor is not a "leaky diode". In the reverse direction a diode is non-conducting. A leaky diode will have a high reverse saturation current. This is an artifact of the device where the reverse current is not linear with voltage. This indicates a conduction different from resistors. In comparison, a polar resistor exhibits a controlled reverse conduction with a finite resistance. In the forward direction, the polar resistor has two distinct differences from the diode. Its IV is linear compared to that of a diode, which is exponential, and a zero (or near-zero) threshold to forward conduction. PN junction diodes show a threshold voltage of 0.6-0.7 V[1] and Schottky diodes have a threshold voltage of 0.2-0.4 V[1]. But the polar resistors are zero or near-zero threshold devices. So, a polar resistor would exhibit a smaller threshold voltage compared to a diode.

In comparison, other devices like the memristor[2,3] and the varistor[4,5] exist. A memristor has two resistance states between which it switches. It also shows hysteresis. A varistor, on the other hand, is a voltage-dependent resistor. At high voltage its

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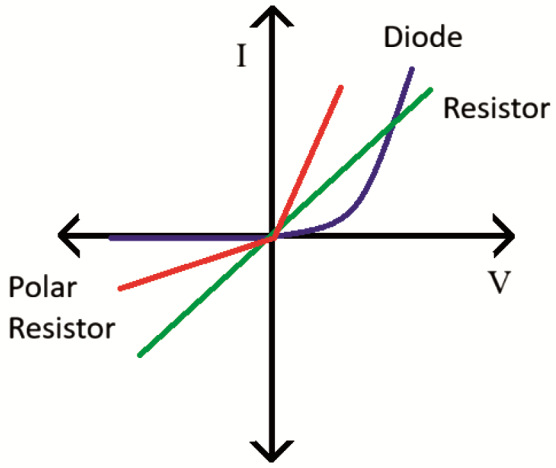

Fig. 1 — Schematic comparing the current voltage curves of a resistor, diode, and a polar resistor

resistance drops. Both the memristor and the varistor are different compared to a polar resistor.

Polar resistors are formally defined as electronic components that follow the Ohm's law V = IR. Here R is the electrical resistance of the device. IV curves are expected to be linear for each polarity, i.e. R is a number and is independent of V or I. For positive polarity, i.e. for V > 0, R = R_+. Similarly, for negative polarity, i.e. for V < 0, R = R_-. For a polar resistor, in general, $R_+ \neq R_-$. R_-/R_+ represents the rectification ratio of the polar resistor, assuming, without any loss of generality, that $R_+ < R_-$. In the special case, where $R_+ = R_-$, the device simply reduces to a linear resistor. In another special case, where $R_- >> R_+$, the device's IV is similar to that of a diode. Thus, in one extreme the polar resistor behaves as an ordinary resistor, and in another extreme it behaves like a diode.

The only instance, in the literature, where a device's IV is similar to the IV of a polar resistor, is ion current rectification in asymmetric nanochannels[6-10]. But, here, the device is ionic; not electronic. When ions flow through asymmetric nanochannels, which are often shaped like funnels, one direction of ionic current flow has more resistance than the other. For one polarity the nanochannel is depleted of ions and for the other it accumulates ions[6]. The accumulated nanochannel has lesser resistance than the depleted one. Thus, forward and reverse resistances are different.

Upon conducting a comprehensive survey for polarity dependent resistance in the literature, some devices are found which have been summarized below.

The first instance is of a bipolar memristor[11,12]. It exhibits two resistance states the high (HRS) and the low (LRS). The bipolar memristor switches from HRS to LRS at a positive threshold voltage; this is the SET process. It switches back from LRS to HRS at a negative threshold voltage which is the RESET process. So, the device shows two resistance states with different resistances and the switching between these resistance states is polarity dependent. But while crossing zero, the current voltage curve corresponds to either the LRS or the HRS. There is no change of resistance around zero crossing. So bipolar memristors are inherently different from polar resistors which have different resistances for opposite polarities. Bipolar memristors also show hysteresis. Such hysteresis is not expected in polar resistors. Bipolar memristors work by the directional migration of ions inside their structures.

Next are unipolar memristors[13,14]. Here also two distinct resistance states with different resistances (LRS and HRS) are exhibited. But the switching between these resistances is not polarity dependent. Both the SET (HRS to LRS) and the RESET (LRS to HRS) processes occur at the same polarity. So, they are also inherently different from polar resistors which changes its resistance when polarity is changed. Unipolar memristors also show hysteresis. They work via a thermal mechanism where transitions are driven by localized heat generation.

Self-rectifying memristors[15,16] show polarity dependent resistance similar to a diode. Like bipolar or unipolar memristors, self-rectifying memristors have a LRS and HRS and show hysteresis. But the main difference is in the ON state (LRS) the current voltage curve resembles that of a diode – supporting exponential conduction for positive polarity and suppressed conduction for negative polarity. In the HRS diode like behavior may persist but the current for both polarities is heavily suppressed. A self-rectifying memristor is closer to a polar resistor compared to bipolar or unipolar memristors. But still, the diode like IV curve is highly non-linear. For positive polarity the current is exponential and for negative polarity it is approximately flat. Polar resistors exhibit a (piecewise) linear IV curve; this distinguishes them from self-rectifying memristors. Self-rectifying memristors mostly use electric field to move ions inside their structures to form conductive channels under forward bias; under reverse bias these channels are weakened or broken.

Ferroelectric tunnel junctions (FTJ)[17,18] also exhibit polarity dependent resistance, but not polar resistance. FTJs consist of an ultrathin ferroelectric dielectric layer sandwiched between two electrodes. If the two electrodes are similar, a symmetric FTJ[17] results; if they are different, an asymmetric FTJ[18] results. An FTJ works due to a change in the polarization direction within the ferroelectric layer. This change mainly happens due to an applied voltage. Hysteresis is present in both symmetric and asymmetric FTJs. The IV curve of a symmetric FTJ is similar to a bipolar memristor, while the IV curve of an asymmetric FTJ is similar to a self-rectifying memristor. Similar to the self-rectifying memristor, an asymmetric FTJ exhibits a diode-like IV curve. So, an asymmetric FTJ does show polarity dependent resistance. But again, these curves are highly nonlinear. So, they are inherently different from the IV curves of a polar resistor.

Asymmetric Schottky contacts[19,20] also exhibit polarity dependent resistance. Such a device can be fabricated with two Schottky metal contacts, with different metals, on the either side of a semiconductor. If the contacts are fabricated with the same metals, the effect can still arise due to different contact geometries like different contact areas. Such a device often acts as an asymmetric back-to-back diode pair. It is asymmetric because the Schottky contacts are fabricated with different metals or have different geometries. Such a metal-semiconductor-metal device shows diode like rectification and hence an IV curve that has different resistances for opposite polarities; however, the IV curves, here, are highly nonlinear. This points out their inherent difference with a polar resistor which has separate linear IV curves for both polarities. Next, the polar resistor is compared with existing devices and then some possible applications of the polar resistor are also explored.

Table 1 compares the proposed polar resistor with several existing linear, nonlinear, and asymmetric two-terminal devices. Conventional resistors exhibit linear and symmetric IV characteristics with polarity-independent resistance. Diodes show polarity dependence; however, their transport is strongly nonlinear and governed by junction barrier effects with a turn-on voltage. Varistors also exhibit nonlinear conduction due to field-dependent transport and breakdown-related mechanisms. Memristive devices, including bipolar and self-rectifying memristors, exhibit polarity-dependent behavior through resistive switching, hysteresis, and memory states arising from ionic migration. Ionic rectifiers similarly rely on ion-transport-controlled asymmetric conduction and are not electronic devices. In contrast, the proposed polar resistor exhibits linear current–voltage behavior in both polarities while maintaining different resistance values for opposite voltage polarities. Furthermore, the device does not require resistive switching, threshold-triggered transitions, or memory effects. The polarity dependence instead arises from asymmetric voltage distribution and carrier density modulation within the semiconductor structure which will be discussed in upcoming sections. Therefore, the proposed device represents a distinct form of passive two-terminal asymmetric resistance.

Table 1 — Comparison between existing electronic devices and the polar resistor

Device	I–V	Polarity / Dependence	Memory / Hysteresis	Threshold/ Switching	Conduction in Both Polarities	Dominant Operating Mechanism
Resistor	Linear, symmetric	No	No	No	Yes	Ohmic conduction
Diode	Nonlinear, asymmetric	Yes	No	Threshold present	Limited reverse conduction	Barrier-controlled transport
Varistor	Nonlinear, symmetric	Weak/absent	No	Threshold present	Yes	Breakdown-controlled
Bipolar Memristor	Nonlinear, asymmetric	Yes	Yes	Resistive switching	Yes	Ionic migration
Self-Rectifying Memristor	Nonlinear, asymmetric	Yes	Yes	Resistive switching	Yes	Rectification, memristive switching
Ionic Rectifier	Linear, asymmetric	Yes	Sometimes	Ion transport-controlled response	Yes	Electrochemical transport
Polar Resistor (this work)	Nearly linear in each polarity	Yes	Not expected	No	Yes	Asymmetric voltage drop and carrier distribution

Now, some possible and proposed applications of the polar resistors are explored. AC waveforms that have different amplitudes or time durations for the positive and negative half-cycles are named asymmetric AC[21-23]. Polar resistors can convert regular AC waveforms into asymmetric AC. Polar resistors naturally create amplitude asymmetry. They can also cause time-domain asymmetry when they are connected to capacitors or inductors in filter circuits. Electrophoresis[21,24], electroluminescence in OLEDs[22,25], and mass spectrometry[23,26] all these techniques systematically use asymmetric AC.

Polar resistors may also enable (soft) rectification, asymmetrical clipping, and polarity-sensitive attenuation that can be used in signal processing[27,28] and audio technology[29,30]. When transitions occur in signals, diodes and active components introduce hard thresholds, distortion or switching noise. In contrast, polar resistors may help preserve the continuity and dynamic range in signals. This can enable undistorted analog processing of low-voltage signals in particular, such as audio signals. Thus, wave shaping[31,32], in the form of clipping[33,34], clamping[35,36], and rectification[37,38] can be accomplished by polar resistors.

Polar resistors can enable passive logic gates[39,40]. Polar resistors can achieve continuous voltage division and signal flow through logic gates, unlike traditional diodes. The improvement in logic swing and voltage drop can be advantageous. This may be especially important in low voltage levels in on-chip logic circuits[41,42].

In unidirectional current sensing[43,44] with diodes or transistors, the sensing circuit faces hard thresholds or active biasing. Current sensing using polar resistors can be passive, linear, and distortion-free. This can be particularly advantageous at small voltages and currents.

Polar resistors can help in on-chip soft impedance matching[45,46]. In traditional impedance matching, on-chip series resistors, MOS-based variable resistors, RC networks, or diode hard voltage clamps symmetrically reduce the signals or introduce nonlinearity. With polar resistors, signal reflections may soften selectively, which allows for passive, wideband, and power-efficient soft impedance matching on a chip.

Polar resistors can enable soft braking[47,48] of on-chip micromotors[49,50]. When braking, reverse currents are produced. Polar resistors can effectively damp these reverse currents with a high reverse resistance without applying any voltage clamping. This technique may provide softer braking of the motor compared to the active braking technique that uses diodes or transistors.

In neuromorphic circuits[51,52], the rectifying synapse[53,54] function in neurons can be modeled better by polar resistors. Rectifying synapses allow sufficient reverse currents but at present they are modeled with diodes. This feature can lead to proper analog synaptic weighting[55,56], low voltages, and accurate spike timing dynamics[57,58]. Analog synaptic weighting refers to the variation of the synaptic conductance. Spike timing dynamic refers to the response of the synapse to a voltage spike. This paper only reports simulations of the polar resistor. Experimental fabrication will be necessary to access the polar resistor's true potential applications.

2 Simulation

Figure 2 outlines the semiconductor structures used in simulations. Figure 2 (a) shows a INI structure, where a n-type layer is sandwiched between two intrinsic layers. The left intrinsic layer is connected to an external DC voltage source, and is called the reverse layer. The other intrinsic layer is grounded; it is called the forward layer. It is seen, while exhibiting polar resistance, the forward layer will be responsible for forward conduction (positive voltage and current), and the reverse layer will be responsible for reverse conduction (negative voltage and current). For example, INI structures of Si and GaAs are simulated. The INI structure can be simulated, but is impractical in practice. This is because it is not possible to create metallic ohmic contacts to semiconductor intrinsic layers. This problem is solved with contact enabling layers (Fig. 2 (b)) of n-type CdS for Si, and of n-type SnO_2 for GaAs. Then, the external ohmic contacts are always made to CdS or SnO_2. The middle layer is always n-type doped. Thus, for the INI structures, simulations are done for I-Si/N-Si/I-Si, or I-GaAs/N-GaAs/I-GaAs. For the NININ structures, simulations

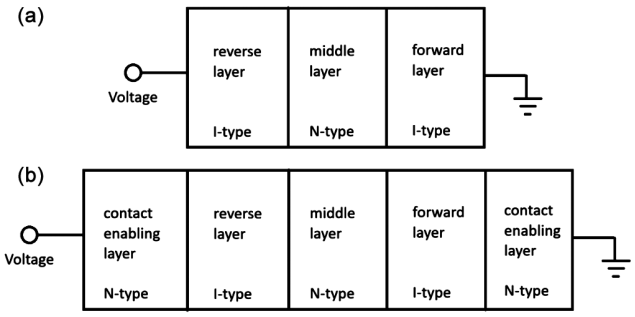

Fig. 2 — Schematics of the (a) INI; and (b) NININ semiconductor structures used for simulations

are done for N-CdS/ I-Si/N-Si/I-Si/N-CdS, or N-SnO_2/I-GaAs/N-GaAs/I-GaAs/N-SnO_2. The materials parameters chosen for simulations, for Si and GaAs[59], for CdS[60], and for SnO_2 [61-64] are provided in Table 2. All simulations are done in ADEPT 2.1[66], a software that solves the Poisson equations, the Continuity equations and the Drift-diffusion equations simultaneously using a discrete mesh and a generalized Newton iteration method. The same software has been used for solar cell studies previously[65].

The simulations were performed with ADEPT 2.1's default adaptive non-uniform mesh consisting of 250 spatial nodes. The adaptive meshing automatically increases node density in regions that have strong spatial variations of electric field or carrier distributions. Test simulations with higher mesh density produced no change in the simulation results.

The simulations were done using the default Newton solver settings with a maximum of 100 Newton iterations and a minimum convergence error tolerance of 10^{-6}. Test simulations with greater number of iterations and a lower convergence error tolerance produced no change in the simulation results. Ideal and ohmic charge neutral contacts were used for both the front and back contacts to the devices.

3 Results and Discussion

First, simulations are carried out for the Si INI structure and it is demonstrated that it the structure exhibits polar resistance. Next, the CdS contact enabling layers are introduced and the simulations for Si/CdS NININ structures are repeated. Then simulations are carried out for GaAs INI and GaAs/SnO_2 NININ structures to demonstrate that GaAs also shows polar resistance, and that polar resistance is not specific to a material system.

To begin, a Si INI structure is considered. Here, truly intrinsic Si is taken. Silicon's intrinsic carrier concentration is around 10^{10}/cc[59]. A nominal doping of 10^{9}/cc was chosen for software convergence. The middle layer is doped 10^{15}/cc. The thickness of the reverse layer is taken to be 500 μm. The middle layer is also 500 μm. The thickness of the forward layer is varied from 500 μm to 100 μm. The current-density (J) – voltage (V) curves for this Si INI structure is shown in Fig. 3.

The different rectification ratios (RRs) obtained in Fig. 3 are: 1, 2.3, 4.1, 6.8 and 8.9. RR is defined as the ratio of forward current at 1V and the reverse current at -1V. Figure 3 shows polar resistance when the thicknesses of the forward layer and reverse layer are different.

It is noted that polar resistance depends on charge recombination[1]. The RR decreases with increased recombination. The SRH electron and hole lifetimes[1] are kept at τ = 100 μs for all layers for which recombination is minimum. The radiative recombination coefficient B is kept at 10^{-12} cc/s for Si. For τ = 1 ns no polar resistance is seen. Polar

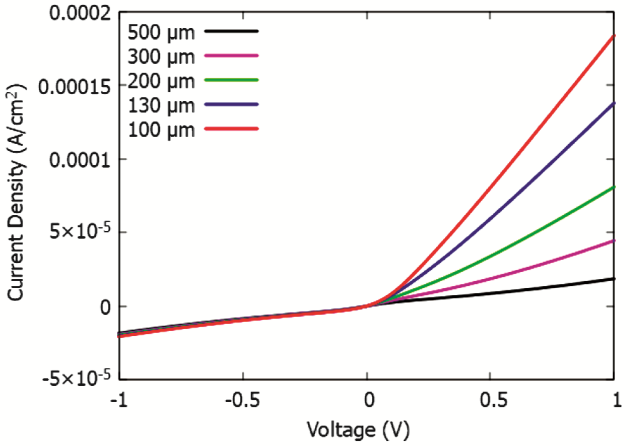

Fig. 3 — JV curves for Si INI structure for different forward layer thicknesses

Table 2 — Semiconductor parameter values considered for simulation

Semiconductor Parameters	Si	GaAs	CdS	SnO_2
Band Gap (eV)	1.1	1.4	2.4	3.6
Electron Affinity (eV)	4.05	4.07	4.5	4.7 (Ref. 62-64)
Dielectric Constant	11.7	12.9	8.9	11.5
Electron Mobility (cm^2/Vs)	1400	8500	250	100
Hole Mobility (cm^2/Vs)	470	400	50	10
Electron DOS Effective Mass	1.08	0.063	0.21	0.27
Hole DOS Effective Mass	0.81	0.51	0.8	1
Conduction Band DOS (/cm^3)	2.8×10^{19}	4.7×10^{17}	2.4×10^{18}	3.5×10^{18}
Valence Band DOS (/cm^3)	1×10^{19}	7×10^{18}	1.8×10^{19}	2.5×10^{19}

resistance was observed to be independent of B. The dependence of polar resistance on the SRH lifetime is not a limitation, as later it is demonstrated that polar resistance in Si/CdS NININ structures, with intrinsic Silicon's background doping densities as 10^{11}/cc or 10^{12}/cc, is independent of the SRH lifetime; i.e. independent of recombination.

Next, the working of the polar resistor is explored. Here, how the Si INI structure achieves polar resistance is discussed and the device physics behind it is explored. For this, the device with reverse layer thickness as 500 µm and forward layer thickness as 200 µm is chosen. From Fig. 3, this device has an RR of 4.1. Figure 4 shows the electron concentration profiles in this polar resistor device at 0V, 1V and -1V.

Figure 4 illustrates the electron profile at 0V (green). The middle layer acts as a charge reservoir. The neighboring intrinsic layers have much lower carrier concentrations. So, at zero volts, electrons diffuse to the two intrinsic layers and create some excess electrons near the two layer boundaries. The charge density of the middle layer is 10^{15}/cc, while the equilibrium electron densities in the two intrinsic layers are 10^{10}/cc which is the intrinsic carrier concentration of Si. Now, a positive voltage of 1V is given to the INI structure. This means the reverse layer is connected to a contact of positive potential, and the forward layer is connected to a contact of negative potential. Now the mechanism within the forward and reverse layers can be analyzed. The negative potential in the contact repels the excess diffused electrons in the forward layer to the left. As a result, the forward layer gets depleted of the excess electrons. This can be verified by following the red curve in Fig. 4. Similarly, the positive potential at the reverse layer attracts the excess diffused electrons to the left which makes the reverse layer to accumulate more electrons in the process. Thus, under positive applied voltage, the forward layer depletes and the reverse layer accumulates. The depleted electronic concentration is 10^{9} – 10^{10} /cc. The accumulated electronic concentration is around 10^{11}/cc. Thus, at 1V, the conductivity of the reverse layer increases and that of the forward layer decreases. This makes the 1V significantly drop across the forward layer. Very similarly, most of the -1V drops across the reverse layer (blue curve in Fig. 4), as, under a negative voltage, the reverse layer depletes and the forward layer accumulates. As the thicknesses of the forward and reverse layers are different, their inherent resistances are different and polar resistance is achieved for this structure. Figure 5 shows the energy band diagrams of the INI structure at 0V, 1V and -1V.

Flat energy bands are seen at 0V for all three layers (green). At 1V, the bands of the forward layer tilts (red). The bands do not bend as in a PN junction[1]. Such tilting of energy bands suggests ohmic voltage drop. No significant tilting of the reverse layer's bands at 1V is observed, suggesting almost no ohmic drop in the reverse layer. Similarly, at -1V (blue), the energy band of the reverse layer tilts and that of the forward layer remains flat. From the band diagrams it can be concluded that for forward conduction the forward layer achieves an ohmic drop, and for reverse conduction the reverse layer achieves an ohmic drop. Figure 6, further, shows the internal electric fields in the INI structure.

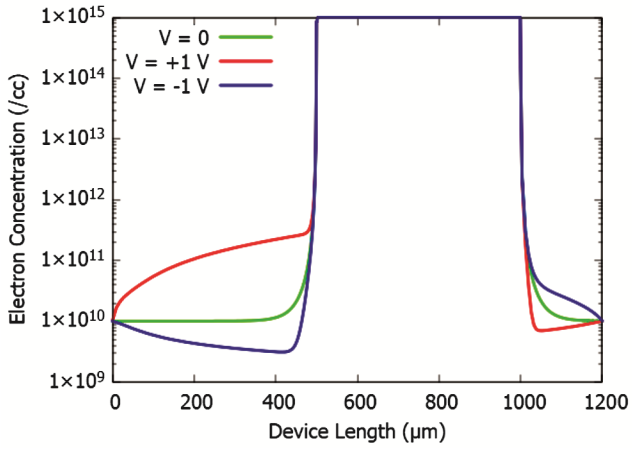

Fig. 4 — Electron concentration profiles inside the Si INI 500 µm/200 µm polar resistor

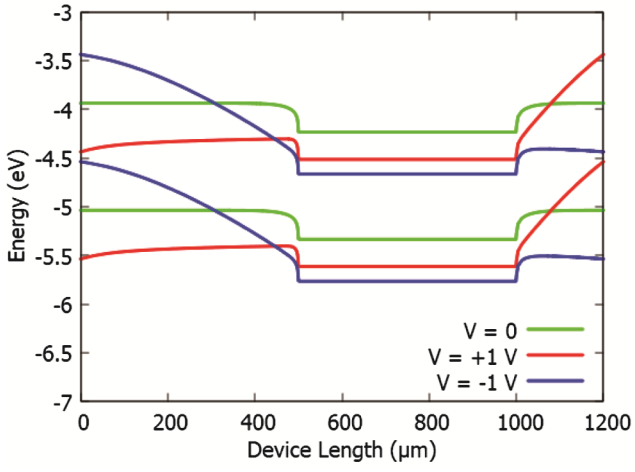

Fig. 5 — Energy band diagrams of the Si INI 500 µm/200 µm polar resistor

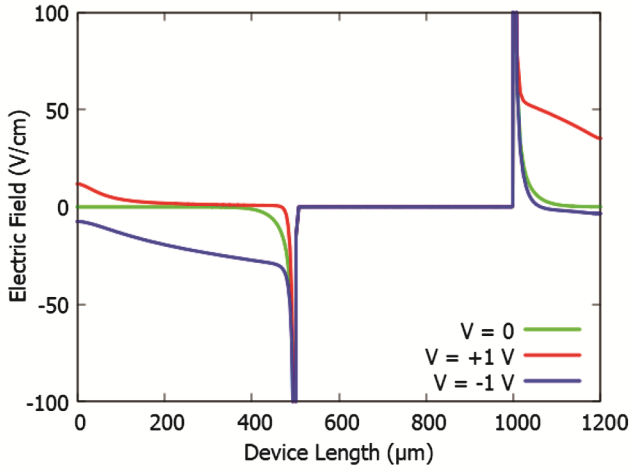

Fig. 6 — Electric fields inside the Si INI 500 μm/200 μm polar resistor

In Fig. 6, at 0V (green), the electric fields in all the layers are close to zero except at the two layer boundaries where the built-in field was observed to reach around 4000 V/cm. At 1V (red) the field increases in the forward layer while the reverse layer shows negligible field. At -1V (blue) the field in the reverse layer increases while no change in the field occurs in the forward layer.

Thus, the working of the polar resistor is clearly demonstrated. Now, some simple resistance calculations are attempted. From the electric field values shown in Fig. 6 it can be calculated how much voltage drops occur in the intrinsic layers. Then, from the known value of the current densities (Fig. 3) and Ohm's law, the mean carrier density is calculated in the intrinsic layers which is responsible for the resistance it exhibits. In all cases it is seen that the calculated carrier density agrees well with what is observed for the depleted layers in the simulations.

The forward layer is first considered under the forward bias of V = 1V. Here, E_V is the mean electric field at 1V, and E_0 is the residual electric field at 0V. Considering t to be the layer thickness and V* to be the voltage drop across the layer, one achieves

$$V^* = (E_V - E_0).t \qquad \ldots (1)$$

Here, E_V = 46 V/cm, E_0 = 0, and t = 200 μm are considered. From Eqn. 1, V* = 0.92 V.

Thus, it is seen, approximately 90 % of the forward voltage drops across the forward layer. Next, the mean carrier density N is calculated, in the forward layer, that gives the layer its resistance. R is taken to be the resistance, J to be the current density, and A to be the device cross-sectional area. q is taken as the electronic charge and μ = 1400 cm^2/Vs as the electronic mobility. Then

$$RA = \frac{V^*}{J} = \frac{t}{Nq\mu} \qquad \ldots (2)$$

N is calculated from Eqn. 2. J = 8.086x10^{-5} A/cm^2 is considered. Putting in the values of V*, t, q and μ, one achieves N = 7.8x10^9 /cc. The simulated N is within 7x10^9 – 1x10^{10} /cc.

Next, the reverse layer is studied under forward bias. Putting t = 500 μm, E_V = 3 V/cm, and E_0 = 0, the calculated V* = 0.15 V. This confirms that around 10% of the forward voltage drops across the reverse layer. The calculated N is N = 1.2x10^{11}/cc. The simulated N varies between 10^{10} – 3x10^{11} /cc.

Next, the reverse layer is considered under reverse bias. t = 500 μm, E_V = 20 V/cm and E_0 = 0. This yields V* = 1V. So, it is concluded that all of the reverse voltage drops across the reverse layer. J = 1.974x10^{-5} A/cm^2 is considered. The calculated N is N = 4.4x10^9 /cc. The simulated N is N = 3.1x10^9 – 10^{10} /cc.

So, polar resistance is seen in the Si INI structure, the working principle has been discussed, i.e. the physics behind the working, and simple resistance calculations confirming that forward conduction is mostly by the forward layer and reverse conduction is by the reverse layer have been demonstrated. Next, an inquiry is: whether any thickness asymmetry in the INI structure necessarily mean polar resistance. It is observed that it is not the case. Polar resistance was found inside a particular window of the thickness phase space. The INI structure is checked for thicknesses between 10,000 μm to 100 nm and the findings are reported. For all cases, the thickness of the middle layer is kept the same as that of the reverse layer.

First, the reverse layer/forward layer thicknesses are kept to be 10,000 μm/1000 μm. For this combination, no polar resistance was found. Even the partitioning of voltage drops (i.e. positive voltage drops across forward layer and negative voltage drops across reverse layer) is not observed. The voltage drops simply across the reverse layer. Next, checks are done for 3000 μm/300 μm, for 1000 μm/100 μm, and for 300 μm/30 μm, and 100 μm/10 μm. Here polar resistance exists. Partitioning of voltage drops across layers exist, and also the current density-voltage (JV) curves are linear. For thinner layers, such as for 30 μm/3 μm, 10 μm/1 μm, 3 μm/300 nm, and

1 μm/100 nm partitioning of voltage drops are found to be present but the JV curves are not linear. For 1 μm/100 nm case the thickness of the middle layer had to be increased because otherwise the middle layer did not have enough charge to flow to the intrinsic layers. The middle layer (its doping and thickness and how they affect the polar resistor) is discussed towards the end of this paper.

Polar resistance is seen in Si INI layers. But, if fabricated, practically, it is of no significance. Intrinsic semiconductor layers cannot be connected to external electronic circuitry because it is almost impossible to make metallic ohmic contacts to them. To circumvent this problem, simulations of an NININ structure were tried where contact enabling layers were n-type Si. But electrons were observed diffusing from the contact enabling layers into the intrinsic layers which ruin polar resistance. So, n-type CdS was chosen as the contact enabling layer. The doping density was taken to be 10^{18}/cc. Here it will be possible to make metallic ohmic contacts to doped CdS, and also electrons do not diffuse from CdS to intrinsic Si layers as the difference in the electron affinities for CdS and Si provides the sufficient energy barrier to stop electrons from crossing over from CdS to Si. The thickness of the CdS layers, on either side, were kept at 100 nm.

Also, intrinsic layers, in reality, are not completely intrinsic and often have a background doping concentration. To simulate such NININ Si/CdS structures (Fig. 2(b)) a background mobile electronic concentration of 10^{11}/cc or 10^{12}/cc were chosen for intrinsic Si. To do this a doping density of 10^{11}/cc or 10^{12}/cc was set for intrinsic Si in ADEPT.

Simulations were done for background electronic concentration of 10^{11}/cc. The reverse layer thickness is kept at 10 μm. The forward layer thickness is varied from 10 μm to 100 nm. The middle layer thickness is kept at 10 μm. The middle layer doping is 10^{15}/cc. The JV curves are shown in Fig. 7.

The RRs of this set of curves are: 1, 2.7, 5.9, 8.3 and 11.8. The curves clearly show polar resistance. Interestingly, this time, the simulation result is not dependent on charge recombination. Checks were performed, in ADEPT, with SRH τ = 1 ns (maximum recombination) in both Si and CdS layers, and a radiative coefficient of B = 10^{-12} cc/s for Si and B = 10^{-9} cc/s for CdS. But polar resistance was not found to depend on the presence of recombination.

It is important to show that the working of the device stays the same even in presence of the contact

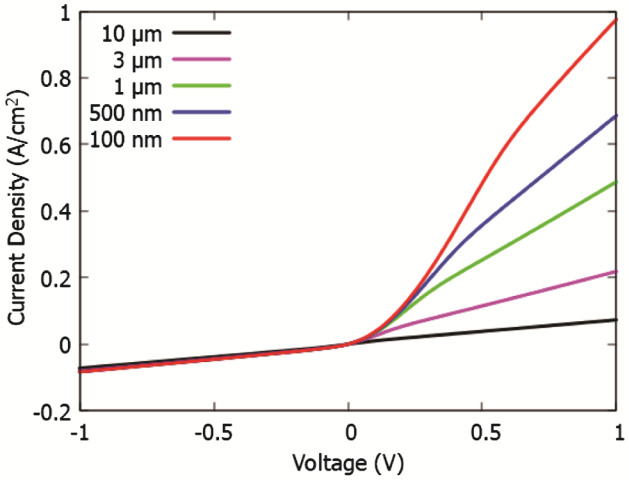

Fig. 7 — JV curves for Si/CdS NININ structure for different forward layer thicknesses, with intrinsic Si background electronic concentration as 10^{11}/cc

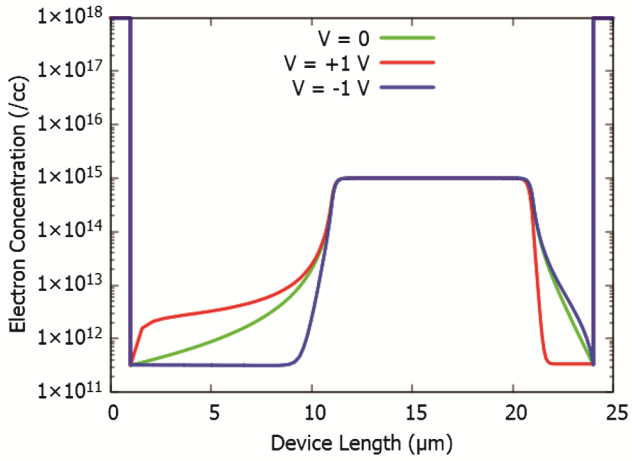

Fig. 8 — Electron concentration profiles inside the Si/CdS NININ 10 μm/3 μm polar resistor

enabling layers. For this, a polar resistor device is chosen with 10 μm as the reverse layer thickness and 3 μm as the forward layer thickness. The RR of this device is 2.7. The CdS layers thickness were kept as 1 μm. Doing this has no effect on the JV curves. This was done so that the CdS layers are visible in the figures. Figure 8 shows the electronic concentration profiles, Fig. 9 shows the energy band diagrams and Fig. 10 shows the internal electric fields.

It is observed, from Figs. 8-10 that for forward bias the voltage drops mostly across the forward layer and for reverse bias the voltage drops across the reverse layer. Next, the resistance calculations are repeated to quantify the voltage drops and the electron concentrations inside the resistive Si layers.

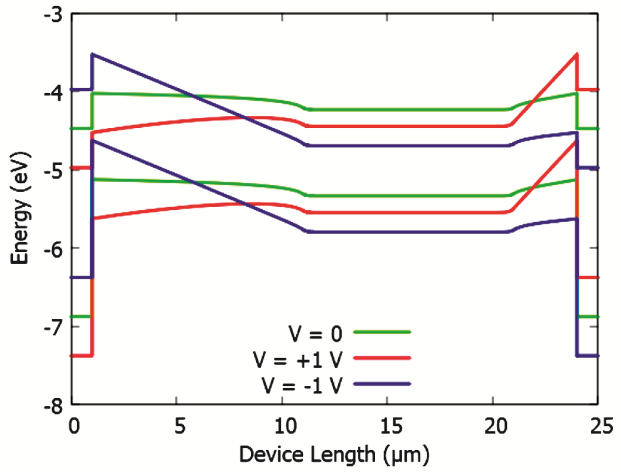

Fig. 9 — Energy band diagrams of the Si/CdS NININ 10 μm/3 μm polar resistor

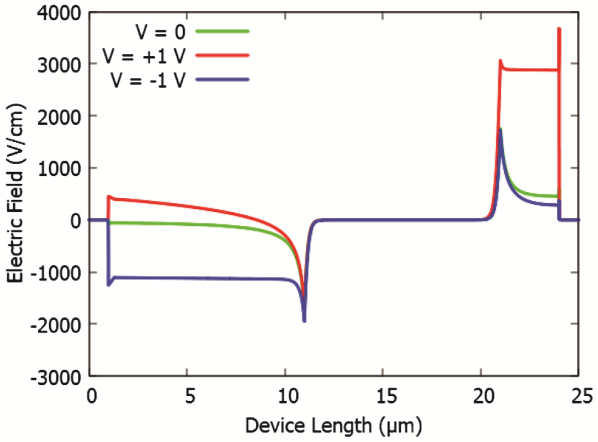

Fig. 10 — Electric fields inside the Si/CdS NININ 10 μm/3 μm polar resistor

Equations. (1) - (2) are referred. For forward bias, and for the forward layer, t = 3 μm, E_V = 2881 V/cm, E_0 = 474 V/cm are considered, and it is calculated that V* = 0.72 V. J = 0.2184 A/cm^2 is considered and it is calculated that N = 4.05x10^{11}/cc. The simulated N = 3.4x10^{11}/cc. For forward bias, for the reverse layer, t = 10 μm, E_V = 350 V/cm, E_0 = 100 V/cm are considered, and calculated V* = 0.25 V. So, it is concluded, in forward bias, 75 % of the voltage drops across the forward layer and 25% of it drops across the reverse layer. Taking J = 0.2184 A/cm^2, calculated N = 3.9x10^{12}/cc. It is seen that the simulated N varies between 3x10^{11}/cc and 10^{13}/cc. For reverse bias, for the reverse layer, t = 10 μm, E_V = 1122 V/cm and E_0 = 100 V/cm are considered. This yields a calculated V* = 1V. So, it is concluded, for reverse bias, all of the voltage drops across the reverse layer. To calculate N, J is taken to be J = 0.08 A/cm^2. The calculated N is N = 3.5x10^{11}/cc. The simulated N = 3.2x10^{11}/cc.

Next, the thickness scans are performed for the Si/CdS NININ structure. Simulations are done for various pairs of reverse layer and forward layer thicknesses and it is checked where polar resistance occurs. The results are the same for 10^{11}/cc and 10^{12}/cc background electronic concentrations in the intrinsic layers. In all cases the middle layer thickness is kept the same as the reverse layer thickness. For reverse layer thickness/ forward layer thickness of 10,000 μm/1000 μm polar resistance is not achieved. Instead, the voltage drops across the reverse layer for both polarities. The result stays the same up to 100 μm/10 μm. For 30 μm/3 μm and 10 μm/1 μm, polar resistance occurs. For all lower thickness pairs, up to 100 nm, partitioning of voltage drops occur, i.e. the forward voltage is dropped across the forward layer and the reverse voltage is dropped across the reverse layer, however, the JV curves are non-linear. So, no polar resistance exists in this regime.

The JV curves showing polar resistance for the Si/CdS NININ structure for background electronic concentration of 10^{12}/cc, for intrinsic Si layers, is shown in Fig. 11. Here also the reverse layer and middle layer thickness is taken as 10 μm, and the forward layer thickness is varied between 10 μm and 100 nm. The RRs, as observed, are: 1, 2.6, 5.8, 8.1 and 11.4. Here also, the simulation results were found to be independent of charge recombination.

Polar resistance in Silicon structures have been demonstrated, be it INI structures, or with the CdS contact enabling layers, i.e. NININ structures. Now, to show that polar resistance is not a specific material phenomenon it is demonstrated in GaAs INI and GaAs/SnO_2 NININ structures.

A GaAs INI structure is simulated first. Intrinsic carrier concentration of GaAs is 10^6/cc[59]. The doping density of the intrinsic layers was kept at 10^5/cc in the ADEPT simulations. The doping density of the middle layer is 10^{15}/cc. Thickness of the reverse layer and middle layer was 10,000 μm. The forward layer thickness is varied between 10,000 μm and 1000 μm. The JV curves are shown in Fig. 12.

The RRs in Fig. 12 were found to be: 1, 2.1, 4.1, 6.6 and 9.7. The JV curves were observed to depend on charge recombination. The reported JV curves in Fig. 12 are for a SRH lifetime τ = 0.1 s. This is a very high SRH lifetime and in reality, it is not expected that GaAs is purified to such an extent that it will

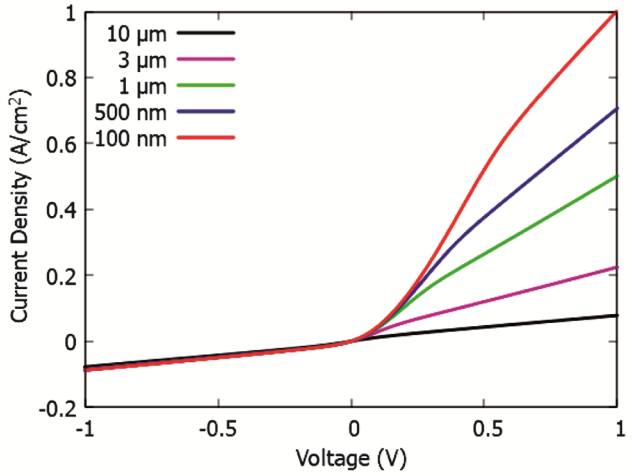

Fig. 11 — JV curves for Si/CdS NININ structure for different forward layer thicknesses, with intrinsic Si background electronic concentration as 10^{12}/cc

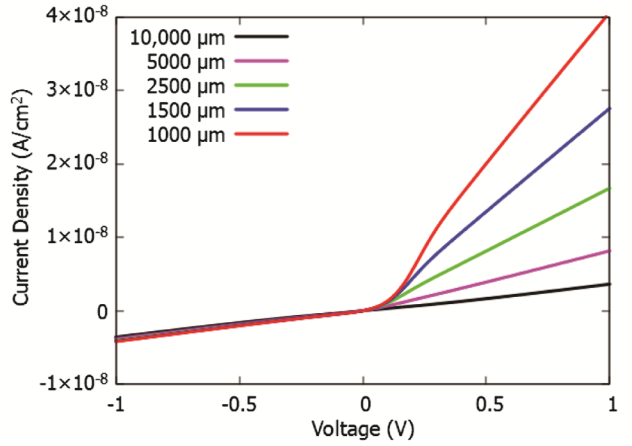

Fig. 12 — JV curves for GaAs INI structure for different forward layer thicknesses

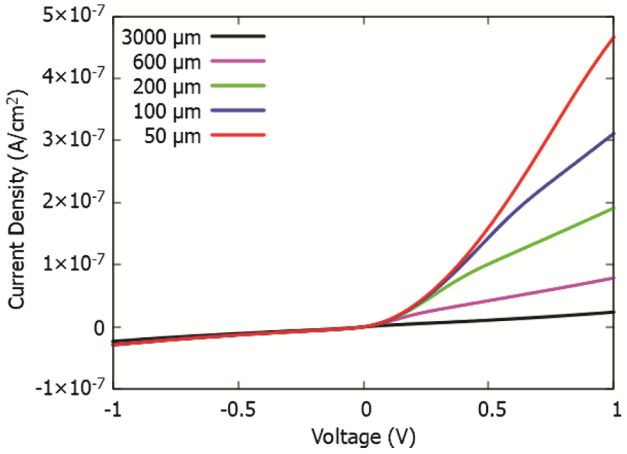

Fig. 13 — JV curves for GaAs/SnO_2 NININ structure for different forward layer thicknesses, with intrinsic GaAs background electronic concentration as 10^7/cc

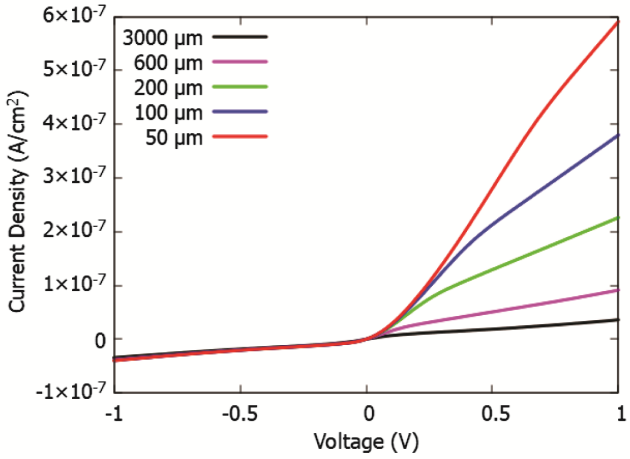

Fig. 14 — JV curves for GaAs/SnO_2 NININ structure for different forward layer thicknesses, with intrinsic GaAs background electronic concentration as 10^8/cc

show a lifetime of 0.1 s. But the INI devices cannot be, anyway, connected to an external voltage source due to ohmic contact problems. In the NININ devices, with SnO_2 contact enabling layers, it will be observed that charge recombination does not play a role. In Fig. 12, the radiative recombination coefficient B = 10^{-9} cc/s. The JV curves were seen not to depend on B, but to heavily depend on τ. But, interestingly, unlike for Si INI structures, where rectification ratio disappears completely for high SRH recombination, in GaAs the maximum rectification ratio (i.e. for forward layer thickness = 1000 µm) drops to 3 when a τ = 1 ns is used; i.e. RR does not collapse completely.

For the thickness scans, a reverse layer thickness/ forward layer thickness of 10,000 µm/1000 µm gives polar resistance. So does 3000 µm/300 µm. But for any lower thickness combinations (1000 µm/100 µm to 1 µm/100 nm) polar resistance does not exist: the voltage partitioning exists but the JV curves are non-linear.

Next, polar resistance is demonstrated in GaAs/SnO_2 NININ structures. 100 nm thick SnO_2 layers add to the GaAs INI in both sides. The doping density of the SnO_2 layers is 10^{18}/cc. The background mobile electronic concentration in intrinsic GaAs layers is kept at 10^7/cc or 10^8/cc. These refer to practical devices. The reverse and the middle layers' thickness is kept at 3000 µm. The forward layer thickness is varied from 3000 µm to 50 µm. Figures 13 and 14 shows the JV curves for 10^7/cc and 10^8/cc background electronic concentration for

intrinsic GaAs. The RRs, in Fig. 13, are: 1, 2.8, 6.7, 10.8, 16.1.

The RRs, in Fig. 14, are: 1, 2.4, 5.7, 9.6, 14.8. In both Fig. 13 and Fig. 14, charge recombination does not play a role in deciding the JV. As in Si/CdS NININ, here also the results are independent of recombination. This is checked by putting a SRH lifetime τ = 1 ns in all layers. The radiative recombination coefficient B = 10^{-9} cc/s for GaAs and 10^{-12} cc/s for SnO2. But the results were seen to not to differ.

Thickness scans were performed to check for polar resistance across the thickness phase space. For reverse layer thickness/ forward layer thickness of 10,000 μm/1000 μm, no polar resistance was observed. For the 10^{7}/cc case, voltage drops across the reverse layer for both positive and negative polarities. For 10^{8}/cc, the reverse layer energy bands bend and do not tilt. For 3000 μm/300 μm polar resistance is found. From 1000 μm/100 μm to 1 μm/100 nm one finds partitioning of voltage drops, but no linearity.

So, polar resistance in Si and GaAs are demonstrated. Now the attention shifts to the middle layer. For all thickness scans discussed in this paper, for the last pair of thicknesses, i.e. for 1 μm/100 nm, the thickness of the middle layer needed to be increased. This is because the middle layer did not have the capacity to supply electrons to the intrinsic layers. Therefore, the optimum thickness and doping concentration of the middle layer are investigated. The 10 μm/3 μm Si/CdS NININ device is selected as a representative example for this analysis.

In Fig. 4 and Fig. 8, it is observed that the middle layer is serving as a charge reservoir. Its main purpose is to provide electrons that can diffuse to the intrinsic layers kept at either side. In all simulations reported in this work so far, the thickness of the middle layer was kept the same as that of the reverse layer. One can indeed decrease the thickness of the middle layer further and ensure proper working of the device. This saves semiconductor material. But it should be borne in mind that there should be enough charge in the middle layer which should be able to diffuse to the intrinsic layers. If somehow the thickness is so small that insufficient charge flows to the neighboring layers the device ceases to work properly.

To investigate this, the doping density of the middle layer is increased. The 10 μm/3 μm Si/CdS NININ device is checked with doping densities of 10^{15}/cc, 10^{16}/cc, 10^{17}/cc and 10^{18}/cc. In all cases polar resistance was found. In fact, the RR increases slightly from 2.7 (10^{15}/cc) to 2.9 (for 10^{18}/cc). But increasing the doping of the middle layer comes with a cost. It unnecessarily increases the electric field peaks at the two layer boundaries (i.e. at the IN and the NI junctions). So, increasing the doping density of the middle layer electrically stresses the device more. In no simulations in this paper it was observed that the electric field crosses the breakdown field (which is around 10^{5} V/cm[59] for Si and GaAs).

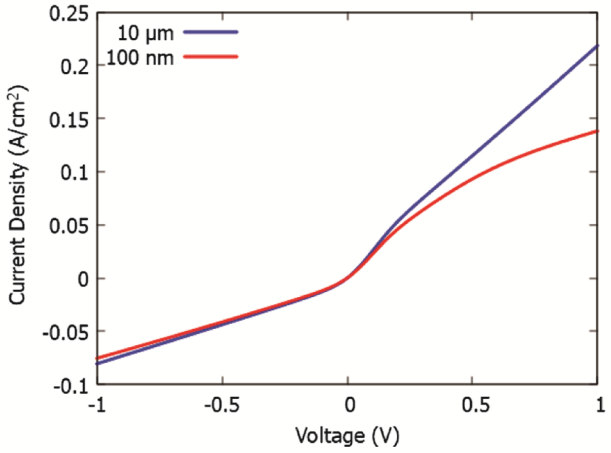

Fig. 15 — JV curves for the 10 μm/3 μm Si/CdS NININ polar resistor for middle layer thickness 10 μm and 100 nm

Next, in the 10 μm/3 μm Si/CdS NININ structure, the middle layer doping density is kept at 10^{15}/cc, but its thickness was decreased to 100 nm to see whether polar resistance exist or not. Figure 15 reports the JV curve.

It is observed that for 100 nm thickness the JV curve becomes non-linear in the forward direction. So, clearly, a thickness of 100 nm is a wrong choice for the middle layer in this case. Figure 16 shows the electron concentration profiles, across the device, for the 100 nm thick middle layer.

Comparing Fig. 16 with Fig. 8, it is seen that in Fig. 16 the maximum electronic concentration of the middle layer drops below 10^{14}/cc. This is in spite of keeping the doping density as 10^{15}/cc. The middle layer has insufficient charge to send to the neighboring intrinsic layers. So, the thickness of the middle layer should not be 100 nm and should be increased.

Finally, the contact enabling layers are explored and how their thickness and doping density affects polar resistance are studied. The thickness of the contact enabling layer does not change the JV curves or affect polar resistance. The thickness has been

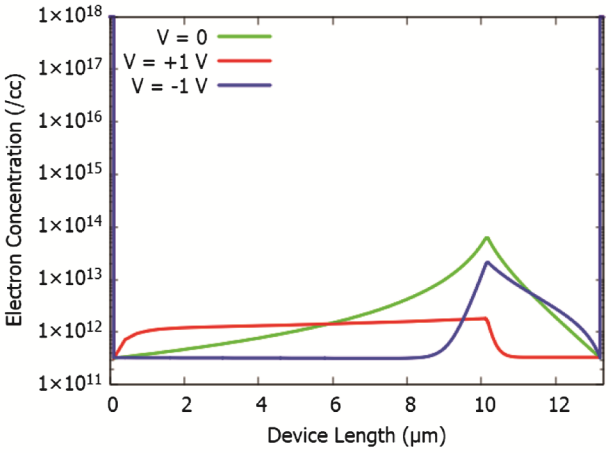

Fig. 16 — Electron concentration profiles inside the Si/CdS NININ 10 µm/3 µm polar resistor for middle layer thickness 100 nm

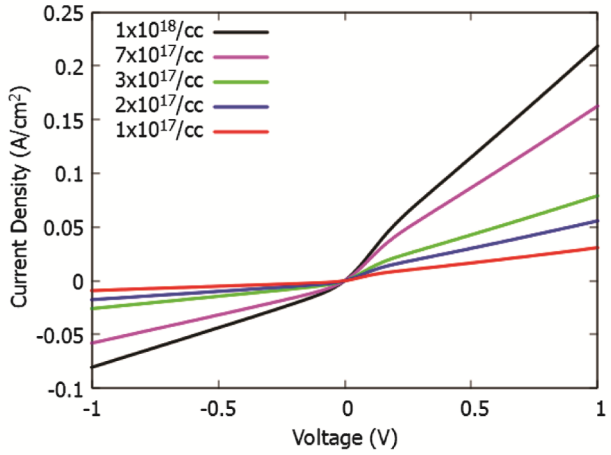

Fig. 17 — JV curves for the 10 µm/3 µm Si/CdS NININ polar resistor with varying CdS doping density

varied from 100 nm to 10 µm and this has been verified for the 10 µm/3 µm Si/CdS NININ device. However, the doping density of the contact enabling layer does affect the JV curves. Figure 17 shows how the JV curves are affected if the doping density is changed from 10^{18}/cc to 10^{17}/cc.

It is observed that current decreases as doping density is decreased. The RRs, here, are: 2.7, 2.8, 3, 3.2, and 3.4. So, the RR increases, but slightly, if the doping density is decreased, but the current decreases almost over an order of magnitude.

Power dissipation (P) of polar resistors is polarity dependent. Since high current flows in the forward direction and low current flows in the reverse direction, power dissipation is more for forward conduction and less for reverse conduction. For either polarity, since P = VI, power dissipation is parabolic with voltage (V^2/R) as resistance remains unchanged throughout the voltage range. The maximum power dissipation of the Si/CdS polar resistors whose JV curves have been shown in Fig. 7 is calculated. For this, a nominal device cross-sectional area of 100 µm x 100 µm is considered. The 10 µm reverse layer and 10 µm forward layer device exhibits a maximum power dissipation of 8 µW at both +1V and -1V as it is a symmetric device with equal forward and reverse resistances. For the 10 µm/3 µm polar resistor the maximum reverse power dissipation remains at 8 µW, and the maximum forward power dissipation is 22 µW. For the 10 µm/1 µm device the maximum forward power dissipation is 50 µW. For the 10 µm/500 nm polar resistor it is 70 µW, and for the 10 µm/100 nm device it is 98 µW. The maximum power dissipation is around 100 µW which shows that the power dissipation of these polar resistors is low and is not expected to cause any significant joule heating.

The frequency response of the polar resistors have been noted. Here, the DC simulations of polar resistors have been shown. A complete AC characterization is outside the scope of this study, and it is also to be borne in mind that the simulator used in this work, ADEPT 2.1, is a DC simulator and cannot do AC simulations. But one can always predict the frequency response of the reported devices from the electron density profiles and how they change under applied positive and negative bias. Polar resistors are majority carrier devices. Here electrons are the majority charge carriers. All layers (considering the polar resistors with contact enabling layers) are n-type and holes do not play a notable role in determining the polar resistor characteristics. In Fig. 8 how the electron concentration profile (the diffusion profile) changes under an applied bias has been shown. If the polarity across a polar resistor is changed within a short time duration, no specific problem is expected. So, it is predicted polar resistors can function properly at high frequencies. This is also supported by the fact that no dependence of the polar resistor characteristics is seen on charge recombination in the DC simulations reported (for devices with contact enabling layers where all layers are n-type). So unlike PN junctions whose minority carrier storage disrupts the high frequency behavior no such behavior is expected from polar resistors. Therefore, polar resistors are expected to work well at high switching frequencies.

Polar resistors are made with semiconductor layers that exhibit resistive properties. So thermal noise (Johnson-Nyquist noise), which is caused by random thermal motions of electrons inside conductors, is expected in polar resistors. These semiconductor layers can also have defect states, which can cause trapping of electrons. Therefore, 1/f noise (Flicker noise) also expected in polar resistors. These two noises are inherently present in all semiconductor resistors, and so they are expected in polar resistors too.

4 Conclusion

Polar resistance in Si and GaAs INI structures were demonstrated. These INI structures are capped with contact enabling layers of CdS or SnO_2 on both sides and the devices demonstrate polar resistance in the resulting NININ structures as well. A rectification ratio up to 10 is demonstrated. The working of the polar resistors is explained and their physics is clarified. The current-voltage curves of the NININ polar resistors do not depend on the presence of charge recombination. It is also observed that structural asymmetry (difference in the thicknesses of the intrinsic layers) do not alone guarantee polar resistance; the thickness range is scanned from 10,000 μm to 100 nm to find where polar resistance exists for Si and GaAs INI and NININ structures. Polar resistance is caused by simple ohmic drops across the intrinsic layers and simple resistance calculations are carried out to support the findings. How the doping density and thickness of the middle layer as well as the contact enabling layers affect the polar resistance is also reported. These Si and GaAs NININ polar resistors can be fabricated as practical real-world devices. Polar resistors may find applications in asymmetric AC waveform generation, signal processing, unidirectional current sensing, soft braking of motors and in neuromorphic circuits.

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