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Low Power Non-Volatile 7T1M Subthreshold SRAM Cell

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A new modified 7T1M non-volatile SRAM cell is presented in this paper for low power applications at subthreshold voltage (very low voltage) simply by connecting the memristor directly with storage node which is acting as storage element and adding a transistor in between the two storage nodes with feedback connection gives better performance in terms of average delay, read /write operations and RSNM/WSNM. The memristor based circuits are simulated at subthreshold is a new insight and a new effort in technology made with improvement of approximately 61% and 23% of RSNM and WSNM respectively compared to existing memory cell 7T1M and power dissipation is decreased by 66% whereas read delay and write delay obtained is nominal. Moreover, It has also simulated an adjusting 6T2M and conventional 6T at subthreshold voltage i.e. V_{DD}=0.3V to compare its stability behaviour at lower supply voltage.

Keywords: Memristance; Subthreshold; SRAM cell; Memristor; Voltage scaling; stability; Power dissipation

1 Introduction

Memory technology is very advanced these days in making new modes of operation in nanotechnology. Power and Energy is one of the major concern. SRAM is mostly used because of its data retaining capacity when compared with DRAM and also it has good power on/off speeds[1]. Increase in the demand of mobile applications with prolonged battery life and low power consumption has come up with new design in memories where subthreshold concept is used for power reduction. This subthreshold concept has emerged as a solution for low power application devices. Lowering the supply voltage V_{DD} saves power as well as energy[2]. Also, since dynamic power consumption is directly proportional to square of V_{DD}, scaling of V_{DD} can reduce the power efficiently under subthreshold condition[3-9].

Non-volatile memory (NVM) has the capacity to back up the previous data and restore when power is cut off, so loss of data and power consumption is improved by integrating the NVM device in SRAM cell (NVSRAM). With analysis and simulations, it is been reported that adoption of NVM is very effective to reduce the consumption of power by lowering the supply voltages. Memristor based memory cells are very challenging where few remarkable work done with structures of 6T2M, 7T2M, 7T1M, 8T2M, 8T1M[10-17] where power dissipation is observed. Keeping in mind the disadvantages of existing cells, this work has combined the concept of subthreshold (low supply voltage) and nonvolatile element in SRAM cell which is a new approach and new possible NVSRAM cell. This paper has proposed a modified structure of 7T1M memristor based SRAM cell and simulated at subthreshold region with lower supply voltage maintaining the trade-off between parameters of the circuit. Motive was basically to improve RSNM/WSNM and power consumption which was not as good in existing work at higher supply voltage. Improving power dissipation and stability is very useful advantage in power hungry mobile devices.

This paper is further organized in sections as following: section 2 describes the basic memristor element behavior and its properties, section 3 elucidates the design methodology used in the work. The results and Simulations of the existing and proposed circuit have been discussed in the section 4 and finally section 5 concludes.

2 Memristor Behavior and Properties

The functional memristor model provides a relation between the memristance and the electric current and the memristor current moves through as explained in Equation(1). The practical HP Lab memristor model was demonstrated which consists of titanium oxide and oxygen vacancies shown in Fig. 1 which was first discovered by HP labs in 2008[18]. A deficient layer of

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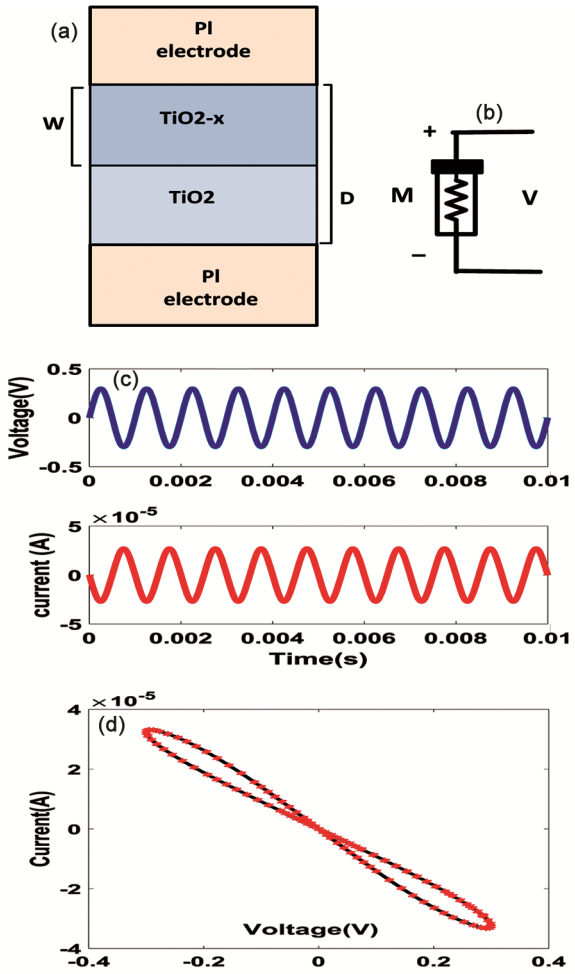

Fig. 1 — (a) Memristive device structure[1,12] (b) Symbol of memristor(c) Voltage and current flowing at element (d) Hysteresis loop at V-I curve obtained at low voltage showing the memristivebehaviour.

titanium is joined between two layers of platinum (Pt). R_{ON} (low resistance) and R_{OFF} (high resistance) condition can be obtained by direction of the current flow. The margin of the doped region moves right in lower resistance as oxygen vacancies drift from the doped (TiO_{2-x}) to the undoped (TiO_2) region and vice versa depending on the flow of current. Fig. 1 also describes the symbol and polarity of the memristor[19].

Relating the charge and flux are called memristive relationship given as in Equation (1) and (2):

$$q(t) = \int_{-\infty}^{t} i(\tau)d\tau \quad \ldots (1)$$

$$\emptyset(t) = \int_{-\infty}^{t} v(\tau)d\tau \quad \ldots (2)$$

A generalized expression to understand memristive behavior is given by:

$$V = R(w_1, w_2, \ldots\ldots w_k \ldots w_n)I \quad \ldots (3)$$

Where w_1, w_2 are state variables. Memristance of memristor having unit of resistance itself.

Equation (3) essentially relates the voltage, current, and the variation in the resistance according to the state of a device at any point of time. It also identifies the charge that passed through the device previously.

The constitutive relation for a memristor is f (∅, q) = 0[19].

The memristor is said to be charge controlled if ∅=∅(q). Then the voltage across the device is given by:

$$V = M(q)I \quad \ldots (4)$$

Where M (q) is termed as memristance given by:

$$M(q) = \frac{d\emptyset(q)}{dq} \quad \ldots (5)$$

Memristor is said to be flux controlled if q=q(∅) of the flux where current across it is given by[19] :

$$I = W(\emptyset)V \quad \ldots (6)$$

$$W(q) = \frac{dq(\emptyset)}{d\emptyset} \quad \ldots (7)$$

Where W (q) is termed as memconductance

As described earlier, undoped resistance is considered as Roff while the doped is Ron and the total resistance obtained is:

$$R_{total} = \boldsymbol{R_{on}}.\frac{\boldsymbol{W}}{\boldsymbol{D}} + \boldsymbol{R_{off}}(\mathbf{1} - \frac{\boldsymbol{W}}{\boldsymbol{D}}) \quad \ldots (8)$$

Where W=doped region, D= length of device. Here, LRS (low resistance state) and HRS (High Resistance state) is dependent on doping and direction of the current flow.

Suppose if a sinusoidal input is applied to memristor element with smaller amplitude like 300mV in Fig. 1(c), and current passes through the element is shown with around 35uA at a frequency of 1KHz. Hysteresis loop obtained by analyzing the TiO_2 based memristorat V-I characteristics is described in Fig. 1(d) reports the memristive behaviour of device even at lower voltage, *i.e.*, 300mV. The pinched hysteresis loop decreases with increase in frequency and tends to become linear acting as a resistor. The

simplicity of the element attracts the interest in researcher where its behaviour is dependent on the states describing maximum and minimum resistances.

3 Design methodology

The design and evaluation of Memristor based SRAM cells at subthreshold region of operation are performed using LT spice[18] .The SPICE model of memristor is used from[19]. The Memristor device parameters are taken from[19] used in the memory cell is described in Table. 1. It is exhibiting hysteresis loop voltage-current curve passes through origin depending on input frequencies as described in[19-21]. Also, the proper sizing of Driver transistor is responsible for a drastic change in the value of SNM. The Cell Ratio and Pull up Ratio affects the stability of the SRAM Cell [22]. W/L ratiois used from the Ref.[23]. SPICE PTM model of MOSFETs at technology of 32nm[24] are used in the simulation. Area of memristor has been analyzed in[25], which describes that it takes less space than CMOS and compatible with CMOS technology is explained in[26]. The threshold voltage of MOSFETs used in the work is Vth=0.65Volts. Graphical and Mathematical ways for calculating delay is referenced from[27] and power reduction technique is obtained by using sub threshold concept.

4 Results and Discussions

In this section, firstly the existing SRAM Cells incorporating the memristors discussed in[10-17] are evaluated for subthreshold application. This part explains the working of 6T2M and 7T1M and its behavior in terms of speed, stability and power. Both 6T2M and 7T1M circuits are supplied with lower voltage V_{DD}=0.3V and V_{DD}=0.4Vare made to work in subthreshold region where supply voltage is lower than threshold voltages of MOSFETS which changes its behaviour drastically and power-hungry circuits are controlled to the greater level. Memory operation with low voltage is attractive but challenges are also high at the same time, so this paper explores the limit of low voltage operation and proposes new memristor based circuit (Proposed 7T1M SRAM cell) with better efficacy. This simulated work of 6T2M, 7T1M and proposed 7T1M at subthreshold voltage is finally compared for different performance parameters as presented in Table 2.

Table. 1 — Memristor element parameter.

Device parameters	Description	Magnitude
R_{on}(ohm)	Min. memristance of memristor	1K
R_{off} (ohm)	Max memristance of memristor	*100K*
Vth(volts)	Resistive switching threshold	*0.3V*
R_{init}(ohm)	Initial Resistance	*80K*

4.1 6T2M SRAM cell

Working in subthreshold region of 6T cell without memristor is demonstrated in[3,4,6,7] where supply voltage is lower than threshold voltage. Memristor based 6TSRAM cell structure is shown in Fig. 2 and its other structure of 6T2M is demonstrated in[10,11] where memristor connection have been adjusted. In

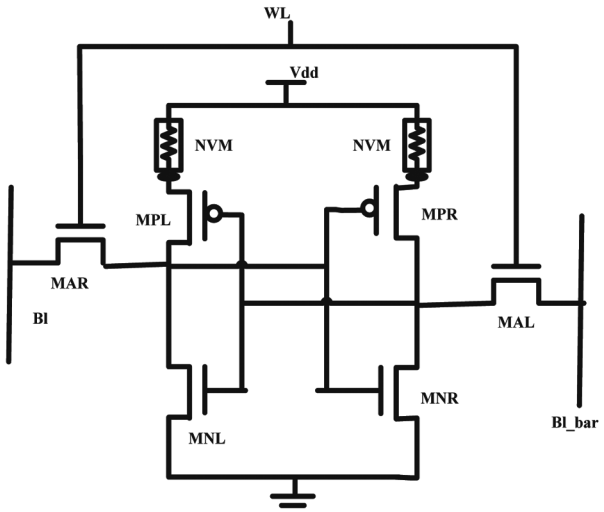

Fig. 2 — 6T2M SRAM cell at subthreshold.

Table. 2 — Comparison of simulated result at subthreshold voltage (this is new work of SRAM cell with memristor at subthreshold.

Parameters	6T SRAM Cell in the subthreshold region [7]	6T2M SRAM Cell [11] Evaluated in the Subthreshold region	7T1M SRAM Cell[12] Evaluated in the Subthreshold region	Proposed 7T1MSRAM Cell in the Subthreshold region
Read delay at 0.3V	321 ps	494 ps	330 ps	350 ps
Write delay at 0.3V	fail	540 ps	490 ps	450 ps
RSNM at 0.3V	fail	58 mV	25 mV	65 mV
WSNM at 0.3V	fail	60 mV	85 mV	105 mV
read Power Dissipation at0.3V	1720.5 uW	850 uW	13.05uW	8.56uW
write power dissipation at 0.3V	-	750uW	313uW	102uW
Memristance	Nomemristor	11K ohm	400K ohm	4G ohm

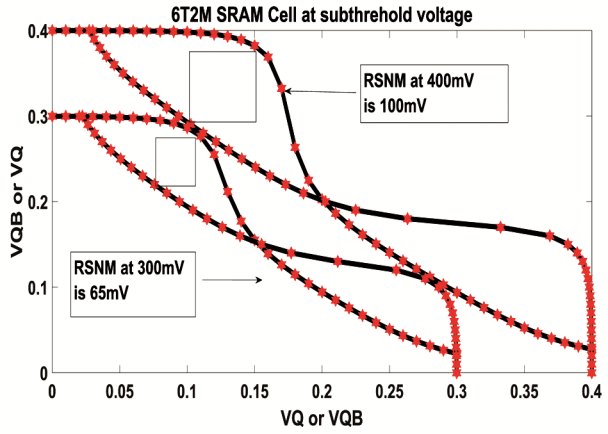

Fig. 3 — RSNM of 6T2M at V_{DD}=0.3V and V_{DD}=0.4V.

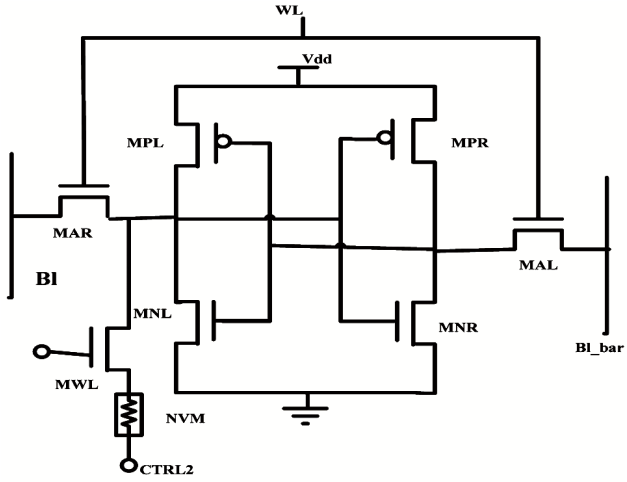

Fig. 4 — 7T1M SRAM cell at subthreshold.

Fig. 2, connection of memristor proves to very fruitful since researchers have explained in[3-9] that 6T SRAM cell fails to work at lower voltages, doesn't function writability operation and affected by process variations. However, since the connection of memristor is direct to the supply voltages, it consumes more power due to direct power supply but has proper read/write functioning after simulation and its RSNM is calculated and shown in Fig. 3 to compare its results further. Fig. 3 shows Read static noise margin of 6T2M which was not in a condition to perform basic operations at such low voltage earlier in existing work.

4.2 7T1M SRAM cell

The work of 7T1M SRAM cell is explained in[12], where it is seen that 1T1M (one transistor with one memristor) is connected directly to one of the nodes and memristor is controlled by MWL as shown in Fig. 4. This connection is basically for storage purpose during the state of read/write operation. Discussion of proper sizing of transistors and its layout design are discussed in[11,12].

The asymmetric designof SRAM cell (7T1M) compared to other SRAM cells, such as, 6T2M[10], 7T2M[15], 8T2M[16] (symmetric design SRAM cells)leads to change in capacitance at the internal nodes, however this circuit has advantages of reducing the complexity comparatively. Fig. 4 is simulated at subthreshold voltage and its behaviour is analyzed at V_{DD}=0.3V to reduce the leakage powerand total power dissipation of the circuit during set and reset state and moreover taking the advantage of non-volatile element.

Read and write operation is performed at various lower voltages, out of which one at V_{DD}=0.3V is described in Fig. 5 explaining the reset and store process during simulation for read/write operation and read SNM is shown later. In the Fig. 5, behaviour of signals is shown in such a way that change in memristor resistance occur according to the change in control signals applied to the 1T1M. First of all, ctrl1 and ctrl 2 is applied high with slight difference turning on MWL and at this point V_{DD} is not applied, memristor is already at high state, reset is not required and if the memristor is at low state, voltage at node will rise due to application of high voltage at ctrl1 and ctrl2, memristor will change from LRS to HRS taking device to reset.

During write operation, access transistors are ON and complimentary data on bit line BL is written on node VQ turning ON MWL programs memristor depending on storage voltage changing its state from high resistance to low completing writing process to the 6T core. Depending on the storage node, writing occur. If VQ=1 VQB=0, memristor is in LRS.

During read operation, Bit lines are high, turning on MWL in similar way, with high power applies to the cell. When memristor is in LRS like in write case, storage node VQ remains at logic'1' but other node discharges through the transistor. When memristor is in the HRS state, there will be increase in voltage node VQ and this fast voltage discharges VQ disturbing another transistor creating difficulties and hence restore of one part is difficult due to asymmetric cell design. Due to asymmetric design of the cell, resistance at memristor is larger at one point of time disturbing capacitance as well as store and restore process and causing rise in average delay at lower voltage.

Static Noise margin is an important parameter for the robustness and stability of the memory cell and it is calculated by voltage transfer characteristics (VTC) of the storage nodes which is complimentary to each other to understand the tolerance level of the noise in it. Coming to the existing work of 7T1M[12], memristor is controlled by transistor MWL depending upon node voltage, when transistor is OFF during read operation in Fig. 4, effect of memristor is almost neglected and so Read SNM is not good in[12] rather focused on improvement of WSNM, but in this work, both RSNM as well as WSNMis focused aiming to overcome the challenges faced in existing one with reduced power dissipation.

RSNM and WSNM of 7T1M is shown in Fig. 6 and Fig. 7 respectively at V_{DD} = 300mV and

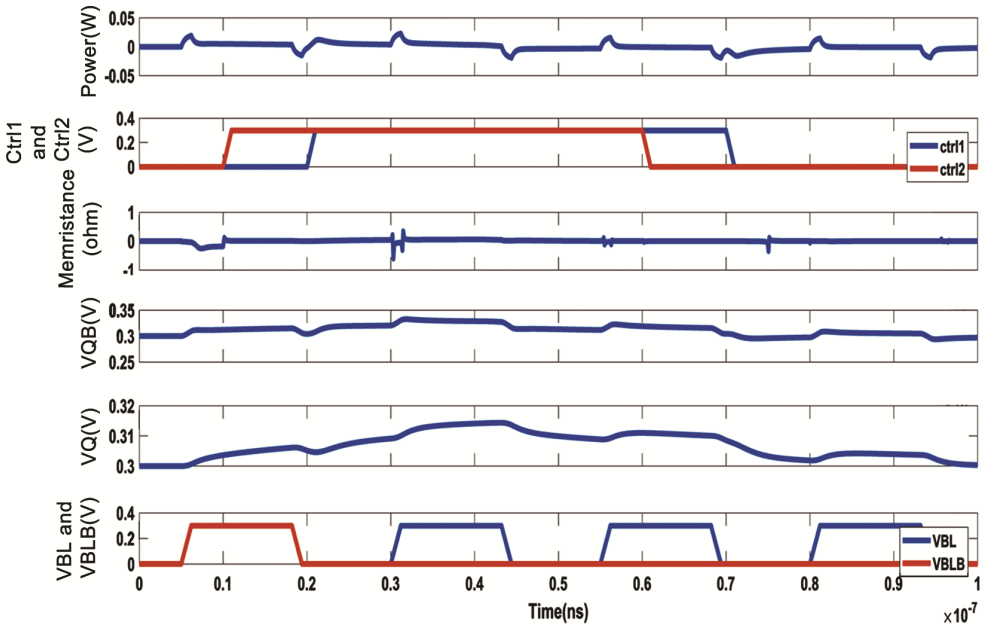

Fig. 5 — Simulation of 7T1M SRAM cell at subthreshold voltage with VDD=300mV.

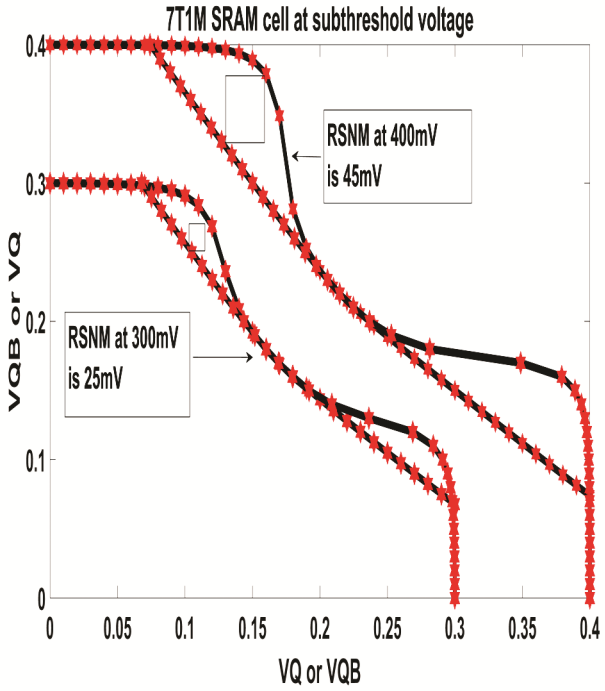

Fig. 6 — RSNM curve of 7T1M cell at subthreshold voltage at V_{DD}=300mV and V_{DD}=400m.

V_{DD}=400mV and it is observed, RSNM and WSNM obtained is very low at lower voltage and values are described in Table 2. So it concludes that 7T1M doesn't have good stability working at lower voltage and there is always trade-off between parameters and such combinations can only be used according to the application of the system. This RSNM needed a requirement for the modification in the circuitto get better read SNM as well as write SNM at lower voltage for better stability.

4.3 Proposed 7T1M SRAM cell

In the proposed work, Fig. 7 displays the proposed 7T1M SRAM Cell Schematic (modified), where MAR is access transistor to perform the access write connected to the word line (WL) and MAR connected to the read line (RL) to perform the read operations. Also, it consists of two CMOS inverters connected to each other by an additional NMOS transistor (MWL) having controlling signal CTRL1 and transistors (MAR and MAL) connected to bit lines (BL) and bit line bars (BLB) respectively. Two control signals ctrl1 and ctrl2 are connected in conventional work but here in the proposed circuit, ctrl2 is connected to memristor andmemristor is directly connected to the node Q instead of connecting to the transistor in the previous case. So, direct connection of additional transistor and memristor to the storage node makes it controlling. The proposed 7T SRAM cell depends on cutting off the feedback connection between the two inverters (inv1 and inv2). An additional NMOS transistor MWL performs the feedback connection and disconnection and the cell relies solely on BLB to perform a writing operation before any writing process.

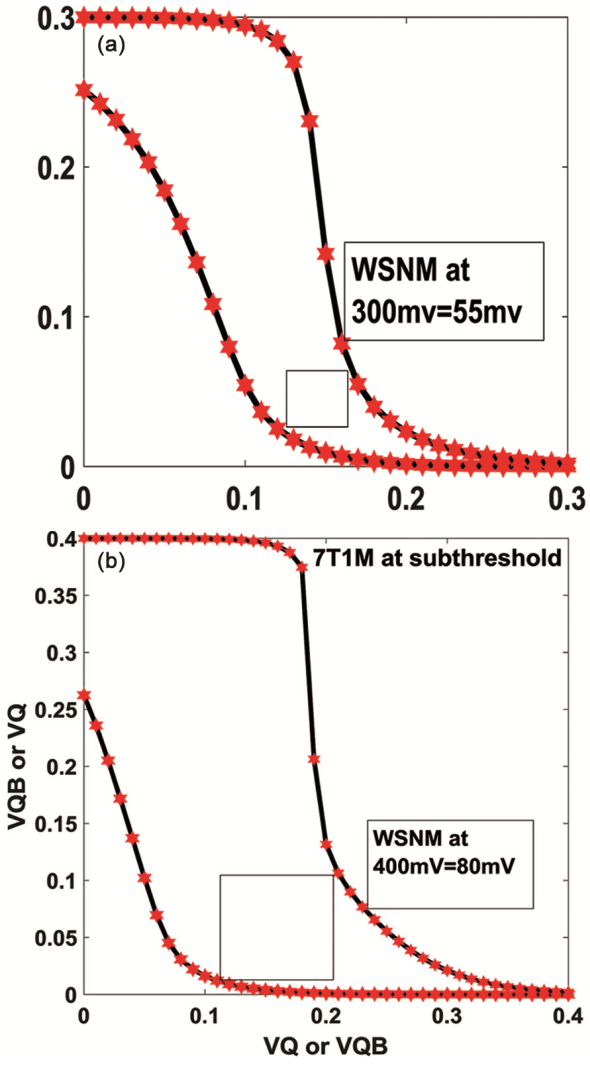

Fig. 7 — WSNM curve of 7T1M cell at subthreshold voltage at V_{DD}=300mV and V_{DD}=400mV.

It is demonstrated that during read operations, both the word line (WL) and the read signal RL are enabled in the read operation of the 7T SRAM cell, while the transistor MWL is kept ON. When QB= 0, the read path is made up of MNL and MAL transistors and works like a typical 6T cell. When QB = 1, MNR, MWL and MAR transistors become the read path. In this way, three transistors are connected in series, which, unless these transistors are carefully sized, decreases the cell's driving capability.

The 7T SRAM cell's write operation begins by turning off the MWL transistor, cutting off the feedback connection. BLB has input data which is compliment of it, MAR is kept ON and MAL is kept off. This type of SRAM cell identifies like two cascaded inverters in sequence where one inverter is followed by another, MAR access transistor transfers the BLB data to which inv2, MNL and MPL drives to develop QB, the cell data. Likewise, QB drives inv1, MNR and MPR, to construct Q. Then to reconnect the feedback link between the two inverters and to store the new data, the word line (WL) is switched off and transistor MWL is turned ON.

Simulation waveform of the proposed circuit is described in Fig. 8 where WL and RL is taken separately to calculate the average delay during the operation. Ctrl1 and Ctrl2 signals have been used same as in the previous simulation results in Fig. 5, according to which node voltages have been calculated. From the behaviour, it is clearly observed that VQ and VQB are the node voltage signals is

almost opposite to each other which is improved and better in functioning, and through which delay, memristance and power dissipation is calculated. Simulation is done at subthreshold voltage like previous circuit (7T1M) and compared with existing to seek the improvement.

Figure 9 shows the RSNM behaviour of proposed SRAM cell which describes the butterfly curve calculated at V_{DD}=0.3V and $V_{DD=}$ 0.4V where maximum square obtained in the curve is better and improved compared to previous 6T2M and 7T1M at subthreshold. Coming to WSNM, the modified structure has also shown its WSNM calculation in Fig. 10 calculated at V_{DD} =0.3V and $V_{DD=}$ 0.4V where it concludes that proposed circuit has improved RSNM as well as WSNM. In this previous analyzed work, when simulated the 7T1M at lower voltage, RSNM was very less and it is also very low like basic 6T cell when seen in 7T1M[12] and so work is focused on only WSNM. This paper aims to improve this RSNM at lower voltage in order to improve not only RSNM/WSNM but also power and delay of the circuit. Since in existing circuit of 7T1M in[12], transistor is connected to memristor and due to its controlling and dominating nature, it deactivates during read operation giving low RSNM. But in the modified circuit, transistor MWL is replaced and connected as feedback connection between the inverters with separate read and write lines obtaining better and improved RSNM/WSNM.

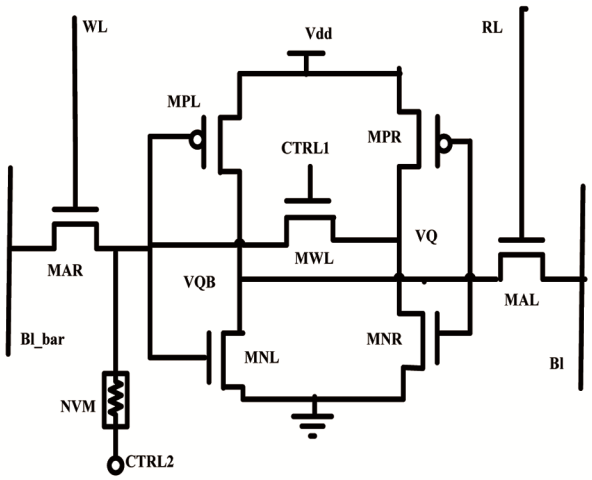

Fig. 8 — Proposed 7T1M SRAM cell working at subthreshold voltage.

Table 2 describes the final comparison of the results which includes delay, power and RSNM/WSNM comparison at V_{DD}=0.3V for the structures 6T2M, 7T1M and proposed 7T1M SRAM cells. The simulation result shows the improved read and write SNM by 61% and 23% respectively when compared with the existing 7T1M structure[12] evaluated at V_{DD}=0.3V. Power dissipation of the proposed SRAM cell reduces approximately 66% compared to exiting 7T1M SRAM cell at read/write condition and nominal Delay obtained in the same range which is quite good for the memory cell. Total memristance is also calculated where proposed work is having higher memristance value. High memristance gives high WSNM described in[15]. Also, 6T does not perform read and write operation properly at this low supply voltage, write is complete failure, so only power dissipated during read is mentioned in the Table 2.

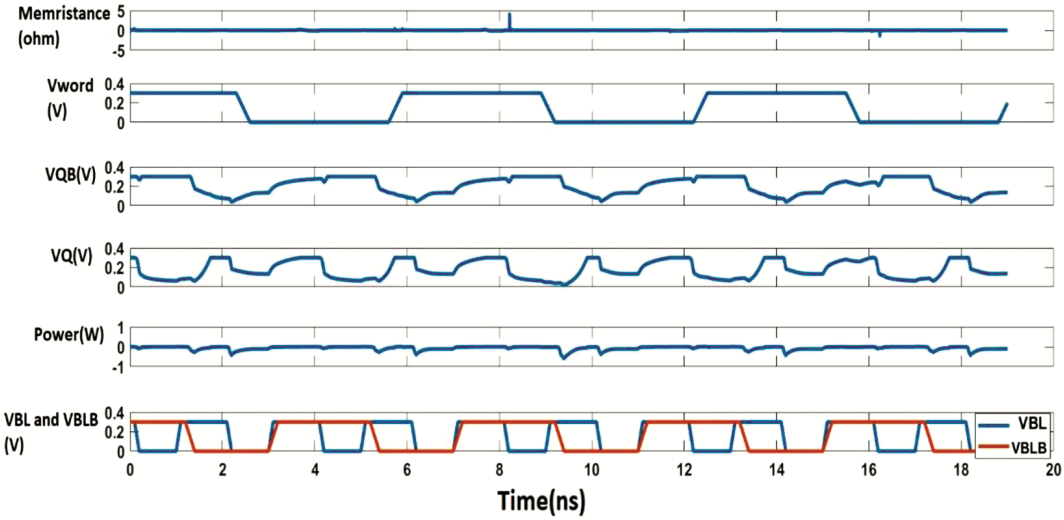

Fig. 9 — Simulation waveform of proposed SRAM cell at VDD=300mV.

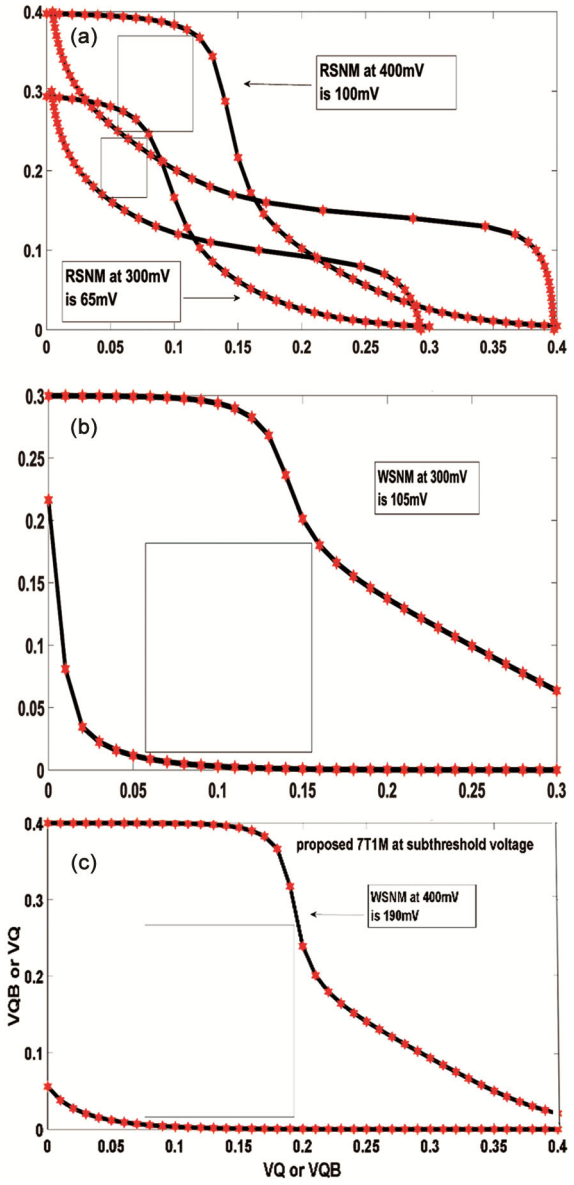

Fig. 10 — (a) RSNM(Read static noise margin) behaviour of proposed SRAM cell at VDD=300mV and VDD=400mV (b) and (c) WSNM behaviour of proposed SRAM cell at subthreshold voltage of VDD=300mV and 400mV.

5 Conclusion

This paper has presented a modified structure of 7T1M cell which is simulated and analyzed at subthreshold voltage at V_{DD}=0.3V and 0.4V where power consumption is reduced rapidly at lower voltage. Stability of the SRAM structure is well improved by using an additional NMOS transistor in the proposed circuit in terms of RSNM and WSNM which was nominal in the conventional 7T1M as discussed in the paper and has focused on RSNM/WSNM as well as power and Delay. This paper has targeted to support for low voltage applications even under subthreshold regime. Working with SRAM cell using memristor at subthreshold voltage is new thing discussed in this paper. In mobile and storage usage, such beneficial SRAM structures are useful with low power, average delay and improved SNM.

Author Declarations

Ethics approval and consent to participate: This article does not contain any studies with human participants or animals performed by any of the authors. In this research, we did not collect any samples of human or animal.

Consent for publication: not applicable (as results does not involve human or animal)

Availability of data and materials: The above mentioned authors have all the relevant data associated with this research work and will be shared if asked in the future. Competing interests: The authors have no relevant financial and non-financial interests to disclose. Funding: No funding was received to assist with the preparation of this manuscript.

Authors' contributions: All author contributed to the study conception and design. Author1 has performed the spice simulations and analysis, calibrated the results and wrote the paper. Author 2 and author 3 has conceived the design, contributed in analysis data and tools/software and formatted and edited as required. Have shown all efforts to obtain results of new element in memory cell of the research. All author read and approved the final manuscript.

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Compliance with Ethical Standards:

Disclosure of potential conflicts of interest: The authors have no conflicts of interest to declare that are relevant to the content of this article. Research involving Human Participants and/or Animals: No Involvement of human or animal. Informed consent: Yes, All authors have consent in this research work

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