

Harmonic Minimization using a Cascaded Multilevel Converter for a Standalone Renewable Energy System

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Received: 27th November 2025; accepted: 10th August 2026

Effective power conversion is necessary when integrating photovoltaic (PV) systems into the electrical grid to manage high voltages, minimize switch stress, and improve power quality while reducing the need for intensive filtering. The advantages of multilevel inverters (MLIs), especially cascaded H-Bridge (CHB) designs, in lowering electromagnetic interference (EMI) and increasing efficiency have made them essential for renewable energy systems. This work proposes a DC-AC-DC-AC converter system with seven-level and thirteen-level topologies. The seven-level converter system is designed and simulated in MATLAB/Simulink using phase-shifted pulse-width modulation (PSPWM) and level-shifted pulse-width modulation (LSPWM) to analyze total harmonic distortion (THD) and determine the best modulation technique for a grid-connected standalone system. The study finds that the thirteen-level converter showed improved power quality and system efficiency, with a significant decrease in THD to 0.43 % after filtering. Real-time simulation on the OPAL-RT platform confirms the adaptability and efficacy of the presented approach in real-world situations. Furthermore, incorporating more reliable and compact medium-frequency transformers supports environmental sustainability by enhancing energy efficiency, reducing material consumption, and supporting modularity for easier maintenance.

Keywords: Multilevel inverter, Phase-shifted pulse-width modulation, Level-shifted pulse-width modulation, Total harmonic distortion, Photovoltaic system, Cascaded H-bridge

1 Introduction

In the renewable energy and electric drive sectors, there's a growing focus on efficiently handling high voltages, reducing switch stress, and maximizing output voltage to minimize the need for extensive filtering. Among these renewable options, Photovoltaic (PV) energy has garnered considerable attention during the same timeframe. Power converters play an important role in integrating renewable energy sources with the grid¹⁻³. Power converters are essential for managing high voltages, reducing switch stress, and enhancing output quality.

Multi-level inverters (MLIs), such as neutral point clamped (NPC), flying capacitor converters (FCC), and cascaded H-bridge inverters, are favored over two-level inverters due to benefits like reduced harmonics and interference, improved voltage level, and efficiency⁴⁻⁷. Various multi-level inverters, such as five-level, seven-level, nine-level, thirteen-level, and many more, have been investigated and evaluated in the literature^{8,9} for different conversion systems of renewable energy sources to find suitable topologies

and control strategies for stand-alone systems as well as for grid-integrated systems. Among these MLIs, the cascaded H-Bridge (CHB) configuration has become crucial due to its efficiency, scalability, robust fault tolerance with modular structure, freedom from capacitor balancing issues, and less electromagnetic interference¹⁰⁻¹².

CHB-MLIs employ various pulse width modulation (PWM) techniques to improve performance and minimize THD^{13,14}. PWM techniques, such as level-shifted PWM (LSPWM) and phase-shifted PWM (PSPWM), are essential for optimizing performance and improving output quality. Multiple PWM approaches within the LSPWM category, such as phase disposition (PS), phase opposition disposition (POD), and alternate-phase opposition disposition (APOD), are classified according to carrier displacement¹⁵⁻¹⁷.

In LSPWM-modulated CHB-MLIs, irregular switching may result in unequal power distribution from DC sources¹⁸. Although PSPWM provides equitable power distribution, it increases switching losses¹⁹⁻²⁰. Conversely, LSPWM encounters challenges related to unequal power distribution

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inconsistencies across cascaded modules and harmonics at multiples of the switching frequency, which may require larger filters^{21,22}.

These power converters also induce harmonic distortion during switching, impacting power quality in a photovoltaic (PV) system. Different filters like LCL, LC, active filters, etc., are frequently used to reduce these harmonics. Among various passive filters for solar inverters, LC filters are most commonly used for off-grid systems, as they are smaller and have less cost²³. However, it isn't very easy to determine suitable parameters for this filter. So, optimizing the parameters of the LC filter is essential to reduce residual harmonics after conversion, ensuring the system meets grid standards and overall power quality²⁴⁻²⁵.

Another concern related to this interface is the size of the converter system, as power transformers are fundamental components in this conversion system, enabling efficient voltage conversion and galvanic isolation. Traditionally, line-frequency transformers are used²⁶, but technological advancements have facilitated the development of transformers operating at medium frequencies (400 Hz to 100 kHz)²⁷. These medium-frequency (MF) transformers can reduce the overall size of the converter system²⁸⁻²⁹. Still, their integration with MLIs and the associated control strategies for maintaining power quality and grid synchronization remain underexplored.

To overcome the above-stated concerns, a thirteen-level converter system with a medium-frequency (MF) transformer is developed to improve harmonic performance and reduce system dimensions³⁰⁻³³. This paper addresses several control issues related to sophisticated power conversion systems. It focuses on selecting and refining PWM approaches to maximize output quality and reduce total harmonic distortion (THD) while effectively controlling many switches in intricate multilayer topologies to guarantee synchronized operation³⁴. Various PWM techniques are applied to a seven-level converter system to identify a suitable technique for use in a thirteen-level converter system. This converter configuration enhances power quality, reduces total harmonic

distortion (THD), and ensures seamless grid synchronization for renewable energy systems.

The primary control challenges addressed include harmonic distortion, uneven power distribution across H-bridge cells, and synchronization issues under asymmetric conditions caused by unequal solar irradiation on different PV modules. The proposed thirteen-level CHB converter system, integrated with optimized PWM techniques (such as PSPWM and LSPWM), ensures uniform switching behavior and synchronized operation of all modules. This minimizes total harmonic distortion (THD), balances switching losses, and improves overall grid compatibility even under asymmetric operating conditions.

As the global energy system shifts toward renewable sources, power conversion technology must also align with environmental objectives. The proposed DC-AC-DC-AC converter topology helps achieve this objective by minimizing THD, which improves energy efficiency and lowers losses. Furthermore, the use of an MF transformer reduces material consumption and system size, lowering the impact of large-scale deployment that supports environmental sustainability.

2 Materials and Methods

2.1 Proposed DC-AC-DC-AC Converter System

The proposed converter system shown in Fig. 1 has these stages: The push-pull converter converts DC voltage into medium-frequency AC voltage. Second Stage: The obtained AC voltage is stepped up using a medium-frequency (MF) transformer. Third Stage: A center-tap rectifier converts the medium-frequency AC (MF-AC) into DC. Final stage: This DC voltage is directed into a cascaded H-bridge (CHB) multilevel inverter, converting it into AC voltage at line frequency.

Phase-shift and level-shift PWM techniques are used to evaluate the performance of the seven-level converter system to choose a suitable modulation technique for the thirteen-level converter system. After analyzing the THD spectrum using these modulation techniques, the study proposes a thirteen-level structure of DC-AC-DC-AC converters for grid

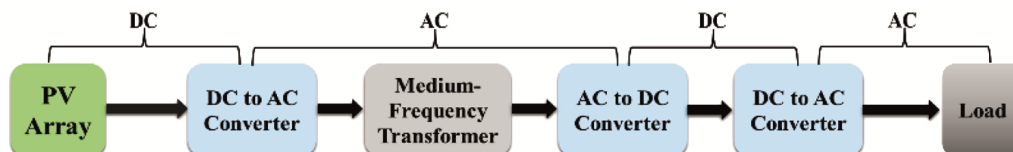


Fig. 1 — Proposed converter system

integration of a stand-alone system. A medium-frequency (MF) transformer is introduced to make the complete converter system smaller, replacing a line-frequency transformer. The size reduction is due to the design of the medium-frequency transformer, which operates at 400 Hz compared to a 50 Hz line-frequency baseline, resulting in an 8:1 frequency ratio. By Faraday's law ($E = 4.44 f N A_c B_{\max}$), core cross-section turns scale inversely with frequency for a fixed voltage and flux density, i.e., the same voltage rating is achievable with roughly an eighth of the core area and turns product before accounting for winding/insulation losses. The suggested architecture enhances the overall power quality for a stand-alone system with lower harmonics.

2.2 Seven-Level Converter System

A seven-level converter system, as shown in Fig. 2, to evaluate suitable modulation techniques. It also sets

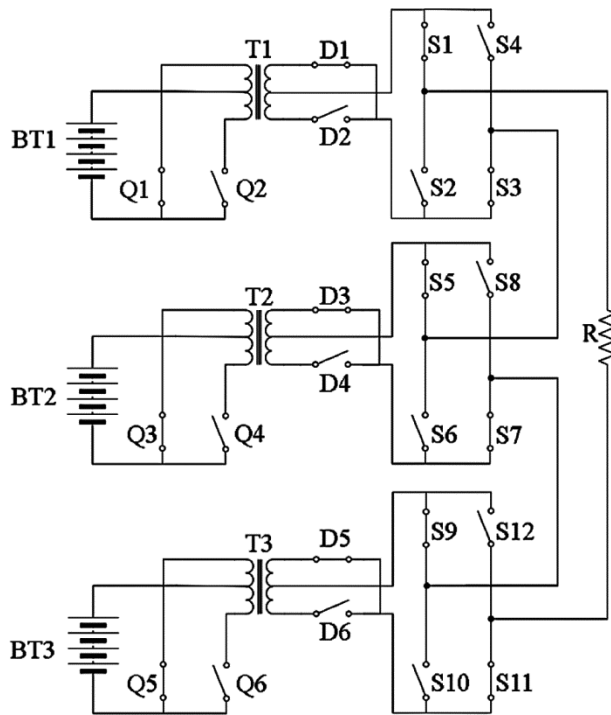


Fig. 2 — Schematic Diagram of Seven-Level Converter System

the reference for outcomes such as THD, power quality, and efficiency for the more complicated thirteen-level converter.

The three DC voltage sources (BT1, BT2, and BT3) provide the input DC voltage. Following this, the push-pull converter comprises six Insulated Gate Bipolar Transistor (IGBT) switches named Q1 to Q6, which convert the input DC to MF-AC. Three MF-transformers, T1, T2, and T3, are used to step up the voltage. Six diodes, D1 to D6, are used to convert this medium-frequency AC into DC to feed it to the CHB inverter, having twelve IGBT switches, S1 to S12.

The three cascaded H-bridge cells (S1–S4, S5–S8, and S9–S12), each with diagonal switch pairs (e.g., S1/S3 and S2/S4 for cell 1), produce +Vdc, –Vdc, or 0 per cell. Table 1 gives the minimal-switching-transition state for all seven levels; redundant zero-states exist for each cell (e.g., S1–S4 all commutated to the opposite same-leg pair) and are exploited by the phase-shifted carriers during real-time PSPWM operation, but the states below are the representative combination for each level.

2.2.1 Modulation Techniques Evaluation

In the CHB inverter, PWM techniques such as PSPWM and LSPWM methods like PD-LSPWM, POD-LSPWM, and APOD-LSPWM are compared to evaluate the seven-level converter system's performance. The phase-shift PWM technique involves producing a slight phase shift between the carriers, which causes the first harmonic band to rise gradually into the harmonic spectrum's upper region. However, a high-frequency triangle carrier is efficiently integrated or contrasted with the modulating waveform to produce these voltages. The waveforms produced by each bridge using phase shift PWM are the same, as shown in Fig. 3. They can be coupled to provide a high-quality sine wave output. Using this method, the converter's switching patterns can be successfully controlled to produce a desired sinusoidal waveform. The harmonic performance of PSPWM depends on

Table 1 — Switching sequence of switches for a seven-level converter system

Level	V (kV)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+3	+13.2	1	0	1	0	1	0	1	0	1	0	1	0
+2	+8.8	1	0	1	0	1	0	1	0	0	1	1	0
+1	+4.4	1	0	1	0	0	1	1	0	0	1	1	0
0	0.0	0	1	1	0	0	1	1	0	0	1	1	0
-1	-4.4	0	1	0	1	0	1	1	0	0	1	1	0
-2	-8.8	0	1	0	1	0	1	0	1	0	1	1	0
-3	-13.2	0	1	0	1	0	1	0	1	0	1	0	1

*1 = ON, 0 = OFF. Complementary devices within each leg (e.g., S1/S2, S3/S4) are always at least one device off to avoid shoot-through

the cross-cancellation of harmonic-sideband components among bridge cells.

Level-shifted PWM involves applying a vertical or level shift to the carrier signals. This method switches every cell in the converter using a single reference waveform. In the converter, each cell or H-bridge has a unique carrier waveform, i.e., the vertical offset or shift between these carrier waveforms. The switching instances of the cells are changed to produce the correct output waveform by applying the vertical shift to the carriers. Three types of level-shifted PWM exist: PD-LSPWM (Phase Disposition Level-Shifted PWM), POD-LSPWM (Phase Opposition Disposition Level-Shifted PWM), and APOD-LSPWM (Alternate-Phase Opposition Disposition Level-Shifted PWM).

In PD-LSPWM, all carrier signals are level-shifted while retaining the same phase. This indicates that the positive and negative carrier signals change by the same amount while remaining synchronized. The waveform for the PD-LSPWM for a seven-level converter architecture is shown in Fig. 4.

In POD-LSPWM, the positive carrier signals are 180 degrees (π radians) phase-shifted from the negative carrier signals^{8,9}. As a result, the positive and

negative carrier signals exhibit a phase opposition disposition, shown in Fig. 5.

In APOD-LSPWM, the phase shift of 180 degrees (π radians) alternates between the carrier signals. This indicates that all other carrier signals have a 180-degree phase shift, but the remaining carrier signals preserve their initial phase, as shown in Fig. 6.

2.2.2 Analysis of Seven-Level Converter System

A performance analysis of the seven-level converter system is first conducted using various modulation techniques to identify the best PWM technique in terms of harmonic distortion, minimal switching losses, and power quality. Simulation of the seven-level converter system for various modulation techniques has been done in this section, which presents the converter terminal voltage waveform and THD evaluation of load current and the output voltage for the seven-level converter systems.

The parameters for this converter system are

Input DC voltage = 1 kV

Switching frequency = 100 Hz

Line frequency = 50 Hz

Transformer turns ratio = 4.4

MF transformer frequency = 400 Hz

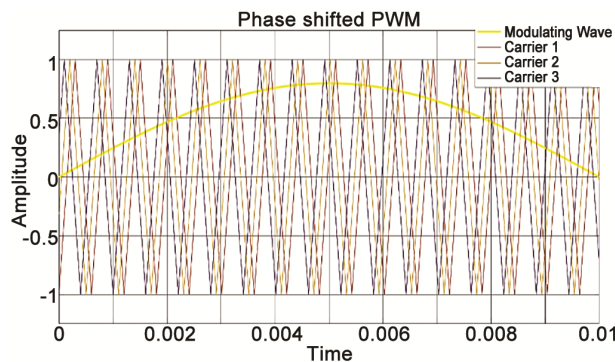


Fig. 3 — Phase-Shifted PWM

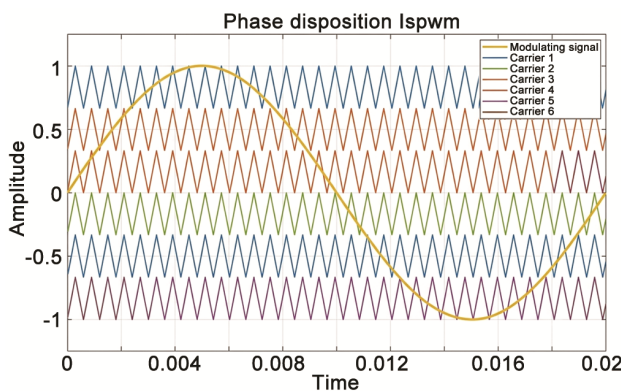


Fig. 4 — Phase Disposition LSPWM

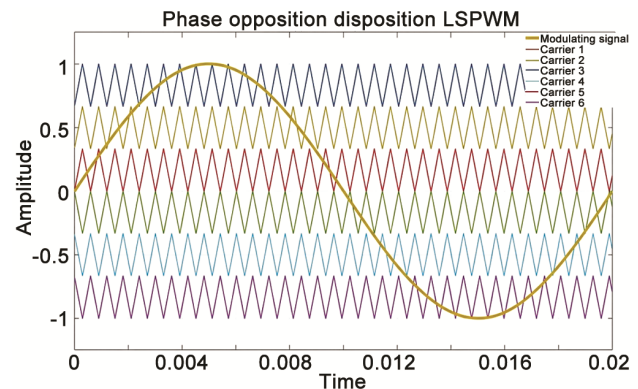


Fig. 5 — Phase Opposition Disposition LSPWM

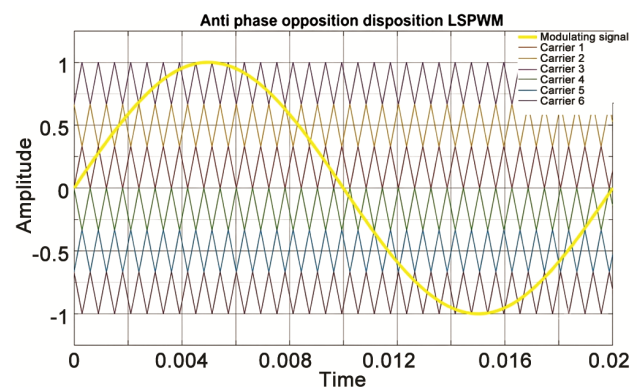


Fig. 6 — Alternate-Phase Opposition Disposition LSPWM

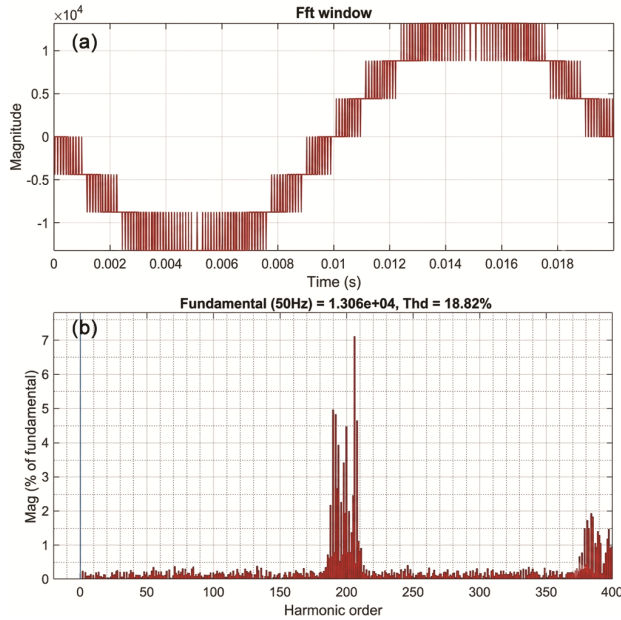


Fig.7 — (a) Output phase; and (b) THD spectrum of voltage of a seven-level converter for the PSPWM technique

Modulation index=0.99

Output levels = 7

Resistive load = 500 ohms

Output phase voltage = 13.2 kV

A phase voltage of 13.06 kV (peak) and 9.237 kV (RMS) is achieved, as displayed in Fig. 7 (a), representing the voltage at the converter terminal for the phase-shifted pulse-width modulation (PSPWM) technique. Figure 7 (b) illustrates the frequency spectrum corresponding to the THD of the phase voltage, quantified at 18.82 %.

A phase voltage of 13.05 kV (peak) and 9.22 kV (RMS) is achieved, as displayed in Fig. 8 (a), representing the voltage at the converter terminal for the phase-disposition LSPWM technique. The overall THD in the phase voltage is 18.74 %, as shown in the frequency spectrum in Fig. 8 (b).

A phase voltage of 13.05 kV (peak) and 9.22 kV (RMS) is achieved, as displayed in Fig. 9 (a), representing the voltage at the converter terminal for the phase-opposition disposition LSPWM technique. The THD in the phase voltage is 18.75 %, as shown in the frequency spectrum in Fig. 9 (b).

A phase voltage of 13.05 kV (peak) and 9.22 kV (RMS) is achieved, as displayed in Fig.10 (a), representing the voltage at the converter terminal for the anti-phase opposition disposition LSPWM technique. The total harmonic distortion in the phase voltage is 18.76 %, as shown in the frequency spectrum in Fig.10 (b).

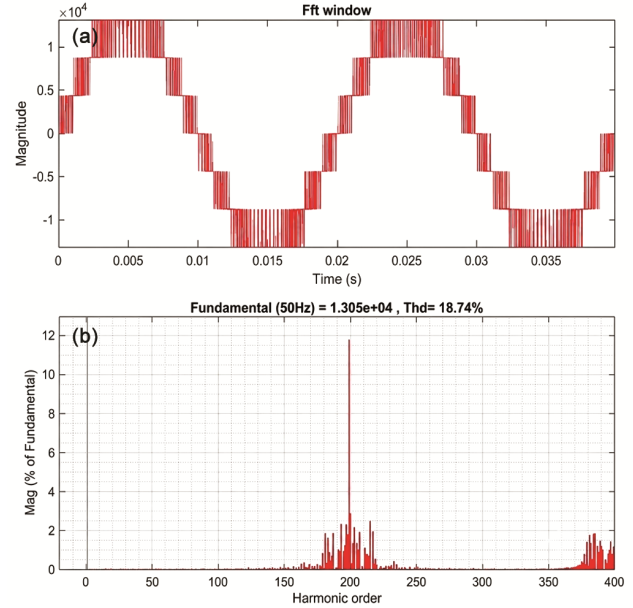


Fig. 8 — (a) Output phase; and (b) THD spectrum of voltage of a seven-level converter for the phase disposition LSPWM technique

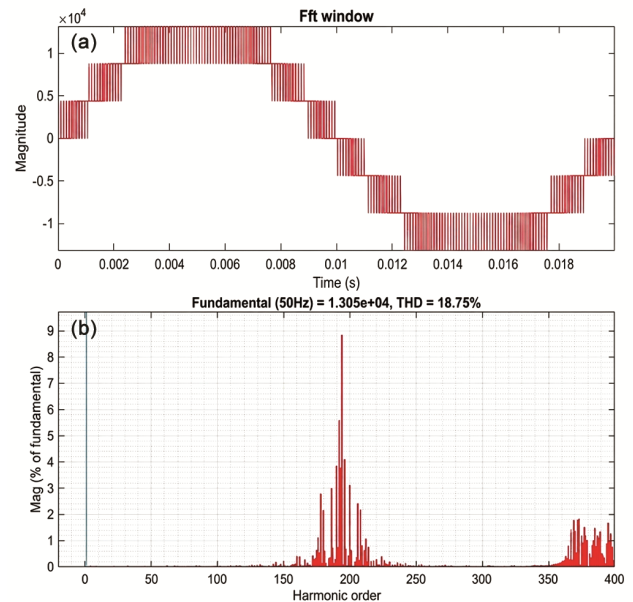


Fig. 9 — (a) Output phase; and (b) THD spectrum voltage of seven-level converter for phase opposition disposition LSPWM technique

2.3 Proposed Thirteen-Level Converter System

The thirteen-level converter system is proposed to demonstrate the variations in THD and efficiency by exhibiting the impact of elevated voltage levels on converter performance. Figure 11 illustrates the simplified configuration of the thirteen-level converter system.

The seven-level converter system with 3 cells is used only for screening purposes to rank PSPWM

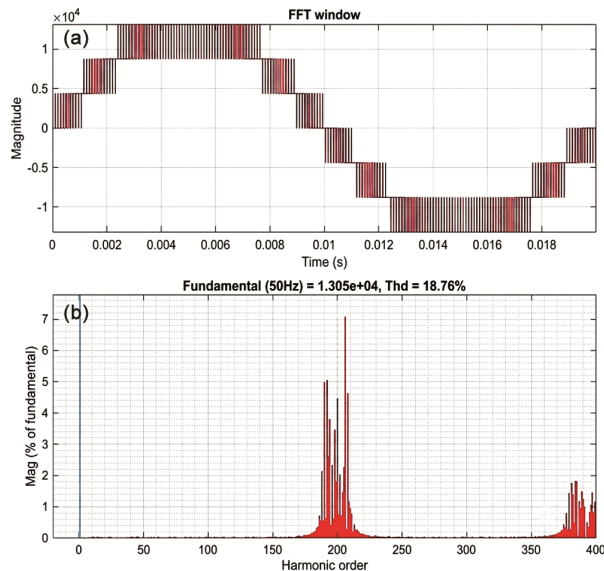


Fig. 10 — (a) Output phase; and (b) THD spectrum voltage of seven-level converter for anti-phase opposition disposition LSPWM technique

against three LSPWM techniques before going to the thirteen-level converter system with 6 cells. Doubling the cell count from 3 to 6 exactly halves the required medium-frequency transformer turn ratio ($N=4.4$ to $N=2.2$) for the same input voltage and same output voltage that nine-level or eleven-level converters do not offer. This work does not prefer nine-level and eleven-level converter systems for analysis. Table 2 below quantifies the switch/diode count trade-off across seven-, nine-, eleven-, and thirteen-level converter system options.

Six DC sources, designated BT1 to BT6, are employed to construct a thirteen-level converter system, followed by a push-pull converter with twelve switches (Q1 to Q12). Six MF-transformers (T1 to T6) provide input to the center-tap rectifier, which comprises twelve power diodes (D1 to D12), and the CHB-MLI, which consists of twenty-four switches (S1 to S24). The converter system employs IGBTs as controlled switches.

2.3.1 Parameter and Filter Design

It offers mathematical modeling for estimating the proposed multilevel converter's design parameters and capacitance-inductance values for filter design. The techniques for determining the design parameters have been covered in the literature¹⁵⁻²⁰. Equation (1) states the necessary number of independent DC sources (K) to produce an M-level output voltage.

$$K = (M - 1)/2 \quad \dots (1)$$

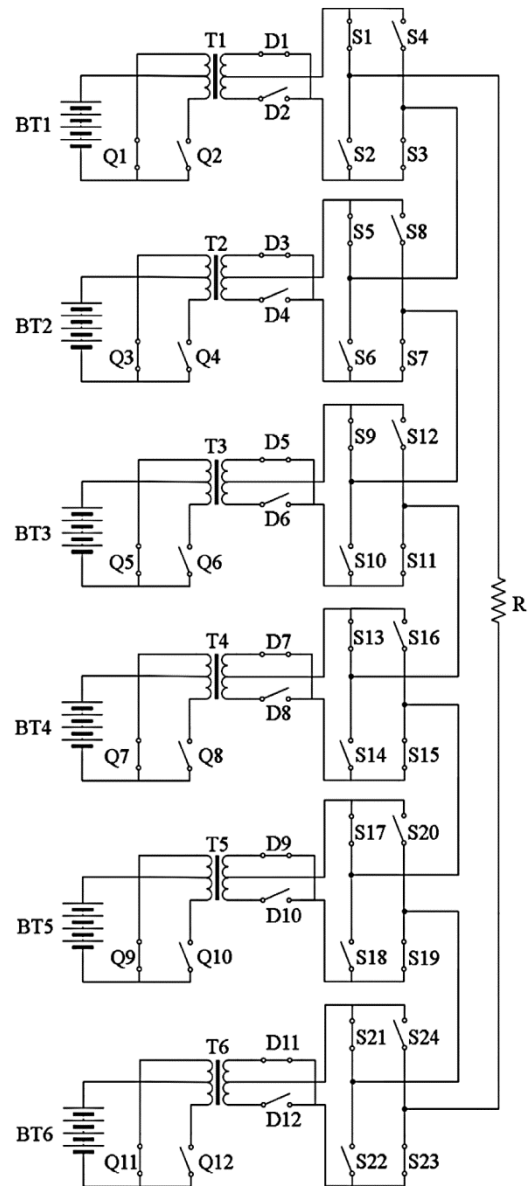


Fig. 11 — Schematic diagram of thirteen-level converter system

Table 2 — Switch/diode count for different multi-level converter systems

Levels (M)	DC sources / cells (K)	CHB switches (4K)	Rectifier diodes (2K)	Push-pull switches (2K)
7	3	12	6	6
9	4	16	8	8
11	5	20	10	10
13	6	24	12	12

Equation (2) represents the electrical system's three-phase output power, given that the star-connected load is resistive.

$$P_o = (\sqrt{3} * V_{LL} I_{ph}) \quad \dots (2)$$

Equation (3) can be used to compute the resistive load per phase.

$$R = (3 * V_{ph}^2) / P_o \quad \dots (3)$$

where; $V_{ph} = V_m \sin(\omega t)$

Equations (4) and (5) may be used to compute the voltages across the MF transformer's secondary side and the secondary's peak current as the transformer ratings and input supply are known.

$$V_2 = n * V_{DC} \quad \dots (4)$$

$$i_{2p} = \sqrt{2} * I_{ph} \quad \dots (5)$$

Equations (6) and (7) can be used to calculate the average and peak values of the current for each source, assuming no energy conversion losses.

$$I_{avg} = P_o / (K * V_{DC}) \quad \dots (6)$$

$$I_{peak} = (3 * n * i_{2p}) / \sqrt{2} \quad \dots (7)$$

For filter parameters, Equations (8) - (12) can be used to calculate the values of L and C for the filter. Variables needed to determine the LC value;

- V_f (voltage across the filter)
- V_{dc} (dc voltage directed to the converter)
- F_g (line frequency)
- F_{sw} (switching frequency)
- E_n (output voltage)
- P_n (rated power)

Equation (8) can be used to determine the current ripple with a 10% variation.

$$I_{ripplepeak} = 0.1 * (P_n * \sqrt{2}) / (3 * V_f) \quad \dots (8)$$

Using equation (9) to calculate the filter inductance may result in a reduction of 10% in the output current ripple.

$$L_i = V_{dc} / 6 * F_{sw} * I_{ripplepeak} \quad \dots (9)$$

$$Z_b = E_n^2 / P_n \quad \dots (10)$$

$$C_b = 1/2 * \pi * F_g * Z_b \quad \dots (11)$$

The maximum value of the capacitor is determined by the power factor loss in the rated output (less than 5%).

$$C_f = 0.05 C_b \quad \dots (12)$$

where; $I_{ripplepeak}$ = peak ripple current

Z_b = base impedance, and

C_b = base capacitance

The practical switching frequency in phase-shifted multicarrier sinusoidal pulse width modulation is written as;

$$F_{sw} = (m - 1) F_c \quad \dots (13)$$

where: m = number of DC sources, and

F_c = carrier frequency

Other methods provide this frequency at a different level than PSPWM. This modulation technique uses (M-1) carriers, where M is the number of output levels. All carriers have the same amplitude and frequency but provide a phase shift of $360/(M-1)$ degrees.

The filter is sized using the base-impedance method given in Eqs. (8) - (12). With these values, the filter's resonant frequency is well above the 50 Hz line frequency (avoiding interaction with the fundamental) and placed below the PSPWM carrier harmonic cluster defined by Eq. (13), which is the standard placement principle for an output LC filter. A single LC filter per phase is used in this proposed work that has materially fewer passive components than an LCL or active-filter alternative for the same duty, which results in size and cost reduction.

2.3.2 Analysis of Thirteen-level Converter System

It analyses a thirteen-level converter system to compare its output voltage, THD, and efficiency. The parameters for this converter system are;

Input DC voltage = 1 kV

Switching frequency = 1000 Hz

Line frequency = 50 Hz

Transformer turns ratio = 2.2

MF transformer frequency = 400 Hz

Modulation index = 0.832

Output levels = 13

Resistive load = 500 ohms

Output phase voltage = 13.19 kV

The filter parameters for the system are;

Filter inductance = 0.045 H

Filter capacitance = 29.61 μ F

Base impedance = 645 Ω

Base capacitance = 4.935 μ F and

Peak ripple current = 0.8189 A

Figure 12 illustrates the line-to-line output voltage of the converter utilizing the PSPWM technique, along with the THD frequency spectrum of the line-to-line output voltage waveform, which exhibits a THD of 11.50 % at the converter terminals without a filter. The RMS phase voltage is 7.618 kV, while the line-to-line output voltage measures 13.19 kV.

Figure 13 illustrates the line-to-line voltage at the filter output, indicating peak and RMS values of 18.66 kV and 13.19 kV, respectively. The overall

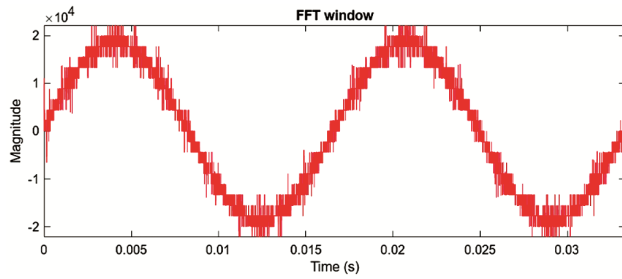


Fig. 12 — Line-to-Line output voltage of the thirteen-level converter without a filter

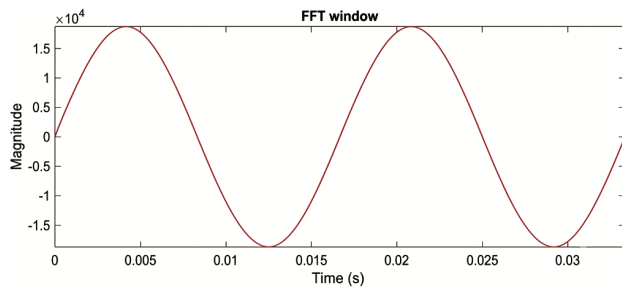


Fig. 13 — Line-to-Line output voltage of a thirteen-level converter with a filter

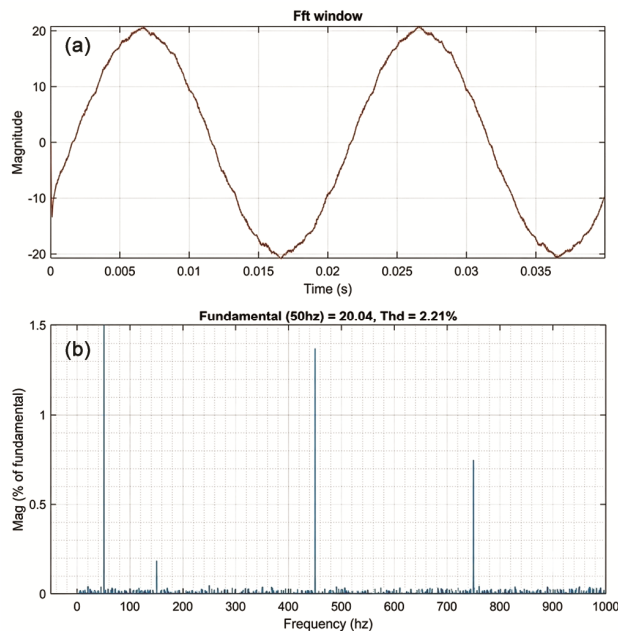


Fig. 14 — (a) Load current of a thirteen-level converter with a Filter; and (b) THD

harmonic distortion is 0.43 % in the line-to-line output voltage waveform with a filter, which is within the standard limit.

Figure 14 (a) illustrates the load current per phase at the converter output terminal, exhibiting a peak value of 20.04 A and an RMS value of 14.17 A, as influenced by the filter. The THD in load current is 2.21%, as shown in Fig. 14 (b).

Table 3 — Comparative analysis of modulation techniques

Parameter	PSPWM	PD-LSPWM	POD-LSPWM	APOD-LSPWM
Output voltage (peak)	13.06 kV	13.05 kV	13.05 kV	13.05 kV
% THD	18.82	18.74	18.75	18.76

3 Results and Discussion

This study analyzes the performance of seven-level and thirteen-level converter systems by analyzing total harmonic distortion (THD), output voltage quality, and efficiency. The seven-level converter system was analyzed using four modulation techniques: PSPWM, PD-LSPWM, POD-LSPWM, and APOD-LSPWM. The output voltage remained consistent across methods, with peak phase voltages of 13.05–13.06 kV and RMS values around 9.22–9.237 kV. The total harmonic distortion (THD) varied between 18.74 % and 18.82 %. PSPWM exhibited the highest total harmonic distortion (THD) at 18.82 % and demonstrated superior thermal management due to a more uniform switching loss distribution. LSPWM methods exhibited a lower total harmonic distortion (THD) of 18.74 % – 18.76 %; however, they encountered issues such as uneven power distribution and increased filter requirements. Thus, the PSPWM technique is found to be a more suitable and efficient modulation method for the converter system, as shown in Table 3. So, further analysis of the thirteen-level converter system is done using the PSPWM technique.

The thirteen-level converter system has shown notable advancements in harmonic suppression by using the PSPWM technique. The line-to-line voltage measured 13.19 kV, the phase voltage is recorded at 7.618 kV RMS, and the total harmonic distortion (THD) is 11.50 %. This represents approx. a 39 % reduction in THD compared to the seven-level converter system. Implementing a filter enhanced its functionality. The peak output voltage rose to 18.66 kV, the RMS voltage to 13.19 kV, and the total harmonic distortion (THD) decreased to 0.43 %, reflecting a 96.3 % reduction. The maximum load current reached 20.04 A, with a root-mean-square (RMS) value of 14.17 A and a total harmonic distortion (THD) of 2.21 %. Although the thirteen-level system introduces greater complexity and cost, the findings validate its superior harmonic suppression and efficiency. Thus, the simulation results demonstrate a notable decrease in THD and underscore the efficacy of the PSPWM method in producing smooth output waveforms with reduced

Table 4 — Comparison of efficiency					
Topology / levels	Application	THD	Efficiency	References	
13-level CHB	Standalone PV	11.50% (unfiltered) / 0.43% (filtered)	98.75%	Proposed work	
6-level, 12-switch multilevel DC link	Grid-tied, IEEE 1547	5.8%	97.59%	21	
CHB + boost front-end	Solar PV, experimental	not stated	95.68%	19	
37-level, reduced switch count	Renewable energy, experimental	1.21% (hardware)/0.8% (simulation)	93.26%	31	

THD. Table 4 provides a comparison of THD and efficiency of the proposed thirteen-level converter system with the previously published literature.

An efficiency-vs-load curve for the thirteen-level system under PSPWM is plotted from the Simulink model using its IGBT/diode conduction and switching loss blocks at four resistive loading points (25 %, 50 %, 75 %, and 100 % of the rated load) under two conditions, i.e., for PSPWM CHB only and PSPWM including losses, as shown in Fig. 15.

In addition to minimizing THD, the proposed converter system improves sustainability by lowering energy losses, which reduces thermal stress and increases component life as the PSPWM spreads switching stress equally across all six cells, cycle after cycle. No single module is repeatedly overstressed relative to its neighbors, which avoids the disproportionate, accumulated thermal cycling that drives premature device failure. PSPWM distributes switching stress equally across all cells, avoiding the repeated, disproportionate thermal cycling of a single module, which is the primary driver of CHB switch failure, thus requiring less thermal management.

3.1 Experimental Evaluation and Validation

The effectiveness of the proposed method is experimentally evaluated using a controller hardware-in-the-loop (CHIL) testbed based on OPAL-RT and a TMS320F28379D control card. The OPAL-RT real-time simulator was used to create the suggested thirteen-level DC-AC-DC-AC converter topology using the PSPWM technique in a Hardware-in-the-Loop (HIL) environment to verify the simulation results shown in Fig. 16. RT-LAB was used to combine the converter model, which was created in MATLAB/Simulink, with the OPAL-RT system for real-time execution. To ensure consistency in comparison, the experimental setup recreated the same operating conditions as those in the simulation.

The correctness of the created model was confirmed by the close match between the MATLAB-simulated findings and the real-time voltage and current waveforms acquired from the OPAL-RT platform. The line-to-line and phase voltages were

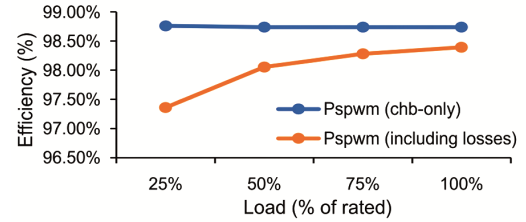


Fig. 15 — Efficiency vs. load curve

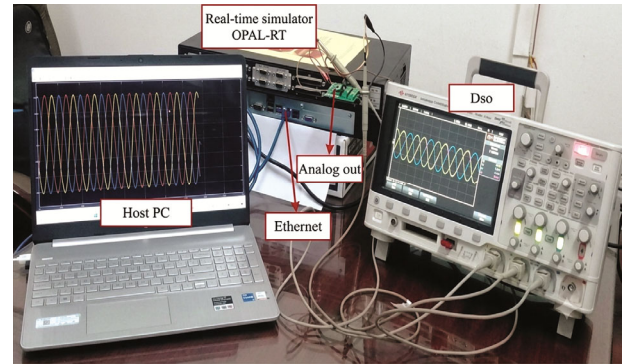


Fig. 16 — Experimental setup for the validation of the proposed thirteen-level converter system

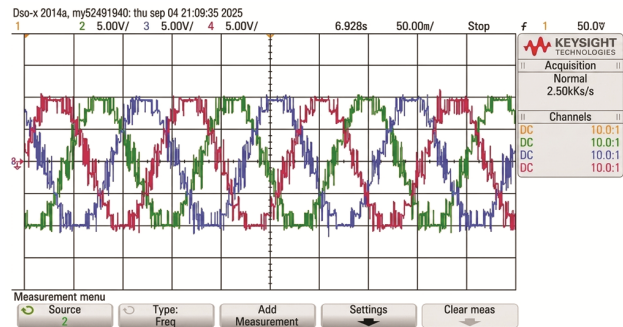


Fig. 17 — Output voltage without a filter for the thirteen-level converter system

found to retain almost the same magnitudes as those in the simulation. Due to sampling delays, switching device non-idealities, and the low resolution of the real-time interface, the observed total harmonic distortion (THD) of the output voltage was marginally higher than the predicted value. The improved harmonic suppression performance of the PSPWM-controlled thirteen-level converter was validated.

The experimental results for line-to-line output voltage without and with a filter are shown in Figs. 17

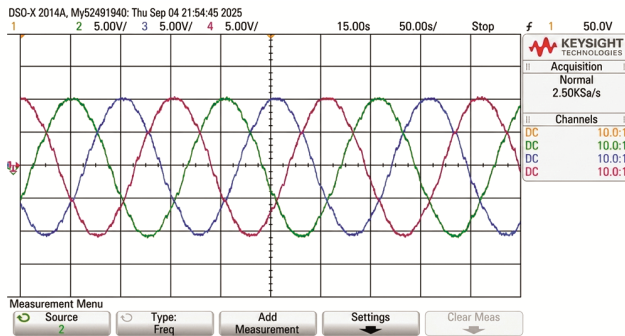


Fig. 18 — Output voltage with filter for the thirteen-level converter system

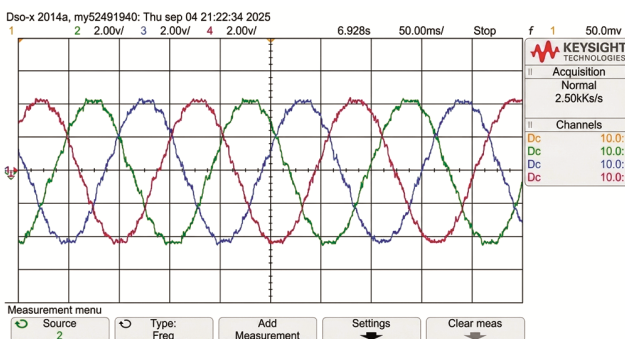


Fig. 19 — Load current without a filter for the thirteen-level converter system

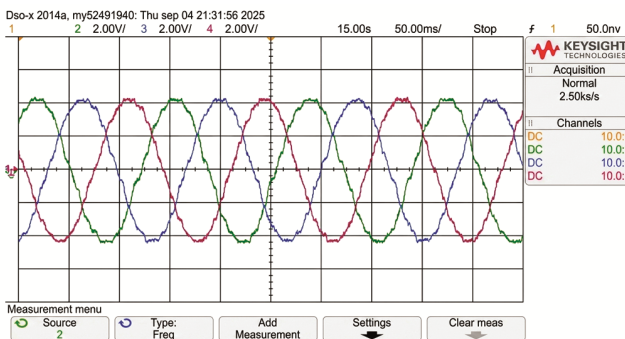


Fig. 20 — Load current with filter for the thirteen-level converter system

and 18, which are near the simulation results shown in Figs.12 and 13, verifying each other. The experimental results for load current for the thirteen-level converter system without and with filters are shown in Figs.18 and 19, respectively.

Near-sinusoidal output waveforms were achieved by adding an LC filter, which further decreased voltage and current ripple. These findings show that the suggested solution offers effective grid integration for stand-alone applications while maintaining a THD within reasonable IEEE-519 bounds. The simulation results are thus supported by the experimental results,

which also confirm the feasibility and dependability of the suggested PSPWM-based multilevel converter design for real-time operation.

4 Conclusion

In conclusion, while the THD values are similar, PSPWM exhibits marginally superior efficiency by minimizing switching losses. The independent thirteen-level DC-AC-DC-AC system for PV integration designed and evaluated in this work demonstrates reduced harmonic distortion within the specific limit and enhanced power quality relative to the seven-level converter system, especially when passive filters are employed. These results are also verified by experimental results obtained by the OPAL-RT simulator.

Along with technological advancements, the converter system takes the environment into consideration. Modularity allows for lower maintenance expenses and longer operational life, whereas medium-frequency transformers use less space and material as size reduces. Together, these characteristics encourage resource optimization and energy efficiency, which improves the sustainability of stand-alone renewable energy systems.

Thus, this thirteen-level converter configuration provides cleaner power for grid integration while offering a more compact design and improved efficiency through medium-frequency (MF) transformers. Consequently, it offers a pragmatic and efficient solution for standalone photovoltaic (PV) systems, ensuring superior power quality with reduced harmonic distortion. These converters are well-suited for renewable energy applications, significantly advancing green energy solutions by improving power conversion efficiency and sustainability.

In addition to facilitating long-term maintainability and lowering electronic waste, the CHB converter's modular design simplifies fault isolation and part replacement. The design approach complies with eco-design principles by minimizing the use of extra materials and permitting the future integration of recyclable components, even though a thorough lifecycle evaluation is outside the purview of this study.

The modular design of these converters facilitates elevated voltage levels while maintaining efficiency, corresponding with the increasing need for scalable and flexible structures in renewable energy applications. The use of a medium-frequency

transformer instead of a line-frequency transformer reduces the overall size of the entire system.

To further enhance the sustainability of the suggested system, future work will concentrate on thermal simulation, optimizing the design for recyclability, integrating life cycle effect evaluations, and creating hardware prototypes utilizing environmentally friendly materials.

References

- 1 Hossain M K, Chowdhury P, Nowshin I, Islam M R, Al-Hysam A, & Farrok O, *Energy Convers Manag*: X, 29 (2026) 101422.
- 2 Nyamathulla S, Chittathuru D & Muyeen S M, *Electr*, 12 (8) (2023) 1944.
- 3 Bughneda A, Salem M, Richelli A, Ishak D & Alatai S, *Energies*, 14 (6) (2021) 1.
- 4 Amamra S A, Meghriche K, Cherifi A & Francois B, *IEEE Trans Industr Electr*, 64 (11) (2017) 8855.
- 5 Mukherjee S, Wandhare R, Gehlot D & Krishnapriya A S, *11th International Conference on Power Systems*, (2025) 1.
- 6 Hameed S R & Al-Mhana T H, *Tikrit J Eng Sci*, 31 (1) (2024) 138.
- 7 Pushparaj N K & Nattamai Balasubramanian P, *Int J Circuit Theory Appl*, 52 (9) (2024) 4461.
- 8 Nyamathulla S, Chittathuru D & Muyeen S M, *Electr*, 12 (8) (2023) 1944.
- 9 Chakir F, El Magri A, Lajouad R, Kissaoui M, Chakir M & Bouattan O, *IFAC-PapersOnLine*, 58 (13) (2024) 478.
- 10 Kouro S, Malinowski M, Gopakumar K, Pou J, Franquelo L G & Wu B, *IEEE Trans Ind Electron*, 57 (8) (2010) 2553.
- 11 Thakre K, Mohanty K B, Kommukuri V S, Chatterjee A, Nigam P & Gupta S K, *Energy Rep*, 8 (2022) 5296.
- 12 Dhanamjayulu C & Girijaprasanna T, *Int Trans Electr Energy Syst*, 2023 (2023) 1.
- 13 Rahman S, Meraj M, Iqbal A, Reddy B P & Khan I, *IEEE J Emerg Selected Topics Power Electr*, 11 (1) (2023) 932.
- 14 Palanivel P & Dash S S, *IET Power Electr*, 4 (8) (2011) 951.
- 15 Naderi R & Rahmati A, *IEEE Trans Power Electr*, 23 (3) (2008) 1257.
- 16 Ramu V, Satish Kumar P & Srinivas G N, *Mater Today: Proceed*, 54 (2022) 710.
- 17 Tariq M, Meraj M, Azeem A, Maswood A I, Iqbal A & Chokkalingam B, *CPSS Trans Power Electr Appl*, 3 (3) (2018) 232.
- 18 Chamarthi P K, Muduli U R, Moursi M S El, Al-Durra A, Al-Sumaiti A S, & Al Hosani K, *IEEE Trans Industr Appl*, 60 (1) (2024) 7048.
- 19 Li Y, Wang Y & Li B Q, *IEEE J Emerg Sel Top Power Electr*, 4 (2) (2016) 589.
- 20 Lee E-J, Kim S-M & Lee K-B, *IEEE Access*, 8 (2020) 78130.
- 21 Bushra E, Zeb K, Ahmad I & Khalid M, *Result Eng*, 22 (2024) 102213.
- 22 Kim S-M, Lee E-J, Lee J-S, Lee K-B, *IEEE Access*, 8 (2020) 187072.
- 23 Belchior F N, De Lima L R, Ribeiro P F & Castro J F C, *IEEE Power Energy Soc Gen Meet*, (2015) pp. 1-5.
- 24 Adak S, *J Electr Eng Technol*, 16 (5) (2021) 2389.
- 25 Poongothai C & Vasudevan K, *IEEE Trans Industr Appl*, 55 (1) (2019) 584.
- 26 Zhao T, Wang G, Bhattacharya S & Huang A Q, *IEEE Trans Power Electr*, 28 (4) (2013) 1523.
- 27 Bahmani M A, Thiringer T & Kharezy M, *IEEE Trans Industr Appl*, 52 (5) (2016) 4225.
- 28 Shogenov A K, *Russ Electr Eng*, 90 (2) (2019) 162.
- 29 Chandran D R, Kumar S & Sanath D, *J Power Energy Eng*, 13 (06) (2025) 30.
- 30 Abhishek, Gupta R & Sahay K, *International Conference in Advances in Power, Signal, and Information Technology (APSIT)*, (2023) pp. 242-246.
- 31 Dissawa L, Perera N, Bandara K, Binduhewa P & Ekanayake J, *AIMS Energy*, 4 (2) (2016) 397.
- 32 Fouda S, Salem M S, Saeed A, Shaker A, Abouelatta M & El-Ela M A, *Alexandria Eng J*, 96 (2024) 156.
- 33 Laib A, Krama A, Sahli A, Kihal A & Abu-Rub H, *IEEE Access*, 10 (2022) 102210.
- 34 Xiao M, Xu Q & Ouyang H, *Energies*, 10 (9) (2017) 1327.