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Design and Analysis of Three-Stage and Five-Stage Digitally Controlled Oscillators with Low-Power Consumption

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This paper presents a design and performance analysis of 3-stage and 5-stage Digitally Controlled Oscillators (DCOs), incorporating NAND gate-based inverter and transmission gate-based pseudo-inverter delay stages. The circuits are designed using 90 nm CMOS technology and simulated with the Cadence Virtuoso tool at a supply voltage (V_{DD}) of 0.7 V. To enhance frequency tuning and minimize power consumption, the proposed architectures utilize a PMOS switching network in conjunction with MOS varactors. When the PMOS switching network control bits are varied from 000 to 110, the 3-stage DCO exhibits a power consumption range from 314.5mW to 323.4mW and a corresponding frequency variation between 4.829 GHz to 3.552 GHz. Under similar conditions, the 5-stage DCO demonstrates power consumption between 314.2 mW to 323.6 mW, with frequency 2.887 GHz to 1.645 GHz. Furthermore, when configured using MOS varactor control bits ranging from 000 to 110, the 3-stage DCO exhibits a power consumption of 314.5 mW and frequencies from 4.829 GHz to 4.458 GHz, while the 5-stage DCO operates at 314.2 mW in power with frequencies ranging from 2.887 GHz to 2.623 GHz. This work also presents the variation in power consumption and oscillation frequency as the supply voltage is swept from 0.4 V to 0.9 V.

Keywords: CMOS, Delay stage, DCO, NAND gate, NMOS, PMOS, Pseudo-inverter, Transmission gate

1 Introduction

An oscillator is a core electronic circuit that produces continuous and periodic alternating current (AC) waveforms across a wide frequency spectrum, typically ranging from a few hertz (Hz) to several gigahertz (GHz)[1-2] Oscillators can be generally categorized into two types: analog-controlled and digitally controlled oscillators. However, Digitally Controlled Oscillators (DCOs) have many advantages over conventional analog-controlled Voltage-Controlled Oscillators (VCOs), including improved frequency stability, programmability, and integration capability with modern CMOS technologies. As a result, the adoption of DCOs has been progressively increasing in CMOS-based electronic circuit designs[3-5].

A digitally Controlled Oscillator is a specialized oscillator that uses digital control signals to modulate and stabilize its output frequency[6]. In response to the growing demand for high-performance and energy-efficient electronic systems, the adoption of DCOs has become increasingly predominant in digital circuit environments. Their implementation in CMOS-based designs offers significant advantages, including reduced power consumption, enhanced noise immunity, and highly stable and linear frequency tuning characteristics[7]. In contemporary electronic systems, digitally Controlled Oscillators have emerged as a critical component, particularly in applications requiring precise frequency tuning, such as clock generation, wireless communication, and digital phase-locked loops (DPLLs)[7]. In the context of contemporary wireless communication technologies, All-Digital Phase-Locked Loops (ADPLLs) have found widespread application due to their improved noise performance and low power consumption. In the architecture of All-Digital Phase-Locked Loops (ADPLLs), the digitally Controlled Oscillator serves as a critical component, as the overall performance of the ADPLL is strongly influenced by the characteristics of the DCO—particularly its power consumption and phase noise behaviour[8-10].

The evaluation of a DCO is typically based on key performance metrics such as power consumption, supply voltage, frequency tuning range, operational speed, chip area, and resolution. In System-on-Chip (SoC) design, minimizing the power consumption of the Digitally Controlled Oscillator is critical to fulfilling low-power design requirements, thereby

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contributing to the overall reduction in power dissipation of the integrated system[10-15]. Digitally Controlled Oscillators offer several advantages over Voltage-Controlled Oscillators, like lower power consumption and improved frequency tuning capabilities, etc. Due to the nonlinear characteristics of frequency and control voltage in VCOs, they are more susceptible to noise as compared to DCOs, which compromises the performance and reliability of the circuit[16-20]. Therefore, DCOs are increasingly replacing VCOs in modern circuit designs[10-15]. Furthermore, the implementation of VCOs in deep submicron CMOS technologies poses significant challenges, making DCOs a more favourable alternative for integration in advanced CMOS-based electronic systems. DCOs are extremely appropriate for implementation in CMOS technology because their digital control mechanism aligns well with CMOS scaling, allowing low-power operation, compact area utilization, and enhanced frequency resolution[21-25]. Therefore, the need for high frequency resolution and low power consumption is likely to remain an important and active research area in the coming years[26-30]. This study introduces novel designs of DCO circuits and provides a comprehensive performance analysis, including a comparative evaluation against existing architectures with similar design frameworks.

2 Methods and Materials

2.1 Architecture of DCO Using Delay Stages

It investigates 3-stage and 5-stage DCO configurations employing alternating delay stages. Each DCO design comprises two types of delay elements: a NAND gate-based inverter delay stage (Fig. 1) and a transmission gate-based pseudo-inverter delay stage (Fig. 2).

The NAND gate-based inverter as shown in Fig. 1. uses the essential properties of a NAND logic gate to function as an inverting circuit. In this circuit configuration, the input signal (Vin) is applied to both inputs of the NAND gate, thereby making the logic gate to perform as an inverter.

The circuit comprises of complementary PMOS and NMOS transistors arranged in a pull-up and pull-down network, respectively. The pull-up network consists of PMOS transistors P1–P3, P11, P12, and the binary-weighted PMOS switches P4–P6, all connected to V_{DD}. The pull-down network is implemented using NMOS transistor N11. Digital control bits (D2, D1, D0) drive the PMOS switches to

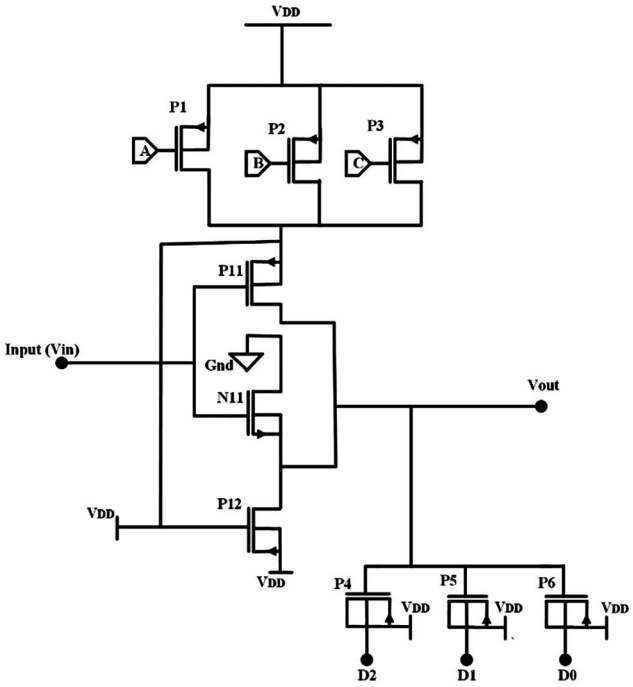

Fig. 1 — NAND gate-based Inverter delay stage

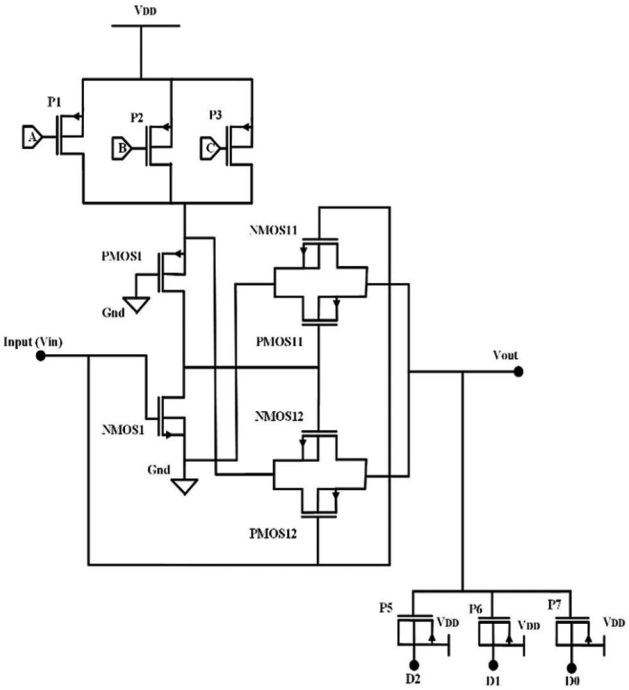

Fig. 2 — Transmission gate-based Pseudo-Inverter delay stage

permit coarse frequency tuning by modifying the pull-up network's effective loading.

When the input signal (Vin) is at logic high, both inputs of the NAND gate are high, which drives the pull-down NMOS network into conduction and turns

off the pull-up PMOS devices. As a result, the output node (Vout) is discharged to logic low. Conversely, when the input signal (Vin) is at logic low, the PMOS transistors conduct while the NMOS devices remain off, thereby charging the output node (Vout) to logic high. The NAND gate-based inverter achieves full voltage swing at the output, offering better noise immunity, high reliability, and compatibility with standard CMOS logic families.

The transmission gate-based pseudo inverter as shown in Fig. 2. functions by combining a transmission gate structure with a conventional inverter configuration to attain enhanced switching characteristics. In this design, the input signal (Vin) is applied to the transmission gate, which consists of complementary NMOS and PMOS transistors controlled by the same input and its complement. This arrangement confirms effective signal transmission with minimal voltage degradation across the entire voltage range.

When the input (Vin) is logic high, the NMOS transistor in the transmission gate conducts strongly, while the PMOS provides additional conduction, thereby reducing resistance and confirming a sharp transition at the output. Conversely, when (Vin**)** is logic low, the PMOS transistor conducts efficiently while the NMOS confirms full discharge capability, yielding improved noise margins compared to conventional pseudo-inverters. The pseudo-inverter structure improves performance by lowering propagation delay and improving driving capability. Additionally, the use of both NMOS and PMOS devices in the transmission gate minimizes threshold voltage drop issues, thereby achieving full voltage swing at the output (Vout). This makes the transmission gate-based pseudo inverter particularly suitable for low-power, high-performance applications in digital circuit design.

The functionality of the entire circuit is based on the feedback mechanism, wherein the output of the final stage is looped back to the input of the first stage. This closed-loop configuration establishes ring topology, which is a fundamental structure used in the design of DCOs. The work of this paper presents a comprehensive comparative analysis of 3-stage and 5-stage DCOs, employing both NAND gate-based inverter and transmission gate-based pseudo-inverter architectures as delay elements. The 3-stage and 5-stage DCO circuits are analysed using a PMOS switching network in conjunction with MOS varactors to achieve output frequency tuning. Both the switching network and MOS varactor are integrated within each delay stage to facilitate precise frequency regulation. In the proposed DCO architecture, the input signals A, B, and C of the switching elements drive the PMOS transistors P1, P2, and P3, correspondingly. Their primary function is to shaping the propagation delay of the cell by regulating the pull-up operation during the transition of the input signal. When inputs A, B, or C transition to a low state, the corresponding PMOS device (P1, P2, or P3) turns ON and contributes to charging the output node. This maintains logic level integrity, proper signal restoration, and stabilizes the overall oscillation waveform. Similarly, the input signals D0, D1, and D2 serve as digital tuning inputs to the MOS varactor binary-weighted PMOS transistors P4, P5, and P6**.** These digital control bits regulate whether each PMOS switch is activated, effectively enabling or disabling specific branches of the PMOS switching network. When a tuning bit is high, the connected PMOS transistor conducts and introduces an additional capacitive and resistive load at the output node.

In a ring-type digitally Controlled Oscillator, the oscillation frequency is determined by the cumulative propagation delay introduced by each delay stage and the total number of stages used in the configuration. The oscillation frequency (F) of the ring DCO can be mathematically represented as shown in Eq. (1)

$$F = \frac{1}{2N\tau_d} \quad \ldots (1)$$

'F' denotes the output frequency of the DCO, 'N' denotes the total number of delay stages utilized in the DCO architecture, and τ_d refers to the propagation delay associated with each individual delay stage.

Figure 3 illustrates the block diagrams of 3-stage and 5-stage DCOs using NAND gate-based inverter

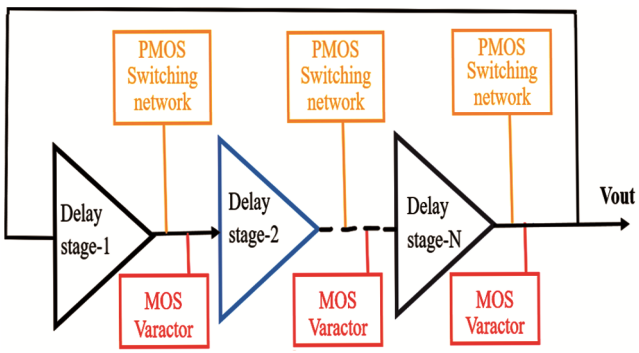

Fig. 3 — Block diagram of 3-stage and 5-stage DCO

and Transmission gate-based pseudo-inverter as delay stages. The 3-stage DCO consists of three stages, arranged sequentially as NAND gate-based inverter, a Transmission gate-based pseudo-inverter, and another NAND gate-based inverter, as shown in Fig. 4. Similarly, the 5-stage DCO includes five delay stages in the following order: NAND gate-based inverter, transmission gate-based pseudo-inverter, NAND gate-based inverter, Transmission gate-based pseudo-inverter, and a final NAND gate-based inverter, as shown in Fig. 5.

In the proposed DCO architecture, frequency tuning is achieved through a combination of coarse tuning and fine-tuning mechanisms. Coarse tuning is implemented using binary-weighted PMOS switching elements in the form of (2^0, 2^1, 2^2, …), which offers large and discrete frequency steps with wide tuning range. In contrast, fine tuning is realized using MOS varactors, whose capacitance changes smoothly with the control bits variation which offers high frequency resolution. The combination of both tuning mechanism permits the proposed DCO architecture to simultaneously attain a

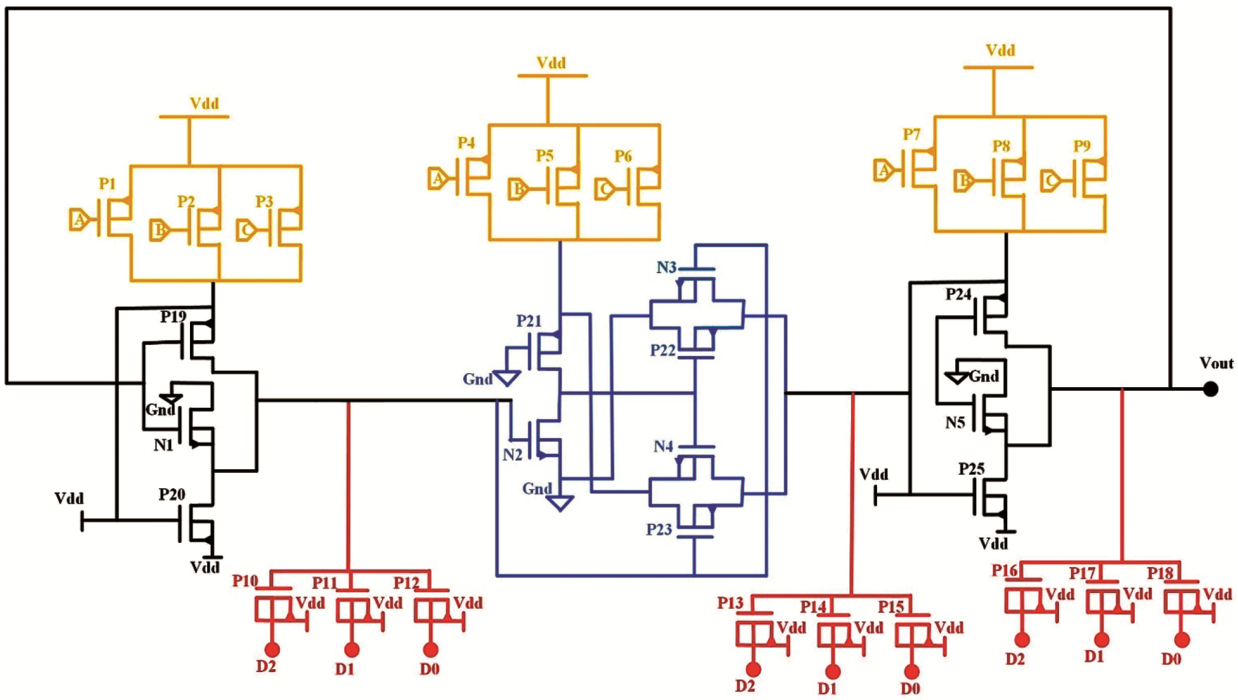

Fig. 4 — 3-stage DCO using Delay stages

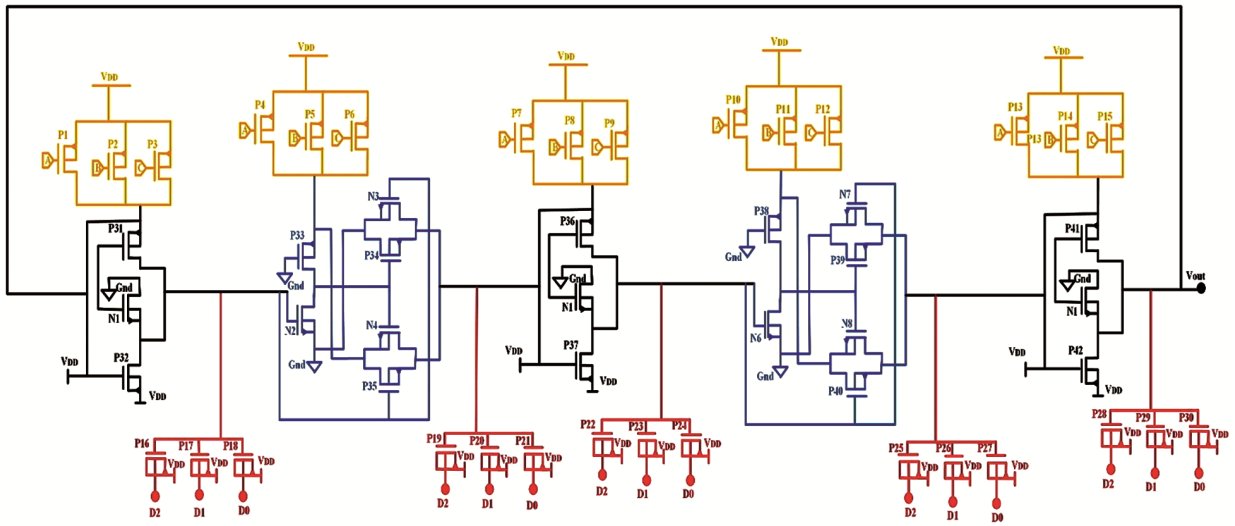

Fig. 5 — 5-stage DCO using Delay stages

wide tuning range and high frequency resolution, which makes the design appropriate for high-frequency and low power VLSI applications.

Table 1 presents the width and length ratio of the transistors employed within the delay stages of the digitally controlled oscillator.

In the MOS varactor structure, the source and drain terminals are shorted together to form a single node, which is connected to V_{DD}, while the bulk terminal is connected to digital control bits. By varying these control bits, regulation of the output frequency is achieved. The gate terminal serves as the second node forming a capacitive structure with the source/drain node. This configuration functions as a variable capacitor, where the capacitance exhibits a non-monotonic dependency on the applied gate voltage.

The 3-stage DCO is shown in Fig. 4. works on the principle of delay propagation through cascaded inverter-based delay cells, with its oscillation frequency digitally tuned by control bits. Each stage of the DCO comprises delay elements that integrate transmission gate-based pseudo-inverters, or NAND gate-based inverters, which give the controllable delay essential for frequency modulation. The input signal is serially passed through the three delay stages, where each stage introduces a propagation delay produced by the effective load capacitance and transistor sizing. The output of the third stage is fed back to the input of the first stage, making a closed-loop ring oscillator structure. This feedback loop confirms continuous oscillation as long as the circuit is powered. Digital control bits (D0, D1, D2) dynamically regulate the load capacitance and switching activity within each delay cell by enabling or disabling MOS transistors connected at the output nodes. By adjusting these control signals, the total delay per stage can be varied, leading to specific tuning of the oscillation frequency. A higher effective capacitance increases delay and reduces frequency, whereas a lower capacitance decreases delay and raises the frequency. Thus, the 3-stage DCO generates a periodic oscillation whose frequency is digitally programmable, making it highly suitable for low-power frequency synthesizers, clock generation, and timing circuits in modern CMOS technology.

Table 1 — Width and Length ratio of DCO Delay stages

Delay stages	MOSFET	Width (nm)	Length (nm)	W/L ratio
NAND gate-based inverter	P11	550	100	5.5
	N11	275	100	2.75
	P12	500	100	5.0
Transmission gate-based Pseudo-inverter	PMOS1	550	100	5.5
	NMOS1	275	100	2.75
	PMOS11	550	100	5.5
	NMOS11	275	100	2.75
	PMOS12	550	100	5.5
	NMOS12	275	100	2.75
PMOS switching network	P1	120	100	1.2
	P2	240	100	2.4
	P3	480	100	4.8
MOS Varactor	P5	120	100	1.2
	P6	240	100	2.4
	P7	480	100	4.8

The 5-stage DCO shown in Fig. 5 is based on a ring oscillator topology, in which five delay stages are connected sequentially to form a closed-loop feedback system. Each delay stage is composed of as defined in 3-stage DCO a NAND-gate-based inverter, pseudo-NMOS logic, and digitally controlled capacitive loading elements. The oscillation frequency is determined by the cumulative delay introduced by these stages. The digitally controlled capacitors (D0, D1, and D2), implemented using MOS varactors, are connected at each stage to adjust the effective load capacitance. By varying the digital control bits, the capacitance at each node is altered, thereby modifying the propagation delay. This change directly impacts the oscillation frequency, enabling fine-tuned frequency control. In operation, the first delay stage receives the input signal, which propagates sequentially through the remaining four stages. The output is extracted from the final stage, yielding a frequency that is digitally programmable through the control bits. This architecture provides a wider tuning range, improved power efficiency, and reduced phase noise compared to conventional inverter-based ring oscillators.

Both architectures utilize a single-ended ring oscillator topology, which imposes delay stages of odd numbers to sustain fluctuations in the output of the oscillator. This topology is widely favoured in integrated circuit design due to its low power consumption and efficient utilization of silicon area.

3 Results and Discussion

The reported work presents a comprehensive simulation-based analysis of power consumption and frequency characteristics for 3-stage and 5-stage DCOs, designed using NAND gate-based inverter

and transmission gate-based pseudo-inverter delay stages. The simulation is done in 90 nm technology using the Cadence Virtuoso tool. A comparative analysis of power consumption and oscillation frequency for both configurations is provided, with results visually represented through graphical plots. The output waveform of the 3-stage and 5-stage DCO corresponding to the 000 control bits of the switching network is shown in Figs. 6-7, respectively.

Table 2 illustrates the variations in power consumption and oscillation frequency for both the 3-stage and 5-stage DCOs under different operating conditions, as the control bits of the PMOS switching network are varied from 000 to 110. For the 3-stage DCO, consumption of power ranges from 314.5 mW to 323.4 mW, while the corresponding frequency decreases from 4.829 GHz to 3.552 GHz. Similarly,

Table 2 — Results of 3-stage and 5-stage DCOs for various control bits of switching network

Control bits A B C	3-stage DCO		5-stage DCO	
	Power (mW)	Frequency (GHz)	Power (mW)	Frequency (GHz)
0 0 0	314.5	4.829	314.2	2.887
0 0 1	315.0	4.705	314.8	2.536
0 1 0	315.7	4.653	315.5	2.448
1 0 0	317.8	4.554	317.8	2.137
1 0 1	319.7	4.449	319.8	1.850
1 1 0	323.4	3.552	323.6	1.645

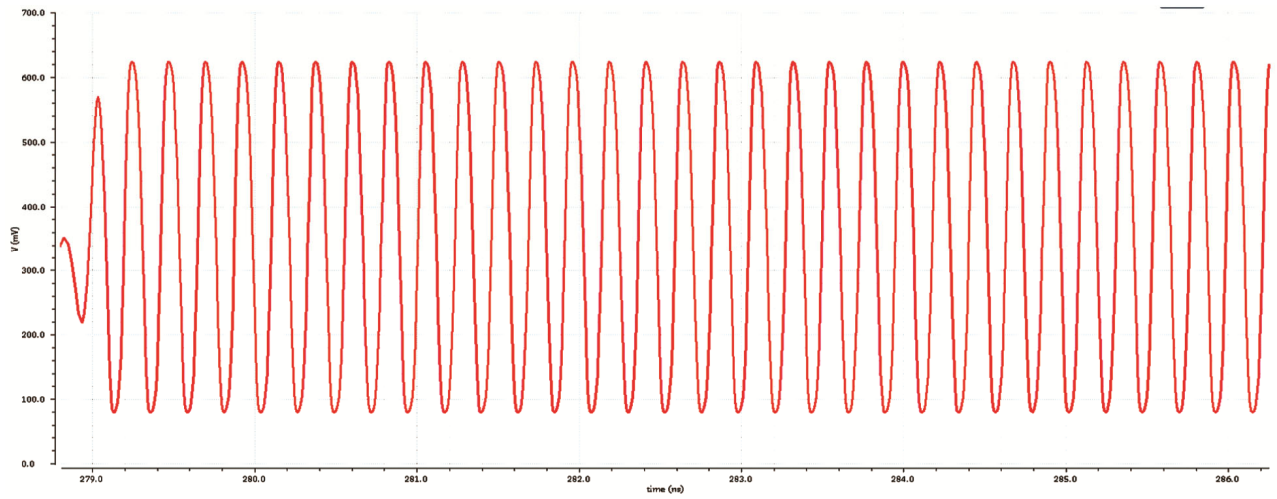

Fig. 6 — Output of 3-stage DCO at 000 Control bits

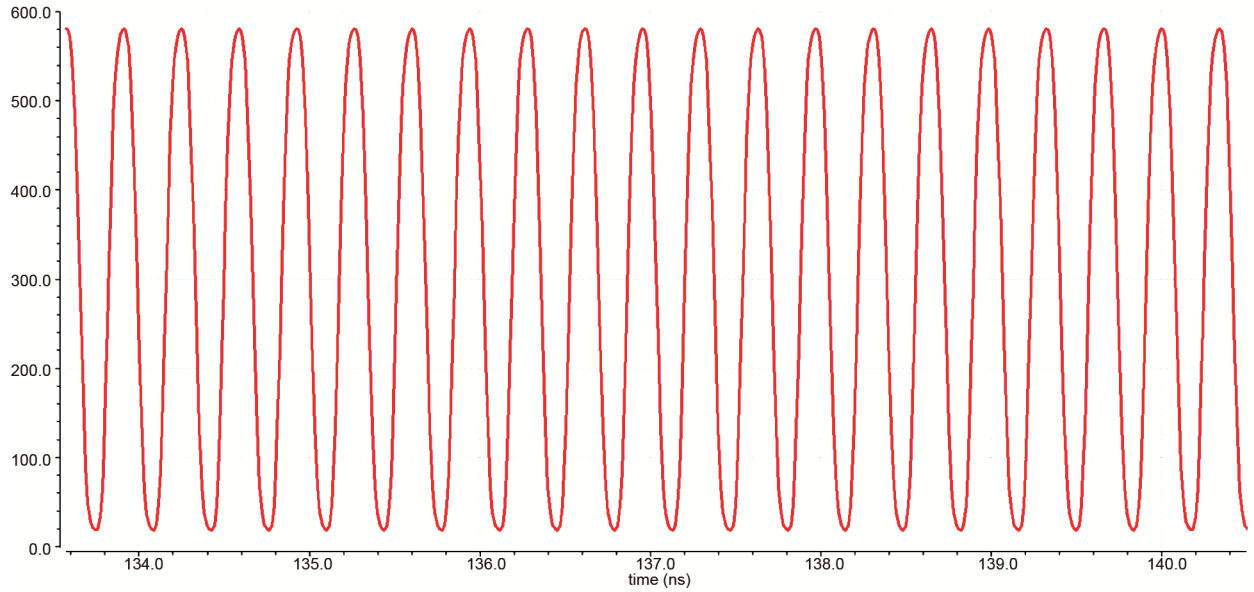

Fig. 7 — Output of 5-stage DCO at 000 Control bits

the 5-stage DCO exhibits power consumption ranging from 314.2 mW to 323.6 mW, with the frequency varying from 2.887 GHz to 1.645 GHz. These variations in performance parameters for both DCO configurations are graphically illustrated in Fig. 8.

Table 3 presents the variations in consumption of power and oscillation frequency for both the 3-stage and 5-stage the power consumption and oscillation frequency variations of the 3-stage and 5-stage DCOs as the voltage varies from 0.4 V to 0.9 V.

For the 3-stage DCO, power consumption ranges from 161.3 mW to 414.1 mW, while the corresponding frequency increases from 0.432 GHz to 4.653 GHz. Similarly, the 5-stage DCO shows power consumption ranging from 160.3 mW to 414.2 mW, with the frequency varying from 0.425 GHz to 5.237 GHz.

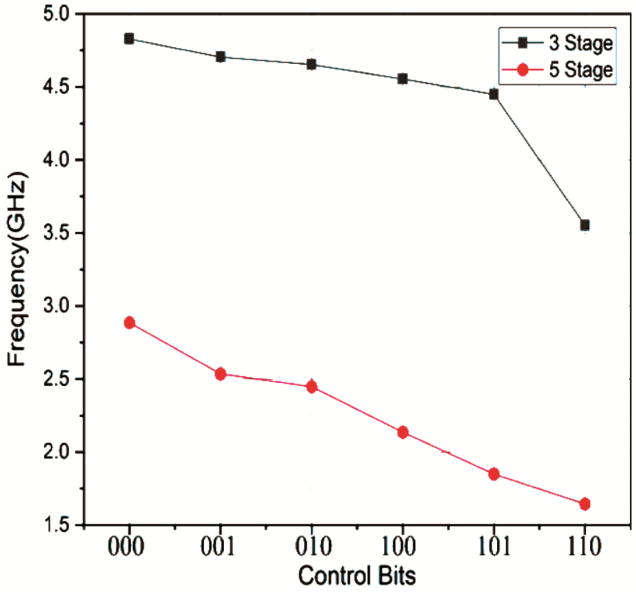

Fig. 8 — Frequency v/s control bits of 3-stage and 5-stage DCO

Table 3 — Results of 3-stage and 5-stage DCOs at various supply voltages

Voltage(V)	3-stage DCO		5-stage DCO	
	Power (mW)	Frequency (GHz)	Power (mW)	Frequency (GHz)
0.4	161.3	0.432	160.3	0.425
0.5	214.3	1.495	213.6	1.045
0.6	265.7	3.022	265.3	1.661
0.7	315.7	4.653	315.5	2.448
0.8	364.7	0.632	364.6	4.457
0.9	414.1	0.633	414.2	5.237

Table 4 presents the consumption of power and oscillation frequency variations of the 3-stage and 5-stage DCOs as the MOS Varactor bits vary from 000 to 110. For the 3-stage DCO, the power consumption is 314.5 mW, while the corresponding frequency increases from 4.829 GHz to 4.458 GHz. Similarly, the 5-stage DCO shows power consumption of 314.2 mW, with the frequency varying from 2.887 GHz to 2.623 GHz. These variations in performance parameters for both DCO configurations are graphically illustrated in Fig. 9.

The layouts of the proposed design circuit of three-stage and five-stage DCO circuits are shown in Figs. 10-11. The three-stage DCO occupies a chip area of 15.45 × 19.045 μm², whereas the five-stage DCO requires a larger area of 27.8 × 20.33 μm².

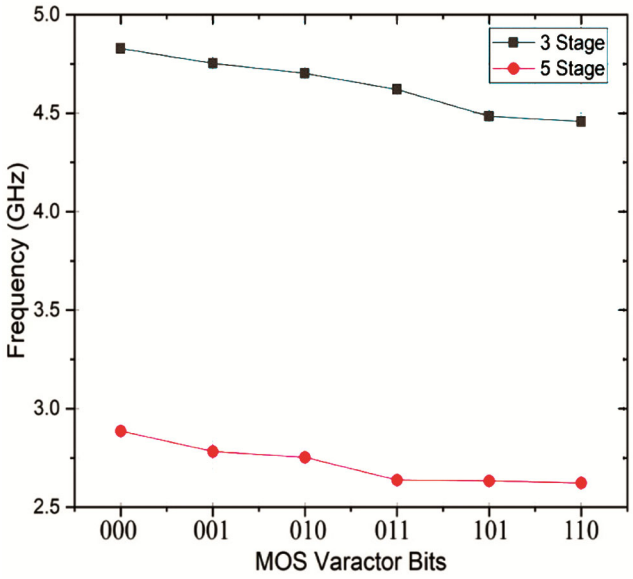

Fig. 9 — Frequency v/s MOS Varactor bits of 3-stage and 5-stage DCO

Table 4 — Results of 3-stage and 5-stage DCOs for various MOS varactor bits

MOS Varactor bits			3-stage DCO		5-stage DCO	
D0	D1	D2	Power (mW)	Frequency (GHz)	Power (mW)	Frequency (GHz)
0	0	0	314.5	4.829	314.2	2.887
0	0	1	314.5	4.754	314.2	2.783
0	1	0	314.5	4.703	314.2	2.753
0	1	1	314.5	4.621	314.2	2.638
1	0	1	314.5	4.485	314.2	2.634
1	1	0	314.5	4.458	314.2	2.623

The proposed DCO exhibits improved performance characteristics, including lower power consumption and enhanced frequency tuning capability. Table 5 provides a comprehensive comparison between the proposed work and various DCO designs architecture reported in the literature, clearly demonstrate the performance enhancements given by the present design. There are certain limitations associated with the proposed DCO architecture. The number of transistors employed in the design is relatively high, which increases overall circuit complexity. Additionally, although MOS varactors and binary-

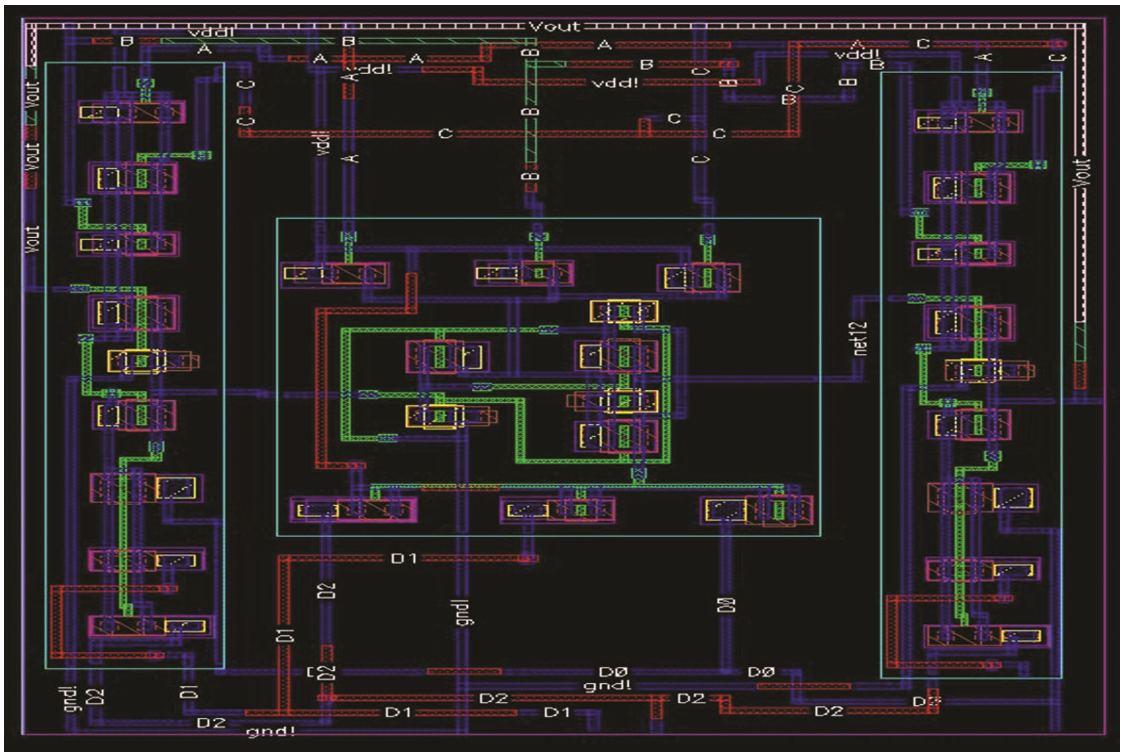

Fig. 10 — Layout of 3-stage DCO

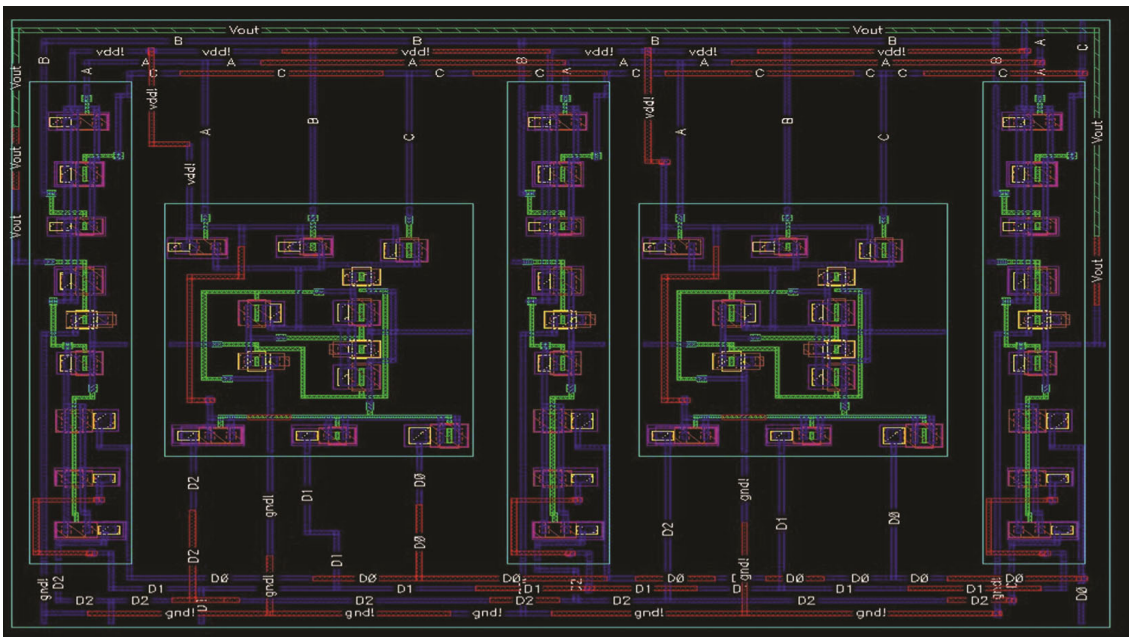

Fig. 11 — Layout of 5-stage DCO

Table 5 — Comparison table of various literate review and Proposed work

Ref.	DCO Architecture	Technology	Oscillation frequency	Reported power	Key features
[26]	Ring DCO with Capacitive Tuning	180nm	0.9–1.6 GHz	520 mW	Very high power; large-area design
[27]	LC-DCO	130nm	1.5–3.4 GHz	410 mW	High power but good phase noise
[28]	Switched-Capacitor DCO	90nm	2.0–4.5 GHz	360 mW	High power consumption
[29]	Digital Ring DCO	65nm	1.3–2.2 GHz	345 mW	Moderate tuning range but very high power
[30]	Active-Inductor DCO	65nm	3.2–6.5 GHz	6.1 mW	Higher noise
Proposed 3-Stage DCO	NAND-based + PMOS Weighted Switching + Varactor Tuning	90nm	4.8 4.829 -3.552 GHz	3 314.5-323.4mW	Wide tuning and high resolution
Proposed 5-Stage DCO	Transmission gate based Pseudo-Inverter + PMOS Weighted Switching + Varactor Tuning	90nm	2.887 - 1.645 GHz	314.2-323.6mW	Wide range and stable oscillation

weighted PMOS transistors significantly improve frequency resolution, they also lead to a larger circuit area and may introduce non-linearities during circuit operation and analysis.

4 Conclusion

This paper presents a detailed investigation of new 3-stage and 5-stage digitally Controlled Oscillator circuit architectures, realized using 90 nm CMOS technology and evaluated through simulations conducted in the Cadence Virtuoso tool at a supply voltage of 0.7 V. The designed circuitry incorporates delay stages based on a NAND gate-based inverter and a transmission gate-based pseudo-inverter, utilizing a PMOS switching network and MOS varactors. The DCO circuit designs are aimed at achieving enhanced performance, particularly in terms of reduced power consumption and improved frequency tuning efficiency. The 3-stage DCO exhibits a variation in power consumption ranging from 314.5 mW to 323.4 mW, with a corresponding frequency range of 4.829 GHz to 3.552 GHz, as the control bits of the PMOS switching network are varied from 000 to 110.

Similarly, the 5-stage DCO demonstrates power consumption values between 314.2 mW and 323.6 mW, with an associated frequency range from 2.887 GHz to 1.645 GHz over the same control bit variation. Furthermore, under varying supply voltages from 0.4 V to 0.9 V, the 3-stage DCO shows power consumption between 161.3 mW and 414.1 mW, and frequency ranging from 0.432 GHz to 4.653 GHz. In parallel, the 5-stage DCO exhibits power consumption values between 160.3 mW and 414.2 mW, with frequency varying from 0.425 GHz to 5.237 GHz over the same voltage range. When controlled via MOS varactor bits from 000 to 110, the 3-stage DCO's power consumption is 314.5 mW with frequencies of 4.829 GHz to 4.458 GHz, while the 5-stage DCO shows 314.2 mW in power and 2.887 GHz to 2.623 GHz in frequency. Supply variations between 0.4 V and 0.9 V further yielded power ranges of 161.3 mW to 414.1 mW (3-stage) and 160.3 mW to 414.2 mW (5-stage), with corresponding frequency spans of 0.432 GHz–4.653 GHz and 0.425 GHz–5.237 GHz, respectively. These digitally Controlled Oscillator architectures demonstrate superior frequency tuning capabilities while maintaining low power consumption, thereby making them well-suited for high-frequency integrated circuit applications.

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