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Fractional Order Mem-Inductor and Mem-Capacitor Mutator using Single DXCCTA

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The paper introduces new designs for fractional-order mem-element mutators utilizing an active component known as the dual-X current conveyor transconductance amplifier (DXCCTA). These mutators serve as both meminductor and memcapacitor emulators. The proposed designs incorporate just one DXCCTA, one memristor and one fractional-order capacitor which is implemented using a constant phase element. The mem-element mutators can operate in both floating and grounded modes. An extensive analysis of the circuits is presented, addressing ideal, and non-ideal analysis. The theoretical performance of the designed mem-element mutator circuits is validated through SPICE simulations using 0.18 µm technology. The proposed mutator designs demonstrate a high operating frequency (up to 800 kHz), low power consumption (2.5 mW), low operating supply voltages (±1.25 V) and robust performance across variations in process, voltage, and temperature. The non-volatility of the proposed emulators is also tested.

Keywords: Analog circuit, DXCCTA, Grounded/ floating structure, Meminductor emulator, Memcapacitor emulator

1 Introduction

The mem-elements emulators are getting popular nowadays due to their interesting properties and broader application areas. The increasing need for advanced electronic circuits has led to substantial research focused on the design and emulation of mem-elements, such as meminductors, memcapacitors, and memristors. The memristors are introduced very early. Like memristors, meminductors and memcapacitors are also utilized to store energy in inductive and capacitive forms. Recently, researchers have also explored fractional-order mem-elements, which extend the conventional integer-order models by incorporating fractional calculus. These elements provide enhanced flexibility in modeling complex dynamical behaviors, making them highly suitable for applications requiring precise tuning of memory effects. Fractional-order memristors, memcapacitors, and meminductors have demonstrated improved performance in neuromorphic computing, chaotic systems, and bio-inspired circuits, further broadening the scope of mem-element-based technologies.

The short survey outlines the key elements of numerous mem-element emulator designs from the recent works. These reported designs to emulate meminductors and memcapacitors utilize different active building blocks (ABBs) and passive components, such as capacitors, resistors, and fractional-order capacitors. The reported structure of individual design whether floating or grounded is also noted, together with the use of multipliers and the order of the elements (fractional or integer). The circuit reported[1-2] utilizes the combination of ABBs. The design[1] uses one voltage differencing inverted buffered amplifier (VDIBA), one operational transconductance amplifier (OTA) along with two capacitors and two MOS transistors. It operates in a floating configuration to emulate an integer-order meminductor. The configuration reported[2] employs one modified voltage differential current conveyor (MVDCC), one OTA, one resistor, and two capacitors. It is designed to emulate an integer-order meminductor in a floating structure. The work[3] employs four OTAs and two capacitors. This design emulates an integer-order meminductor in a grounded structure. Another variant with three OTAs and one second-generation current conveyor (CCII) is used to emulate an integer-order memcapacitor in a grounded structure. The design presented[4] incorporates two voltage differencing current conveyors (VDCCs) and two MOS transistors, with two capacitors. It is capable of emulating both a meminductor and a memcapacitor of integer-order in a floating structure. A single VDCC, one OTA, one resistor, and two

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capacitors are used in the circuit[5] to emulate an integer-order memcapacitor in a grounded configuration. This design[6] utilizes two voltage differential transconductance amplifiers (VDTAs) and two capacitors to emulate an integer-order meminductor in a floating structure.[7], two CCIIs and one OTA, along with two resistors and two capacitors, are employed to create a grounded emulator for both an integer-order meminductor and memcapacitor. The configuration[8] features two OTAs and one current differencing buffered amplifier (CDBA) with one capacitor and one fractional-order capacitor. It is used to emulate a fractional-order meminductor in a floating structure. In the design of[9], two CCIIs and one memristor are used with one resistor and one fractional-order capacitor to emulate both a meminductor and a memcapacitor of fractional order in a grounded structure. A similar configuration with three CCIIs and one memristor, using two resistors and one fractional-order capacitor, is also used for the same purpose[9]. The work reported[10] features one CBTA and one memristor with one capacitor in a floating setup. It supports both a meminductor and a memcapacitor configuration and it is suitable for integer-order applications. One OTA, one memristor are integrated with one resistor and one capacitor to form a grounded configuration[11]. It provides an integer-order memcapacitor element. The structure[12] employs three AD844 ICs, one memristor with three resistors and one capacitor in a grounded structure, supporting both a meminductor and a memcapacitor elements of integer-order type. The emulator[13] uses four AD844 ICs, one TL084 IC, and one voltage divider (VD) with six resistors and two capacitors to provide a floating structure of meminductor and memcapacitor elements of integer-order type. A voltage differencing differential input buffered amplifier (VD-DIBA) based design of meminductor and memcapacitor emulator using one VD-DIBA, two capacitors and external MOS transistors is reported[14]. A meminductor emulator of integer order type using one OTA, one CCII, one CDBA, one resistor and two capacitors is presented[15]. The structure[16] implements a grounded configuration, supporting both a meminductor and a memcapacitor emulators of fractional order type. It consists of three CCIIs, three amplifiers with three resistors and two fractional capacitors. The mem-element emulator[17] incorporates one VDIBA, one current follower (CF), one capacitor and one fractional capacitor in a grounded setup, supporting a meminductor emulator of fractional-order type. The circuit[18] utilizes three CCIIs, three resistors, one capacitor, and one fractional capacitor in a grounded configuration. It supports both a meminductor and a memcapacitor emulators of fractional-order type. The circuit design[19] features two configurations: the first one uses one CCII, one resistor, one capacitor, and one fractional capacitor in a grounded setup, and the other one exploits one OTA and one CCII using the same passive components but in a floating structure. Both structures support a fractional-order memcapacitor emulator.

In this paper, novel mutator designs are proposed that utilize one dual-X current conveyor transconductance amplifier (DXCCTA), one memristor and one fractional-order capacitor. The proposed designs feature a minimal configuration. This approach enables the emulation of both a memcapacitor and a meminductor, offering flexibility for various practical applications. In addition, the emulators can operate in both floating and grounded configurations, further expanding their usability in different circuit environments. The paper offers in-depth analysis, considering the influence of ideal, and non-ideal aspects on the emulator's performance. To validate the theoretical results, SPICE simulations are conducted using 180 nm technology, confirming that the proposed emulators exhibit high frequency response, low power consumption, and reliable performance across variations in process, voltage, and temperature (PVT). By introducing novel and efficient designs for fractional-order mem-element emulation, this research focuses to enrich the abilities of mem-element circuits and deliver practical solutions for applications in emerging technologies. The detailed comparison given in Table 1 showcases the novel aspects of the proposed emulators, which stand out due to their minimal component configuration, along with their ability to emulate fractional-order elements in both floating and grounded modes.

2 Fractional Order Mem-Elements

Mem-Elements refer to components in electrical circuits that have memory. Memristors, memcapacitors and meminductors are memory elements where the current or voltage depends not just on the present state, but also on past states. When fractional orders are introduced, they become fractional memristors,

Table 1 — Comparison of the proposed mem-element emulators with other relevant works

Ref.	ABB Used	Passive Components Used	Use of Multiplier	Grounded/ Floating Structure	Mem-ductance type (M_L/M_C)	Simultaneous availability of incremental and decremental M_C	Integer/Fractional Order
[1]	1 VDIBA, 1 OTA, 2 MOS	2C	No	Fl	M_L	NA	I
[2]	1 MVDCC, 1 OTA	1R, 2C	No	Fl	M_L	NA	I
[3]	4 OTA	2C	No	Gr	M_L	NA	I
	3 OTA, 1 CCII	1R, 2C	No	Gr	M_C	No	I
[4]	2 VDCC, 2 MOS	2C	No	Fl	M_L, M_C	No	I
[5]	1 VDCC, 1 OTA	1R, 2C	No	Gr	M_C	No	I
[6]	2 VDTA	2C	No	Fl	M_L	No	I
[7]	2 CCII, 1 OTA	2R, 2C	No	Gr	M_L	NA	I
	2 CCII, 1 OTA	2R, 2C	No	Gr	M_C	No	I
[8]	2 OTA, 1 CDBA	1C, 1FC	No	Fl	M_L	NA	F
[9]	2 CCII, 1 Memristor	1R, 1FC	Yes	Gr	M_L, M_C	No	F
	3 CCII, 1 Memristor	2R, 1FC	Yes	Gr	M_L, M_C	No	F
[10]	1 CBTA, 1 Memristor	1C	Yes	Fl	M_L, M_C	No	I
[11]	1 OTA, 1 Memristor	1R, 1C	Yes	Gr	M_C	No	I
[12]	3 AD844, 1 Memristor	3R, 1C	Yes	Gr	M_L, M_C	No	I
[13]	4 AD844, 1 TL084, 1 VD	6R, 2C	No	Fl	M_L, M_C	No	I
[14]	1 VD-DIBA	2C	No	Gr	M_L, M_C	No	I
[15]	1 OTA, 1 CCII-, 1CDBA	1R, 2C	No	Gr	M_L	NA	I
[16]	3 CCII, 3 Amplifiers	3R, 2FC	Yes	Gr	M_L, M_C	No	F
[17]	1 VDIBA, 1 CF	1C, 1FC	No	Gr	M_L	NA	F
[18]	3 CCII	3R, 1C, 1FC	Yes	Gr	M_L, M_C	No	F
[19] Fig. 8(a)	1 CCII	1R, 1C, 1FC	Yes	Gr	M_C	No	F
[19] Fig. 9(c)	1 OTA, 1 CCII	1R, 1C, 1FC	Yes	Fl	M_C	No	F
This Work	1 DXCCTA, 1 Memristor	1FC	No	Fl	M_L, M_C	Yes	F

Fl: Floating, Gr: Grounded, I: Integer, F: Fractional, M_L: Mem-inductance, M_C: Mem-capacitance

fractional memcapacitors, and fractional meminductors respectively. The expressions of memristance (M_R), mem-capacitance (M_C) and mem-inductance (M_L) of these memory elements are given below.

$$v(t) = M_R(t)i(t) \quad \text{... (1)}$$

$$v(t) = M_C(t)q(t) \quad \text{... (2)}$$

$$\varphi(t) = M_L(t)i(t) \quad \text{... (3)}$$

A direct relationship between $\varphi(t)$ and $q(t)$ is defined by a new element called 2nd order memristor as given below.

$$\Phi(t) = R_{2M}(t)q(t) \quad \text{... (4)}$$

A generalized model of fractional order mem-elements named as memfractor is given[20] which can represent all the above expressions by using a single equation as follows:

$$D_t^{\alpha_1}\varphi(t) = F_M^{\alpha_1,\alpha_2}(t)D_t^{\alpha_2}q(t) \quad \text{... (5)}$$

where D_t^{α} is the fractional operator, α_1, α_2 are the real number between 0 and 1, and $F_M^{\alpha_1,\alpha_2}$ is the memfractance. For $\alpha_1 = 1$ and $\alpha_2 = 1$, memfractor represents a conventional memristor, for $\alpha_1 = 1$ and $\alpha_2 = 0$, memfractor represents a conventional memcapacitor, for $\alpha_1 = 0$ and $\alpha_2 = 1$, memfractor represents a conventional meminductor and for $\alpha_1 = 0$ and $\alpha_2 = 0$, memfractor represents a conventional second order memristor. A fractional order meminductor is defined as follow.

$$D_t^{\alpha_1}\varphi(t) = F_M^{\alpha_1,1}(t)i(t) \quad \text{... (6)}$$

where $F_M^{\alpha_1,1}(t) = M_L^{\alpha_1}$ is mem-inductance. A fractional order memcapacitor is defined as follow.

$$v(t) = F_M^{1,\alpha_2}(t)D_t^{\alpha_2}q(t) \quad \text{... (7)}$$

where $F_M^{1,\alpha_2}(t) = M_C^{\alpha_2}$ is mem-capacitance.

3 Proposed Fractional order Mem-element Mutators

The proposed mem-element mutators are based on active element DXCCTA which is an active component known for its excellent performance in analog circuits, featuring a combination of OTA and dual-X second-generation current conveyor[21]. Several linear and non-linear applications based on DXCCTA are reported in the literature[21-27]. The circuit diagrams of the proposed mutators realizing fractional order meminductor emulator and memcapacitor emulator are depicted in Fig. 1. It is noted that only one DXCCTA, one memristor and one fractional capacitor are used in the circuit realization of each mutator. In the circuit of meminductor mutator, a floating memristor and a grounded fractional capacitor are used. The circuit of memcapacitor mutator uses a grounded memristor and a floating fractional capacitor. The mutator circuits shown in Fig. 1 implement floating structures of meminductor and memcapacitor. However, if either terminal Z_P or Z_N in Fig. 1(a) is grounded while an input is applied to the non-grounded terminal, a grounded structure of the meminductor can be realized. Similarly, a grounded structure of the memcapacitor can be realized, if either terminal X_P or X_N in Fig. 1(b) is grounded while an input is applied to the non-grounded terminal. The fractional capacitor used in this paper is realized using Valsa's approximation[28] as shown in Fig. 2. The terminal attributes of DXCCTA are defined as given below.

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m & g_m & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP} \\ V_{ZN} \\ V_O \end{bmatrix} \quad \ldots (8)$$

The transconductance (g_m) of the DXCCTA in (8) is expressed as provided below:

$$g_m = \sqrt{(KI_B)} \quad \ldots (9)$$

where, $K = \mu_n C_{OX}\left(\frac{W}{L}\right)$. It is observed from (9) that the transconductance (g_m) can be adjusted through the bias current, I_B.

The analysis of the proposed meminductor emulator yields the following input impedance function.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{s^\alpha C_\alpha M_R}{2g_m} \quad \ldots (10)$$

It is observed from (10) that it realizes a fractional order meminductor with mem-inductance given as

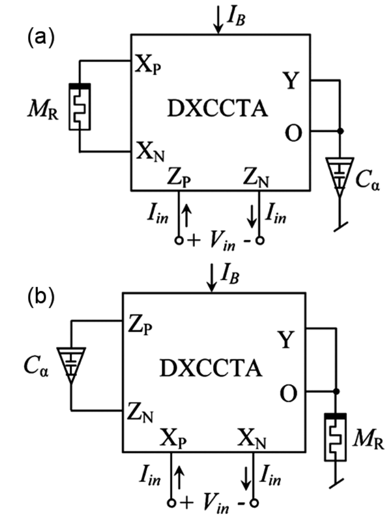

Fig. 1 — Proposed mem-element mutators' design (a) meminductor emulator; and (b) memcapacitor emulator

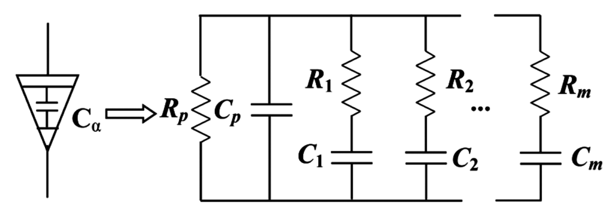

Fig. 2 — Fractional capacitor using Valsa's approximation[28]

$M_L^\alpha = \frac{C_\alpha M_R}{2g_m}$. In (10), M_R is the memristance of the memristor.

By putting $s = j\omega$ in (10), the input impedance function can be written as follows.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{\omega^\alpha C_\alpha M_R}{2g_m} e^{\frac{j\alpha\pi}{2}} \quad \ldots (11)$$

The analysis of the proposed memcapacitor yields the following input impedance function.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_m M_R}{s^\alpha C_\alpha} \quad \ldots (12)$$

It is observed from (12) that it realizes a fractional order memcapacitor with mem-capacitance given as $M_C^\alpha = \frac{C_\alpha}{g_m M_R}$. By putting $s = j\omega$ in (12), the input impedance function can be written as follows.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_m M_R}{\omega^\alpha C_\alpha} e^{\frac{-j\alpha\pi}{2}} \quad \ldots (13)$$

4 Non-ideal Analysis

Thenon-ideal terminal relationships of DXCCTA are described as follows.

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & 0 & 0 & 0 & 0 & 0 \\ -\beta_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & \delta_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & \delta_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\gamma g_m & \gamma g_m & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP} \\ V_{ZN} \\ V_O \end{bmatrix} \quad \ldots (14)$$

In Eq. (14), γ represents the transconductance inaccuracy, β_1, β_2 represent the non-ideal voltage transfer gain and δ_1, δ_2 represents the non-ideal current transfer gain. The routine analysis of proposed meminductor by incorporating the non-idealities yields the following input impedance function.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{s^{\alpha} C_{\alpha} M_R}{\delta(\beta_1+\beta_2)\gamma g_m} \quad \ldots (15)$$

The observed mem-inductance from (15) is given as follows.

$$M_L^{\alpha} = \frac{C_{\alpha} M_R}{\delta(\beta_1+\beta_2)\gamma g_m} \quad \ldots (16)$$

The analysis of the proposed memcapacitor by incorporating the non-idealities yields the following input impedance function.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{\delta\beta\gamma g_m M_R}{s^{\alpha} C_{\alpha}} \quad \ldots (17)$$

The observed mem-capacitance from (17) is given as follows.

$$M_C^{\alpha} = \frac{C_{\alpha}}{\delta\beta\gamma g_m M_R} \quad \ldots (18)$$

It is observed from (16) and (18) that mem-inductance and mem-capacitance are affected by non-idealities of DXCCTA. However, these non-idealities are effective only at very high frequencies and are unity at lower frequencies, hence their effect could be neglected at lower frequencies.

5 Results

The proposed fractional-order mem-element emulators are simulated via PSPICE using 0.18 µm CMOS technology. The CMOS structure of DXCCTA is shown in Fig. 3[22]. The transistors sizes are listed in Table 2. The supply voltages used are ±1.25 V and bias current I_B is set to 90 µA. The memristor circuit[29] is used to test the proposed fractional-order mem-element emulators. The capacitor value used in memristor circuit is set to 30 pF.The circuit of mem-inductor is simulated at first. A sinusoidal voltage source of 80 mV is applied at the input. A fractional capacitor, $C\alpha$ of 20 pF/sec$^{1-\alpha}$ is used in the simulation results. The values of resistors and capacitors involved in the VALSA model of fractional capacitorare given in Table 3. The input flux of mem-inductor is directly proportional to the voltage of capacitor $C\alpha$. Therefore, voltage of capacitor $C\alpha$ is used to represent the input flux as flux is not directly measured electric quantity. The transient characteristics of mem-inductor for input current and voltage of capacitor $C\alpha$ (which is directly proportional to input flux) at 500 kHz frequency are shown in Fig. 4. The pinch hysteresis characteristics

Table 2 — MOS transistors aspect ratios

MOS Transistors	W(µm)/L(µm)
M_1, M_2	0.36/0.18
M_3–M_5, M_{14}, M_{15}	0.72/0.18
M_{16}–M_{18}	1.2/0.18
M_6-M_{13}, M_{19}, M_{20}	2.4/0.18
M_{21}, M_{22}	3.6/1.8
M_{23}–M_{26}	7.2/1.8
M_{27}, M_{28}	2.4/1.8

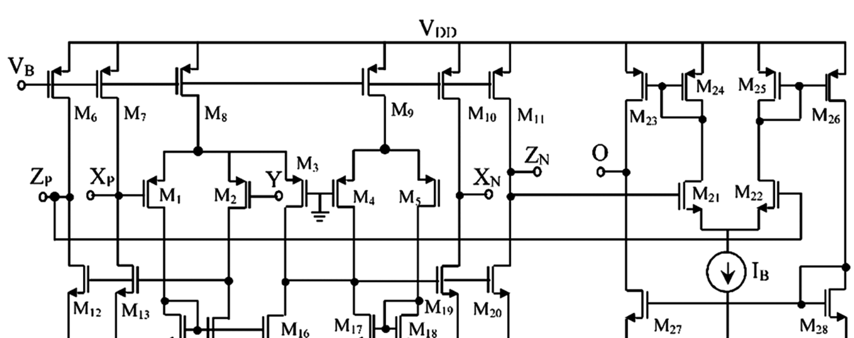

Fig. 3 — CMOS structure of DXCCTA

Table 3 — Values of resistors and capacitors used in fractional capacitor 20 pF/sec$^{1-\alpha}$

α	R_P	R_1	R_2	R_3	R_4	R_5	C_P	C_1	C_2	C_3	C_4	C_5
0.95	408.9M	86.9M	15.2M	2.7M	0.47M	82.2k	8.3p	1.15p	1.05p	0.96p	0.87p	0.8p
0.9	293.7M	69.8M	13.4M	2.6M	0.49M	95.3k	3.42p	1.43p	1.2p	0.99p	0.83p	0.69p

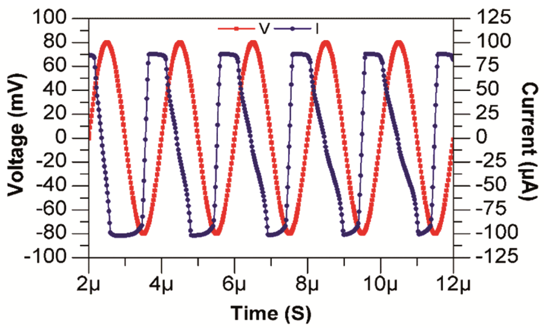

Fig. 4 — Transient responses of mem-inductance emulator at *f* = 500 kHz

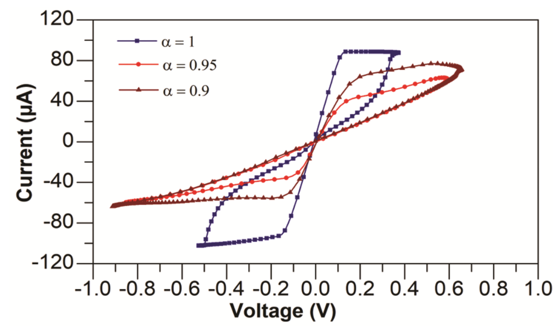

Fig. 6 — Pinch hysteresis characteristic of meminductor for different values of *α* at *f* = 600 kHz

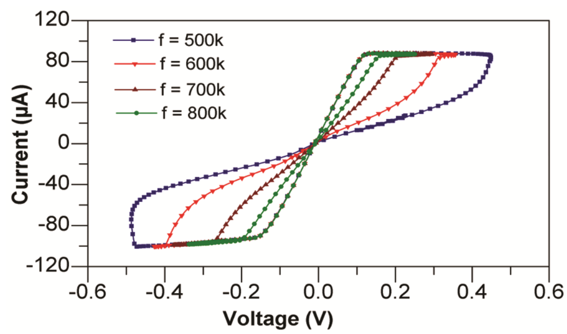

Fig. 5 — Pinch hysteresis characteristic of meminductor for different values of frequency at *α* = 1

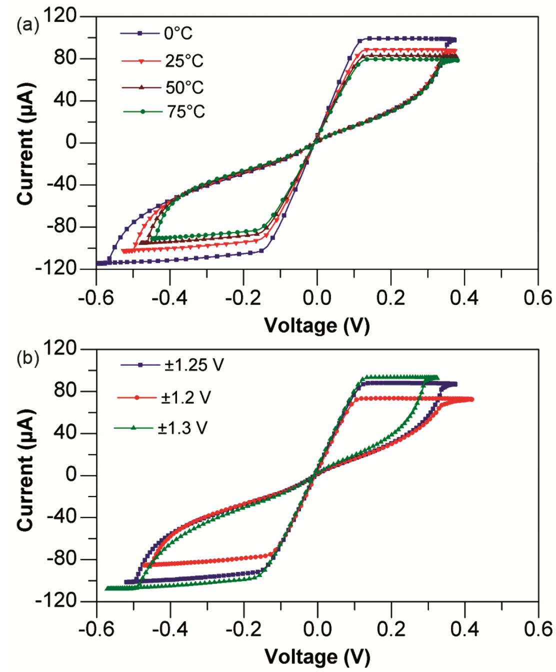

Fig. 7 — Pinch hysteresis characteristic of meminductor for different values of (a) temperature; and (b) supply voltages

observed between input current and flux at different frequencies when *α* = 1 are shown in Fig. 5. The pinch characteristics observed between input current and flux at different values of *α* at 600 kHz frequency are shown in Fig. 6. The performance of the proposed mem-inductor emulator is further checked against PVT variations. Fig. 7(a) shows the pinch hysteresis characteristics at different temperatures (0, 25, 50 and 75°C) and Fig. 7(b) shows the pinch hysteresis characteristics at different supply voltages (±1.2, ±1.25 and ±1.3 V). Monte Carlo simulations are performed for 100 runs for a 5% variation in threshold voltages to check the performance of mem-inductor emulator against process variation. The corresponding MCS results are depicted in Fig. 8 in the form of histogram for variation in input current frequency. The mean value of input current frequency is found 615 kHz (2.5% deviation from theoretical value). The non-volatility of the proposed mem-inductor emulator is tested by applying a voltage pulse with 20 ns pulse width and 100 ns pulse period and 80 mV in amplitude. Figure 9(a) shows the transient responses for incremental mem-inductor emulator. The mem-inductance increases during the ON time of pulse and the last value is retained during the OFF time of pulse. The transient responses of decremental mem-inductor emulator are shown in Fig. 9(b). The mem-inductance decreases during the ON time of pulse and the last value is retained during the OFF time of pulse.

The circuit of mem-capacitance emulator is further simulated. A sinusoidal current source of 20 µA is

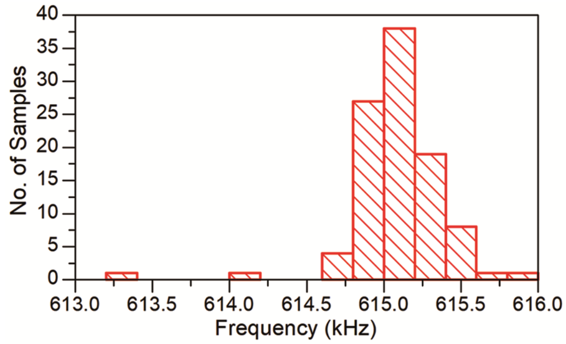

Fig. 8 — MCS results depicting histogram of input current frequency for variation in threshold voltages

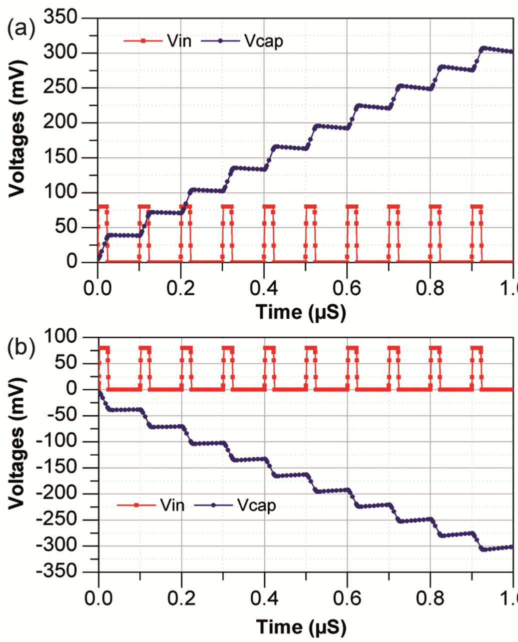

Fig. 9 — Transient responses of the proposed emulator for (a) incremental meminductor; and (b) decremental meminductor

applied at the input. The input charge of mem-capacitor is directly proportional to the voltage of capacitor *Cα*. The transient characteristics of mem-capacitor for the developed input voltage and voltages of capacitor *Cα* (which is directly proportional to input charge) at 540 kHz frequency are shown in Fig. 10. The pinch characteristics between input voltage and charge at different frequencies when α = 1 are shown in Fig. 11. The pinch hysteresis characteristics between input voltage and charge (voltages of capacitor *Cα*) at different values of α at 540 kHz frequency are shown in Fig. 12. The non-volatility of the proposed mem-capacitor emulator is tested by applying a current pulse with 50 ns pulse width and 120 ns pulse period and 20 μA in amplitude. Fig. 13 shows the simultaneously obtained

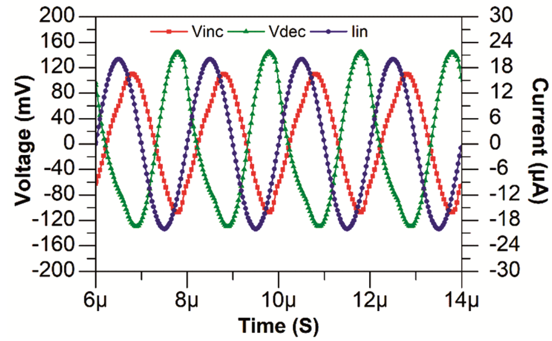

Fig. 10 — Transient responses of mem-capacitance emulator at 500 kHz

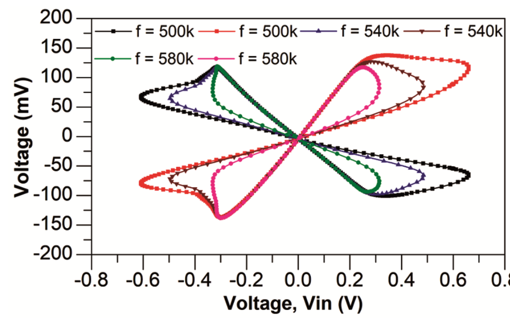

Fig. 11 — Pinch hysteresis characteristic of memcapacitor for different values of frequency at $\alpha = 1$

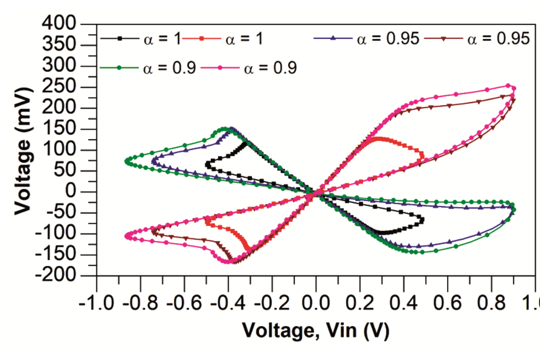

Fig. 12 — Pinch hysteresis characteristic of memcapacitor for different values of α at f = 540 kHz

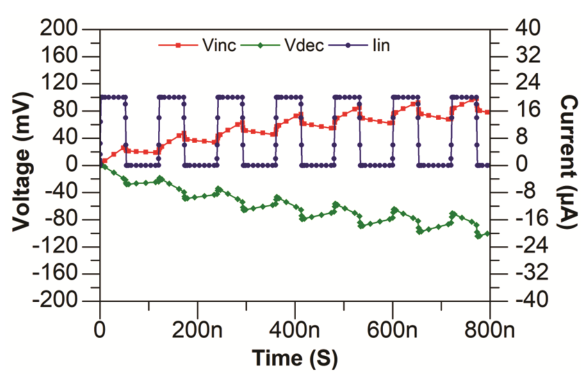

Fig. 13 — Transient responses of the proposed mem-capacitance emulator

transient responses for incremental and decremental mem-capacitor emulator. The mem-capacitance increases and decreases respectively for incremental and decremental mem-capacitor emulator during the ON time of pulse and the last value is retained during the OFF time of pulse.

6 Conclusion

The proposed fractional-order mem-element mutators based on DXCCTA offer a promising and efficient solution for emulating meminductors and memcapacitors with fractional-order characteristics. The design utilizes only one DXCCTA, one memristor, and one fractional capacitor, making the circuit both simple and cost-effective. Through PSPICE simulations, using 0.18 µm CMOS technology and ±1.25 V supply voltages, the proposed mutator circuits have demonstrated excellent performance in terms of both accuracy and robustness across various conditions with operational frequency up to 800 kHz and a power consumption limited to 2.5 mW. The designed mem-elements exhibit non-volatility and pinch hysteresis characteristics, which are critical for applications in memory-dependent systems. Overall, the DXCCTA-based mem-element mutators offer a highly effective, practical, and versatile solution for simulating fractional-order behaviors in modern electronic circuits. Their performance in both theoretical and simulation tests paves the way for future applications in advanced control systems, signal processing, and neuromorphic computing, where such memory-dependent and non-linear characteristics are essential.

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