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Dynamic Characteristics of LIF Neuron Circuits Using CMOS and Volatile Memristor Devices

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For several years, the Von Neumann architecture has been the foundation of contemporary computers. The straightforward, less intricate, and easy-to- use nature of this architecture for the processor and memory design, makes this computational framework popular among the other architectures over the past years. The application of this architecture is not sufficient for parallel processing and complex computational tasks. Hence, this has created a huge demand for the architecture that supports extensive parallelism, energy efficiency and scalability. In this regard, researchers are exploring non- Von Neumann architectures like neuromorphic computing systems, which are proved to be potential candidate for the construction of neuron and synapse circuits of the architecture. In this work, CMOS and volatile memristor- based leaky-integrate- fire (LIF) neuron circuits are simulated and analyzed using Cadence Virtuoso. Further, the circuits are compared with respect to attributes such as frequency of spikes, spike duration, pattern of spikes, spiking nature, complexity of the circuit, frequency adaptation, reset circuit requirement, and energy per spike among others. In addition, the work explores and showcase the effect of various input, circuit and memristor device parameters on the spiking nature of the volatile LIF neuron circuit.

Keywords: Non-Von Neumann architecture, Spiking neural network (SNN), Frequency adaptation, Volatile neuron

1 Introduction

The neuromorphic computing systems have been able to replicate the functionalities of the human brain effectively. The systems built utilizing this technology are classified as non-Von Neumann architectures since they perform the data storage and processing in the same location. The characteristics of the neuromorphic technology such as parallelism, greater energy efficacy, high integration with CMOS, scalability and co-existence of storage and processing of data makes it a good candidate for artificial intelligence and machine learning applications that require large amounts of data[1]. Spike neural networks (SNN) are a common implementation of this computational architecture, consisting of synapses and neurons. The pre-synaptic neurons of SNN processes the incoming data spikes and transmits the processed spikes to post synaptic neurons via synaptic devices[2]. Bio-plausible models of neurons and synapses have been successfully created using traditional CMOS technology. However, the complex design, high density inheritance, limited scalability, and high-power consumption of CMOS devices hinder their usage in the development of neuromorphic technology. Hence there is a huge exploration in the construction of neuromorphic computing systems utilizing emerging devices, which in turn results in efficient neuron and synapse circuits.

Memristor is an emerging device offering appealing characteristics like non-volatility, less silicon area, rich device dynamics, energy efficiency, and among others. Memristor is further categorized into non-volatile and volatile devices. The volatile type memristor have gained a lot of attention lately as a means for developing neuron and synaptic models. The volatility of the memristor provides it the capability to demonstrate the short-term memory of the neuron[3].

This work considers the implementation and analysis of LIF type neuron model, which is a fundamental idea in computational neuroscience that is well-known for its ease of use and effectiveness in mimicking the behavior of biological neuron. The model describes the dynamics of a neuron as an integrator of synaptic currents with a leaky membrane potential that gradually decreases with time. The neuron fires and generates output spikes when the membrane potential rises above a predetermined threshold. The hardware implementation of large-scale neuromorphic systems is boosted by this neuron

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model due to its scalability, real-time simulation capabilities, and its computational efficiency[4]. Traditional CMOS technology has been extensively utilized for the implementation of neuron circuits due to its mature fabrication processes and compatibility with standard electronic design tools. Low-power operation, fast processing, and scalability are features of CMOS- based LIF neuron circuits that make them ideal for a variety of applications, ranging from machine learning to sensory processing. These circuits have complex circuit designs, huge energy demand and utilize a larger number of transistors and capacitors to simulate the dynamics of biological neurons. This has led to the successful usage of volatile memristors for the deployment of LIF circuits. The special properties of memristor devices are exploited by LIF circuits to implement synaptic weights and neuronal dynamics in a compact and energy-efficient manner. In contrast to conventional CMOS techniques, memristor-based implementations take advantage of the inherent memory and analog computing capabilities of the memristor device, which opens up new architectural and computational paradigms. Memristor-based neuron circuits can demonstrate learning and self-organization abilities due to their dynamic adaptability, opening the door for neuromorphic systems that are more resilient as well as responsive to changes in their environment. Through investigating volatile memristors' potential in neuromorphic computing, this work opens up new directions for the development of artificial intelligence systems, pushing them toward increased cognitive capacity and energy efficiency. In this work, exploration of complexities and analysis of LIF neuron circuits employing two diverse devices, such as volatile memristor and complementary metal oxide-semiconductor (CMOS) is carried out. The novelty of this investigation lies in a comprehensive comparative analysis of CMOS and volatile memristor-based LIF neuron circuits concerning attributes such as spike nature, spiking rate, circuit complexity, energy consumption per spike, spike strength, spiking pattern, and frequency adaptation. This contrast reveals the capability of memristor technology to surpass the constraints of conventional CMOS circuits in neuromorphic computing applications.

The following is the structure of the remainder of the paper. In section 2, a brief discussion is provided on the conceptual modeling of the LIF neuron circuit using resistor-capacitor components. Section 3 covers the examination of the CMOS-based LIF circuit's functioning. At the output, the CMOS-based LIF circuit generates monophasic spikes that encompass responses related to linearity and non-linearity of the circuit. The operational characteristics and analytical justification of the volatile memristor-based LIF circuit are covered in section 4. The comparison of various parameters and behavioral characteristics of two considered neuron circuits is presented in section 5.

2 Materials and Methods

2.1 The Leaky Integrate Fire Neuron Model

Neural networks are primarily composed of neurons, which are nodes that are mathematically expressed and are responsible for data distribution and processing. Various models of neuron, such as the Hodgkin Huxley (HH)[5], LIF , integrate and- fire (IF)[4], Izhikevich[6], and AdExIF[7] models, have been extensively studied for circuit structure, merits, and faults despite the lack of comprehending neural network activity. Because of the straightforward implementation, the LIF neuron model is well-liked by neural network topologies, particularly SNN. In the absence of any input current, the membrane potential of this model progressively approaches towards its resting potential[8].

The circuit of the LIF neuron model is represented in Fig. 1 and it offers an understandable representation of the basic principles that govern neuronal function. The model captures core neuron dynamics with suitable placement of electrical components, each of which represents an essential component of brain function. Essentially, the circuit consists of a leaky resistor (R_{leak}) that replicates the passive discharge phenomenon and a capacitor (C_{mem}) that represents the membrane capacitance of the neuron. Interestingly, a voltage-controlled switch in series with the capacitor functions as a symbolic threshold

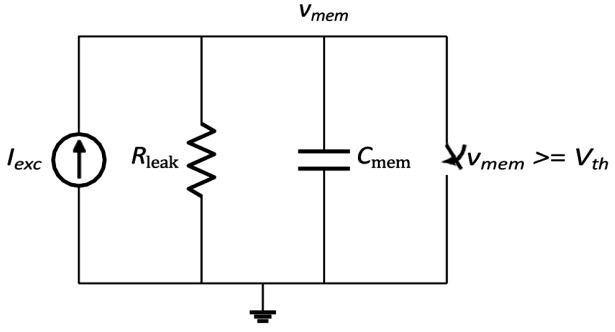

Fig. 1 — Conceptual LIF neuron structure

mechanism, precisely controlling when synaptic inputs cause neurons to fire. The circuit's integration of input excitation current I_{exc} sets of series of spiking events: firstly, the membrane potential gradually builds up the charge across the membrane capacitor, representing input integration; secondly, when the membrane potential exceeds a predetermined threshold at which point the output spikes are generated, modeling the firing process seen in biological neurons. The model then smoothly moves into a resetting phase, which primes the neuron for more excitations by returning the membrane potential to a predetermined resting voltage after this neuronal discharge.

The study of spike frequency modulation in response to different input strengths offer additional analysis of the complexities of neuronal behavior. Specifically, stronger inputs accelerate the process of charge accumulation, which in turn accelerates the membrane potential's ascent toward the firing threshold and increases spike frequency. Conversely, weaker inputs delay the discharge process, which results in a lower spike frequency. The intricate interactions between electrical components are dynamic and closely resemble the physiological workings of neurons, offering important insights into the mechanics behind brain computing. The LIF circuit model provides a complex comprehension of the intricate interactions between electrical signals and computational processes in the brain, demonstrating the remarkable synergy between neuroscience and electrical engineering through its detailed representation of neuronal dynamics. The LIF neuron model is often described using a simple first-order differential equation that captures the dynamics of the neuron's membrane potential. The LIF neuron model's differential equation describes how the membrane potential changes over time in response to input excitation and leakage currents. The equation is derived based on Kirchhoff 's current law for the conservation of charge[1]. The equation is typically expressed as:

$$\tau_{mem}\frac{dV_{mem}(t)}{dt} = -V_{mem}(t) + R_{leak}\, I_{exc} \quad \text{... (1)}$$

where I_{exc} represents input excitation current, $V_{mem}(t)$ is the instantaneous membrane potential, R_{leak} is the leakage resistance, τ_{mem} is the time constant of the circuit, and derivative of $V_{mem}(t)$ reflects rate of change in membrane potential over time, which encapsulates the dynamics of a neuron's membrane potential.

2.2 CMOS LIF Neuron Model

The CMOS-based LIF neuron circuits is a traditional way of implementing neural models, which mimic the behavior of biological neurons to a closer degree. The CMOS-based LIF circuit considered for the analysis[9] is shown in Fig. 2. The parasitic capacitance C_{mem} at node N serves as the neuron membrane capacitance and is charged through PMOS transistor M_1. The applied input excitation voltage is converted to excitation current I_E by M_1. The parasitic resistance R_{mem} at N represents the leaky component of the neuron model. Further, the transistor M_6 implements spike frequency adaptation mechanism and the output spike frequency f_{spike} is controlled via its gate voltage V_C. With V_E and V_C set to a value equal to V_{supply}, no spikes are generated, and the circuit is said to be in the rest state. As V_E drops below V_{supply}, an excitation current is injected to the node N through M_1. The charge on the parasitic capacitance C_{mem} accumulates and the membrane potential V_{mem} increases (integration process). Once the nodal voltage V_{mem} reaches a value equal to the threshold voltage of M_5, V_1 declines and in turn activates M_7 and causing spike generation at the output (firing process). The degradation in V_{mem} triggers the M_4, which reduces the output spikes and completes the spike creation process. If, in case the I_E is insufficient to trigger M_5, no spikes occur, and potential across C_{mem} discharges due to leakage component. Greater value of excitation currents results in shorter charge times and higher spike frequency, and vice-versa. As shown in Fig. 2, sub- sections of the circuit accomplishing the function of biological neuron are as follows: integration, threshold, firing, reset, and spike frequency adaptation sections. Accurate modeling of these sections under consideration meets the requirements of an effective LIF neuron model. The excitation current I_E passing through M_1 can be expressed as

$$I_E = I_{C_{mem}} + I_{R_{mem}}, \quad \text{... (2)}$$

where $I_{C_{mem}}$ and represents current through parasitic membrane capacitor and resistor respectively. This equation reflects the combined currents through capacitor membrane and the leakage component and can be modified as

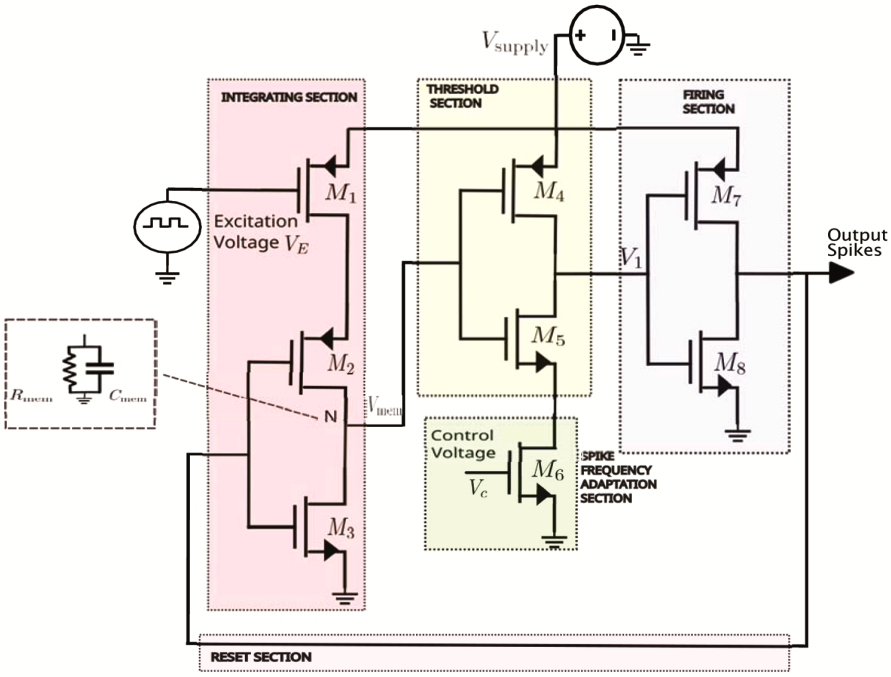

Fig. 2 — CMOS-based LIF neuron circuit with spike frequency adaptation[9]

$$I_E = C_{mem}\frac{dV_m}{dt} + \frac{V_m}{R_{mem}} \quad \text{... (3)}$$

Equation (3) establishing the relationship between excitation current and membrane potential, represents a simple first-order differential equation, similar to Eq. (1). The phenomenon of spike frequency adaptation is observed in neurons when an ongoing stimulation causes a shift in the firing rate due to certain circuit parameters. The transistor M_6 implements frequency adaptation in the circuit via voltage V_C. Reducing V_C causes V_1 to discharge at faster rate, which in turn lowers frequency of spiking, and vice- versa. The realization of LIF operation without the utilization of external resistor-capacitor components makes this circuit area efficient with respect to other CMOS based LIF circuits[9]. The simulation of neuron using CMOS is carried out in Cadence Virtuoso environment using 180 nm technology. The parameters considered for the simulation are as follows: V_E during off and on period is 0.5 and 2 V respectively, time period is 36 ns with 50 % of duty cycle, $V_{supply} = 1.8$ V, and $V_C = 0.5$ V . The circuit generates spikes with $f_{spike} = 333.7\,MHz$ during the period for which $V_E = 0.5\,V < V_{supply}$. The simulation results for the aforementioned conditions are shown in Fig. 3. The control voltage V_C is varied over a range to observe the frequency adaptation mechanism. The Table 1

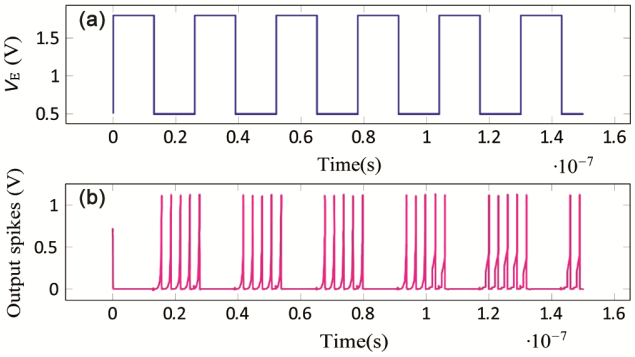

Fig. 3 — Simulation results of CMOS LIF circuit for $V_C = 0.5$

Table 1 — Influence of control voltage on spike frequency

$V_C(V)$	1.8	0.9	0.7	0.5
$f_{spike}(Hz)$	4.61E+09	4E+09	2.68E+09	333E+06

indicates the influence control voltage on spike frequency. From the above it is evident that the reduction in V_C causes decrease in f_{spike}. Further, energy consumption per spike is one of the significant attributes of the neuron circuit, proper tuning of which leads to the construction of efficient neural networks. The energy consumption per spike is evaluated using the following expression.

$$E = \frac{\int_{t_1}^{t_2} i(t)\, V_{supply}\, dt}{N} \quad \text{... (4)}$$

where V_{supply} and $i(t)$ are values of the current and voltage drawn from supply respectively. The t_1 and t_2 represents the boundary values of time range over which the energy calculation is performed. The number of spikes over the integral time is represented by *N*. Compared to high frequency spiking, low frequency spike generation demands more power from the circuit. The primary cause for this is, extended conduction of transistors of the inverters at high gain during low frequency spiking. As per Eq. (4), the energy per spike at 333 MHz is evaluated to be 138.5 fJ.

2.3 Volatile LIF Neuron Model

2.3.1 Volatile Memristor SPICE Model

The development of a volatile memristor model addresses the need to capture the short-term retention of resistance state, which in turn imitates the short-term memory characteristics of biological neurons. Traditional memristor models have primarily focused on non-volatile behavior, overlooking transient responses and limited retention times exhibited by real-world devices. In this work, the SPICE model of volatile memristor[10] is considered for the implementation of LIF neuron circuit and the sub-circuits of the model is shown in Fig. 4.

The volatile circuit computes the current and maintains state information for variable 'x'. This sub-circuit models the short-term, transient response of the memristor, akin to volatile resistance switching. The non-volatile sub module 'y' is designed to simulate longer-term state retention, and it contributes to the non-volatile behavior of the memristor. The charge accumulation sub-circuit monitors the cumulative current through the memristor and triggers transitions from volatile to non-volatile behavior. The state variable 'z' represents the accumulation of charge based on the history of current through memristor model.

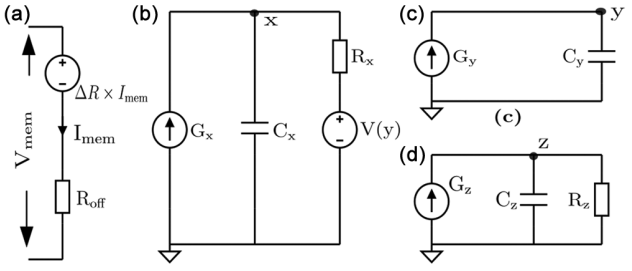

Fig. 4 — Sub-circuits of the memristor model (a) Output sub-circuit (b) Volatile sub- circuit (c) Non-volatile sub-circuit; and (d) Charge sub-circuit[10]

The set of equations defining the sub-circuits are as follows,

$$R_{mem}(x) = x.R_{on} + (1-x).R_{off} \quad \text{... (5)}$$

$$C_x \frac{dx}{dt} = \frac{x-y}{R_x} + I_0(x) \quad \text{... (6)}$$

$$C_z \frac{dz}{dt} = I_{mem} - \frac{z}{R_z} \quad \text{... (7)}$$

$$C_y \frac{dy}{dt} = \begin{cases} I_0(y), for\ z > q_p\ and\ V_{mem} > 0 \\ I_0(y), for\ z > q_p\ and\ V_{mem} > 0 \\ 0, else \end{cases} \quad \text{... (8)}$$

$$I_0(h) = \frac{I_{mem} \cdot \mu_v \cdot R_{on} \cdot f(h)}{D^2}, \quad \text{... (9)}$$

where R_{on}, R_{off}, and R_{init} establishes the initial conditions as well as the boundaries of resistances, x_0, y_0, and z_0 represents the initial values of the state variables of x, y and z respectively of the model. R_x determines the time constant of the volatile state decay, while C_x regulates the amount of volatile resistance switching about input stimuli; C_y sets the rate of nonvolatile; the threshold parameters q_p and q_n determine when non-volatile switching activity begins; C_z and R_z form a leaky integrator that monitors a voltage z proportionate to the charge that flows through the device. The internal variable z is used to condition the dynamic change of y, making the model more responsive to varied spatial stimuli. The SPICE code of the aforementioned memristor model is converted into symbol in Cadence Virtuoso and pin configurations are set accordingly. The created symbol is instantiated in the schematic editor for the further simulation of memristor-based LIF neuron circuit.

The Fig. 5 illustrates the variation of memristance in response two distinct values of input amplitude. The

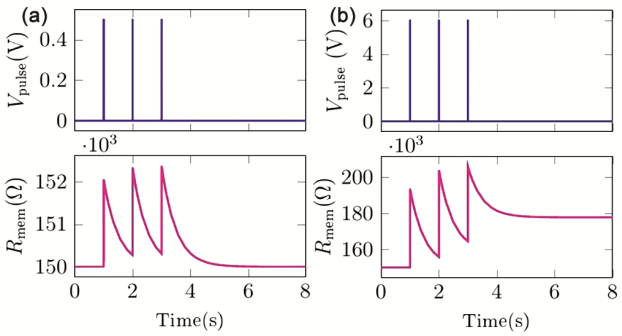

Fig. 5 — (a) Volatile switching characteristics of the memristor model for V_{pulse} = 0.5, inter pulse interval of 1 s; and (b) Non-volatile switching behavior of the memristor model for V_{pulse} = 6 V, inter pulse interval of 1s

device exhibits volatile nature under weaker stimulus, in this scenario device returns to the initial resistance value after the withdrawal of the input excitation. In case of stronger input stimulus, the device illustrates non-volatility and hence retains the resistance value even after the removal of input source. This clearly demonstrate the volatile and non-volatile switching nature of the considered memristor SPICE model. The SPICE code of the model is transformed to symbol and is used in simulation of neuron circuit in Cadence Virtuoso.

2.3.2 LIF Neuron Circuit using Volatile Memristor Model

The integration of volatile memristor into the LIF neuron model offers a significant advancement in the performance parameters of spike neural net- works. The volatility of the device paves way in incorporating short term memory in the neuron circuit. The memristor based LIF neuron circuit is shown in Fig. 6. The input pulses from the source V_{pulse} charges the mem- brane capacitor C through membrane resistance R. The capacitor is employed to simulate cell membrane capacitance, while the memristor is utilized to model ion channel conductivity. Upon the attainment of threshold voltage by C, the memristor shifts to the low resistance state (LRS), which initiates the discharging of the capacitor through the volatile memristor. The LIF circuit constructed detects this as a "firing event". The memristor device switches back to high resistance state (HRS) following the firing process and this demonstrates volatile nature of the device. Hence, there is no requirement of reset circuitry for the LIF circuit. The firing process, spike frequency, latency and other behavior of the neuron can be altered by varying volatile memristor device and circuits parameters.

Simulation of the volatile memristor based LIF circuit is carried out by exciting the circuit with continuous sequence of pulses with an amplitude of 2 V and time period of 2 ms with 75 % of duty cycle. The initial value of the device resistance R_{init} is set to 55 kΩ, R_{on} and R_{off} values are set to 1 Ω and 100 kΩ respectively. The other parameters of the memristor model are listed in Table 2 . As depicted in Fig. 7 the capacitor voltage reaches the threshold value during the sixth input pulse, the circuit produces a single current spike at the output node with a strength of 270 μA.

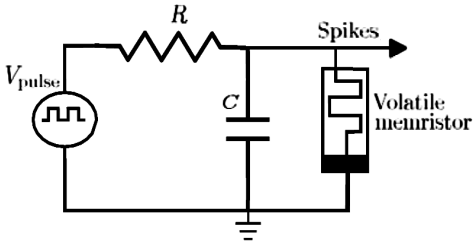

Fig. 6 — Volatile memristor model based LIF neuron circuit

The behavior of the LIF circuit is dependent on multiple factors such as input parameters, membrane capacitance, neuron resistance and memristor device attributes. It is observable that for a given capacitance value, the R_{init} of the device and neuronal resistance values sets the value of threshold voltage of the neuron circuit. The neuron circuit fires at different instant of time as the input pulse width varies. Compared to inputs with shorter pulse duration, the capacitor achieves the threshold voltage more rapidly as the pulse width increases and hence there is firing at different instant of time. The Fig. 8 depicts the effect on the firing for two different input pulse widths.

As the input amplitude reduces, the capacitor requires a greater number of input pulses to charge to the threshold level. This process leads to delayed firing action and decreased spike current. The influence of the input amplitude on the spike latency and the spike current is depicted in Fig. 9. It can be observed that as the input voltage decreases from 2 to 1.5 V the time of firing and spike current decreases from 274.5 to 178 μA respectively. The initial resistance of the volatile

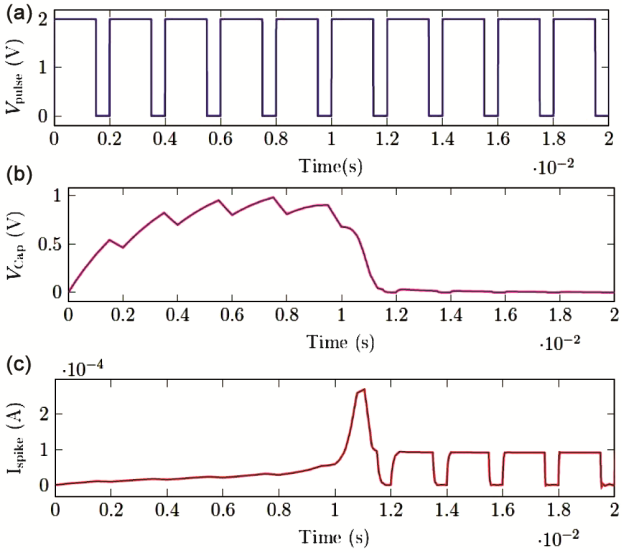

Fig. 7 — Results of a volatile memristor-based LIF neuron simulation (a) Input stimulus (b) Voltage across capacitor; and (c) Single current spike

Table 2 — Parameters of volatile memristor device

Metrics	D	R_x	R_z	C_x	C_y	C_z	μ_v	q_p	q_n
Values	10 nm	1 Ω	0.1 Ω	0.5 Ω	1 F	1 F	100 p	100 nV	-80 nV

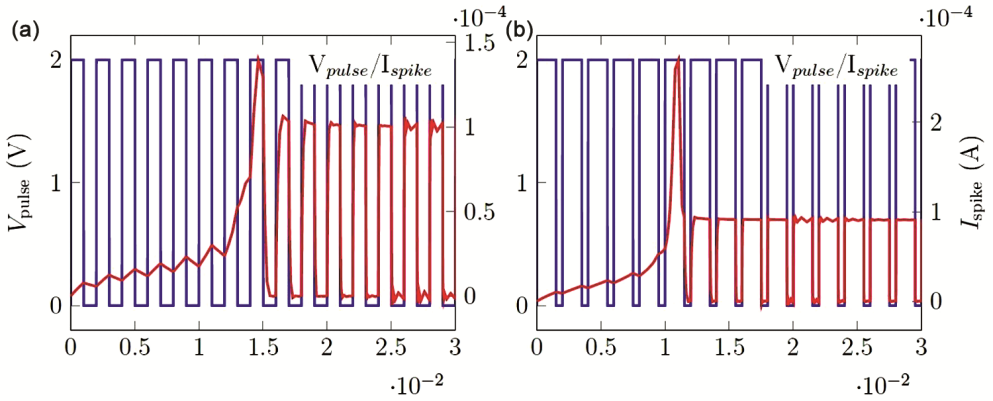

Fig. 8 — Influence of input pulse duration on the spike latency (a) Spiking for input pulse duration of 2 ms; and (b) Spiking for input pulse duration of 1.5 ms

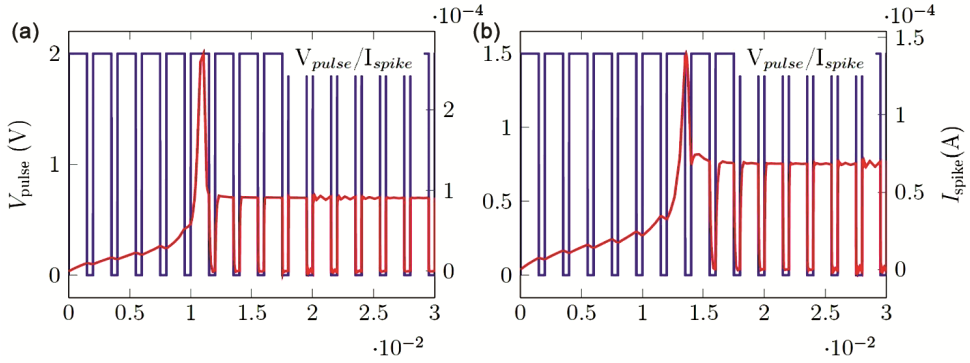

Fig. 9 — Effect of input pulse amplitude on the firing event (a) Output current spike for $V_{pulse} = 2\,V$ (b) Output current spike for $V_{pulse} = 1.5\,V$

memristor represents the resting state of the neuron. The value of R_{init} determines the time taken by the neuron circuit to generate the spiking. For fixed values of neuron membrane resistance and capacitance, R_{init} controls the number of pulses required to charge the capacitance to the threshold value. Greater is the value of R_{init}, the circuit requires more input pulses to deliver a spike at the output. The relationship between $R_{init}$and spike latency of the neuron is shown in Fig. 10.

The short-term memory component of a biological neuron is modeled by the memristor device's volatile nature. In this work, volatility of the device under consideration is validated through simulation of the neuron circuit by providing two input train of pulses separated by resting period. Specifications of the input excitation is as follows: pulse train is composed of 5 pulses with an amplitude 2 V and ON period of 2 ms with a 50 % duty cycle. The pulse trains are separated by the resting period of 700 ms. For the aforementioned simulation conditions, firing event occurs at 5th and 4th pulse of first and second pulse train respectively. The instance at which firing occurs can be further tuned by proper selection of resting period and membrane resistance values. During the resting period the device

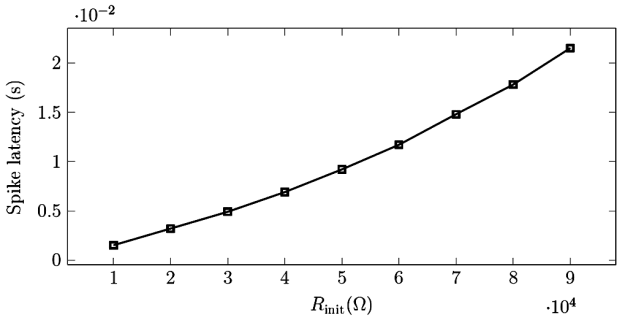

Fig. 10 — Spike latency as a function of R_{init}

resistance gradually returns back to the initial value. The need for the reset circuitry is eliminated due to the volatility of the device and hence circuit becomes more compact. The Fig. 11 illustrates the volatile resistance switching mechanism of the memristor device. Further, an important figure of merit of the neuron circuit[11], the energy per spike is evaluated to be 53 nJ for the aforementioned simulation conditions utilizing.

$$E_{spike(mem)} = V_{spike(mem)} \cdot I_{spike(mem)} \cdot t_{spike} \quad \ldots (10)$$

where $V_{spike(mem)}$ is the spike voltage, $I_{spike(mem)}$ is the spiking current and t_{spike} is the minimum spike width.

3 Results

3.1 Comparison of the CMOS and Volatile LIF Neuron Circuits

The simulation of CMOS and volatile-based LIF neuron circuits is per- formed in Cadence Virtuoso platform and the spiking behavior of both the circuits are demonstrated. The 180 nm technology-based CMOS LIF circuit is composed of eight transistors, out of which one of the transistors is dedicated for the implementation of the adaptive frequency mechanism. The spike frequency is modulated with respect to the control voltage and there exists a directly proportional relationship between the two parameters. This circuit's capacitor-less design enhances its area efficiency relative to capacitor-based CMOS neuron circuits documented in the literature. A brief comparison with current literature is as follows. A CMOS-based LIF neuron circuit employs 12 MOS transistors and 1 capacitor[12]. The necessity of an external capacitor in the design leads to an augmented area demand. The circuit demonstrates an elevated energy per spike of 1.099 nJ, and the spiking event is inherently non-adaptive. The study[13] demonstrates a CMOS neuron circuit comprising 10 MOS transistors and 2 external capacitors, resulting in increased area occupancy. The neuronal circuit has a maximum operational frequency cutoff of 343 kHz and is innately non-adaptive. A CMOS-NEMS hybrid LIF neuron circuit[14], employing 13 MOS transistors and 2 capacitors. The reset circuitry of the device is constructed utilizing an external MOS transistor and capacitor. The circuit has adaptive characteristics, with spike frequency regulated by input current excitation. Whereas, the utilization of external capacitors for implementing reset and leaky functionality increases area requirements. The CMOS LIF neuron circuit considered in this work eliminates the need of external membrane capacitor and also provides adaptive spike action.

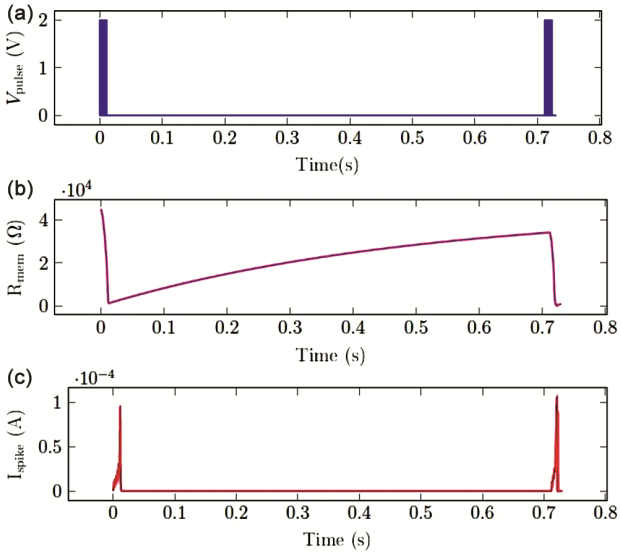

Fig. 11 — Simulation of volatile nature of the device (a) Input pulse train with a resting period of 700 ms (b) Variation in the memristance of the device (c) Current spike

The memristor-based LIF circuit utilized in this work, employs volatile memristor model to incorporate the short-term memory behavior and this makes the neuron to fire a single current spike rather than series of spikes in response to constant input stimulus. The energy consumption per spike of the circuit is in the range of nJ, which can be further reduced drastically for mega Hertz spike rate, as the energy per spike is inversely proportional to the number of spikes[15]. Hence, volatile memristor-based LIF is more energy efficient than the CMOS neuron counterpart and makes it more suitable candidate for the deployment of energy efficient and compact SNN. Further- more, compared to conventional CMOS neuron circuitry, the circuit yields a compact neuron circuitry by removing the necessity for the reset circuitry while utilizing fewer circuit components. In addition, compared to CMOS LIF circuit, the memristor LIF neuron takes up a smaller area given that the volatile memristor utilized is characterized with width of 3 nm. As per the simulation outcomes the comparison between the considered LIF circuits is tabulated in Table 3.

Table 3 — Comparison of the attributes of CMOS and volatile memristor-based LIF circuits

Attributes	CMOS	Volatile memristor
Type of neuron	LIF	LIF
Spike nature	Voltage	Current
Rate of spiking	MHz	KHz
Reset circuit requirement	Yes	No
Transistors	8	Nil
Spike strength	0.44 V	1.87 mA
Spike duration (s)	0.26 μ	0.51 m
Energy/Spike (J)	138.5 f @333 MHz	53 n @ 500 Hz
Membrane R and C	No	Yes
Refractory period (s)	Nil	Nil
Spike pattern	Burst spikes	Single spike
Frequency adaptation	Yes	No
Spike latency	No	Yes

4 Conclusion

The proposed work demonstrates the spiking characteristics of CMOS and volatile memristor-based LIF neuron circuits. The spike frequency of the capacitor-less CMOS neuron is regulated by the control voltage and the circuit generates a series of spikes in response to constant input stimulus. The generation of sequence of spikes for the unvarying excitation and usage of a greater number of transistors leads to higher energy per spike. In contrast, the volatile memristor based LIF circuit utilizes no transistors, eliminates the requirement of reset circuitry, and generates a single spike in response to the constant stimulus. Hence area occupancy and energy per spike consumption of the volatile neuron is reduced to greater extent. The memristor also offers control of the characteristics of spike via circuit as well as device parameters which makes it more versatile and suitable for implementation of SNN. In addition, the volatile and non-volatile behavior of the device is controllable via the applied input energy and this feature may be utilized to develop neuron circuit with both short- and long-term memory features. Finally, the study and exploration of emerging device-based neurons circuits lead to expansion of the horizon of neuromorphic computing systems.

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