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Highly-Stable and Lower-Power Static Random-Access Memory Design in Carbon Nanotube Field Effect Transistor Nanotechnology

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Carbon nanotube field-effect transistor (CNTFET) technology is emerging as a potential replacement for metal oxide semiconductor field-effect transistor (MOSFET) technology. CNTFET uses carbon nanotubes (CNTs) as a channel, due to which CNTFET technology displays superior electrical characteristics, like increased carrier mobility, ballistic carrier transport, and adjustable threshold voltage. While working with MOSFETs, different short-channel effects (SCEs) result in the degradation of various performance parameters. The MOSFET-based static random-access memory (SRAM) faces various SCEs, leakage, and higher power consumption at smaller technology nodes. Therefore, this research work proposes a CNTFET-based SRAM cell design that utilizes a reliable leakage minimization technique (LMT) to overcome these challenges. The proposed LMT-SRAM circuit is designed for low-power, high-performance embedded memory. To design the LMT-SRAM cell, a reliable leakage minimization block is inserted between the pull-up and pull-down networks of the cross-coupled inverters, which reduces the power dissipation. CNTFETs, because of their superior electrical properties, help the proposed design to achieve improved performance metrics. The proposed LMT-SRAM circuit is simulated with the Stanford University 32nm CNTFET technology model using HSPICE for a power supply of 0.9V and at room temperature conditions. The simulation results justify that the proposed CNTFET-based LMT-SRAM cell attains 98.6% reductions in average power dissipation when compared to previous designs. The proposed design shows 91.6% faster execution while in write mode and 33.6% faster execution while in read mode. The design has also shown remarkable stability and variability during read and write operations. The butterfly and N-curve methods are used to determine static noise margin (SNM) for the proposed LMT-SRAM cell. Monte Carlo (MC) simulations are performed to verify SNM stability across process, voltage, and temperature (PVT) variations. The Kolmogorov-Smirnov (K-S) test is also performed using MATLAB to determine the normality of the dataset obtained from the MC sample run.

Keywords: CNTFET, LMT-SRAM, SNM, Stability, Energy-efficient, N-curve, PVT, K-S Test

1 Introduction

To design efficient and compact electronic systems, continuous downscaling of transistors has raised several SCEs in MOSFET-based circuits, such as increased leakage current, reduced gate control, process variations, and increased power dissipation[1,2]. These emerging challenges affect the reliability and energy efficiency of circuits, which further questions miniaturization[2]. To counter these scaling issues in MOSFETs, researchers are exploring 'Beyond CMOS' alternative transistor technologies like fin-shaped field-effect transistors, CNTFETs, graphene nano-ribbon field-effect transistors, and quantum-dot cellular automata[3]. CNTFETs are considered the most appropriate substitute for transistor technology to be used in low-power applications with high-performance requirements[4]. The CNTFET device structure is analogous to the MOSFET with four terminals, i.e., drain, gate, source, and body, with the only difference in the channel. CNTFETs make use of CNTs as the semiconductor channel[5]. The CNT is obtained by rolling a graphene sheet into a cylindrical tube. The direction of rolling is determined by its chirality vector, which is a decisive factor for a CNT to be semiconducting or metallic[5].

CNTs have a unique one-dimensional band nanostructure, which restricts backscattering of charge carriers and reinforces the ballistic transport inside the CNT channel[5]. CNTFETs also demonstrate characteristics such as higher thermal conductivity, increased current-carrying capability, and less power dissipation. The CNTFET's gate induces complete control over the conductivity of the CNT-based channel, which enables energy-efficient and high-

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performance circuit operation[6]. Anticipating the vast artificial intelligence revolution, a critical need for high-speed on-chip memory with reduced power consumption and high performance is created[7]. Future low-power applications, such as mobile devices and high-performance computing systems, will consist of generative artificial intelligence chips, for which memory arrays are going to be an important constraint[7,8]. The efficient data storage and instant retrieval are critical for achieving high-performance operations. High-speed registers and cache memory in computing devices, which serve as temporary storage to accelerate data access, are implemented using SRAM[8]. SRAM accounts for a major share of transistors in microprocessor integrated circuits, which stresses the need for optimization of SRAM's power efficiency along with performance and an improved figure of merit[9]. To achieve an optimized SRAM, MOSFET devices ought to be replaced with CNTFET devices as a first step. The CNTFET device has low OFF-state current, high speed of operation, and adjustable threshold voltage[10].

This research work proposes a CNTFET-based SRAM cell, which incorporates a reliable leakage minimization block between the pull-up and pull-down networks to enhance power efficiency and stability[11]. The LMT regulates the leakage power by stacking two n-channel and one p-channel transistors in between the pull-up and pull-down networks and uses the input signal to control the stack. These inserted transistors create a resistive path between the power rails and mitigate the large leakage current[12]. The LMT effectively balances leakage power and propagation delay in both active and standby modes. The proposed design takes advantage of both CNTFET technology and LMT. The proposed design for the SRAM cell is simulated using the Stanford University 32nm CNTFET technology model on HSPICE tool. The various analyses are performed to evaluate the design's time response and current-voltage characteristics and compare its performance with state-of-the-art SRAM designs.

The rest of the research paper is arranged as follows: Section 2 discusses the basics of CNTFET technology. In section 3, the previous research work is listed. The proposed LMT-SRAM circuit design is introduced in section 4. The simulation results are assimilated in section 5 to make a performance comparison. Section 6 concludes the paper.

1.1 CNTFET Technology

CNTFET is considered as one of the promising new technologies. This section discusses fundamentals of CNTFET devices. The carbon atoms in the CNTs are bonded with one another using sp^2 hybridization, which leaves no bond dangling and enables the easy integration with high-K dielectric materials[5,13]. CNT is obtained from a sheet of graphite, which is rolled up and joined together along the chirality vector, (m, n). The C_h represents the circumference of the CNT[14] which is given in Eq. (1).

$$C_h = a\sqrt{\mathrm{m}^2 + n^2 + mn} \quad \ldots (1)$$

where, a=0.142nm, is interatomic distance between carbon atoms.

CNTs are classified into three types based on chirality vector, such as armchair for $(m = n)$, zigzag for $(m = 0 \; or \; n = 0)$and chiral for all other indices values. CNTs are also classified as single-wall or multi-wall depending on the number of concentric hexagonal graphene sheet rolled up to make CNT.

The electrical properties for CNTs are determined based on their diameter (D_{CNT}), and chirality. The chirality vector determines the conductivity of CNT. It is classified as metallic if $(m = n)$, and isacting as a semiconductor when $(m - n)$ results ina multiple of 3[12]. The diameter of a CNT[15] is calculated as in Eq. (2).

$$D_{CNT} = \frac{\sqrt{3}C_h}{\pi} \quad \ldots(2)$$

For a CNT with chirality (19, 0), diameteris 1.487nm, and threshold voltage is 0.293V.The threshold voltage (V_{th}) for CNTFET devices, depends on CNT's diameter[13] and is given in Eq.(3).

$$V_{TH} = \frac{E_\pi}{e.D_{CNT}} \quad \ldots (3)$$

where, E_π represents the bond energy between neighboring carbon atoms, e is the charge, and D_{CNT} is diameter.

In a CNT, electrons are confined within the graphene's atomic plane[16]. Due to this quasi-1D structure of CNT, electron motion in the nanotubes is restricted along the direction of the tube axis. Thus, the scattering of electrons is possible only in the forward or backward directions, and no wide-angles cattering is possible. The observed long elastic

scattering mean-free path is 1μm, which implies ballistic carrier transport. Semiconducting CNTs also show higher mobility of 10^3-10^4cm^2/Vs. The current carrying capacity is also higher around 10^9A/cm^2 in the case of multi-walled CNT[17]. The superior conduction characteristics along with ballistic carrier transport make CNTs a desirable substitute for nano electronics applications. The operation principle and four-terminal structure of CNTFET[18] are like the traditional MOSFET device, as shown in Fig. 1.

The cross-sectional view of a four-terminal CNTFET device shows semiconducting carbon nanotubes, acting as a conducting channel to connect the source and drain terminals. The device is controlled electrostatically via the gate. The unique quasi-1D device structure ensures efficient gate electrostatic control all over the channel region in comparison to MOSFET device[18,19].

Though CNTFETs offer superior scalability and electrical performance, the large-scale integration of CNTFETs is still not feasible due to fabrication challenges such as chirality control, purity, CNT alignment, contact resistance, and inconsistent pitch. As reported[20], ballistic transport requires precise contact engineering to minimize Schottky barriers. The difficulty of purifying and positioning CNTs uniformly for synthesizing the electronic devices using nanomaterials is emphasized[21]. CNTs always exist as mixed metallic and semiconducting CNTs, which gives rise to variability, and the CNTs' misalignment due to non-uniform pitch and variable diameter limits the circuit yield and reliability. These non-idealities lead to parasitic capacitance and hamper the speed as well as performance of the circuit[19-21]. Several experimental efforts have been made since 1998 towards manufacturable CNTFET circuits. The researcher[21] introduced techniques to purify CNTs and placement of CNTs at a certain density for both consistent and inconsistent pitch. The researchers[22] produces high yields of semiconducting single-walled CNTs with controlled diameter and chirality, specifically reducing metallic content. Several improved chemical vapor deposition techniques were used. The researcher[19] introduced compact SPICE models that include non-idealities. These developments are expected to bridge the gap between the CNTFET device theory and its physical nanoscale integration.

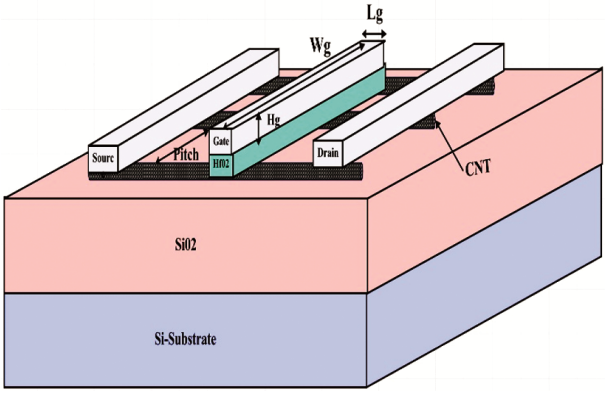

Fig. 1 — Cross-sectional View of CNTFET[17]

2 Literature Review

The authors[12] have designed a CNTFET-based six-transistor (6T) SRAM design incorporating different leakage control techniques such as sleep, zigzag, leakage feedback, sleep stack, and sleepy keeper. The different design structures were simulated using the Stanford University 32nm CNTFET technology. The sleepy keeper-based SRAM incredibly reduced power dissipation and delay by 84.26% and 38.12%, respectively[23], the author made a comparison between two SRAM circuits; one is a conventional 6T SRAM cell[24] with cross-coupled inverters, whereas the other SRAM design consists of only three-transistor (3T) cross-coupled. The designs are simulated using the Stanford 32nm CNTFET model. The 3T SRAM design has shown an improved power delay product of 86–97% when compared to the 6T CNTFET SRAM circuit and 90–99% in comparison to the 45nm MOSFET-based 6T SRAM. The researchers[25] have proposed an eight-transistor (8T) CNTFET SRAM cell. The proposed design demonstrates better SNM for write and hold operations. The suggested design utilized very little power, 50% during write and 3% during hold operation, respectively. The authors[26] have introduced SRAM design with reduced power and enhanced speed (RPES), which has very small propagation delay and leakage current. RPES made two changes: first, replaced MOSFETs with CNTFETs, and secondly, it inserted two stacked transistors between the pull-up and pull-down networks. It achieved are duction in power dissipation of 70%in comparison to conventional SRAM and 27% when compared to ternary four transistors. The authors proposed an 8T CNTFET SRAM cell, which uses two different threshold transistors and transmission gates for bitline access[27]. It consumes less power and has fast execution. It has remarkable SNM and electrical quality metrics. CNTFET-based

6T SRAM cell with a leakage control technique named input dependent (INDEP) is proposed[28]. The circuit takes advantage of both CNTFET and low-power technique called INDEP. The design shows a reduction in power consumption during hold, read, and write operations of 70.60%, 91.16%, and 62.50%, respectively. The authors have proposed an 8T SRAM cell design using CNTFETs[29]. It features a single-ended, dual-port circuit, which is suitable for low-power internet of things systems, as it displays improved read and write efficiency with the least power consumption. It offered a reduction of 41.5% in leakage power and improved SNM. In research paper[30], the high-performance, low-power eleven-transistor CNTFET SRAM design uses a traditional inverter with a cascaded CNTFET transistor and a Schmitt-based inverter with pull-up transistors. The design is simulated using 32 nm CNTFET model file from Stanford at a supply voltage of 0.9 V and room temperature conditions. The SRAM design reduces the write power consumption to 1.584 nW, the hold power consumption around 4.563 nW, and the read power around 0.00457 μW. It suits low-power applications.

3 Research Methodology

3.1 CNTFET-based LMT-SRAM Cell

SRAM holds an accountable portion of chip area, which makes it critical for system efficiency to optimize SRAM's power consumption and stability. MOSFETs being aggressively scaled down into the nanoscale regime has intensified SCEs, which leads to large leakage power interfering with stable SRAM operation. To overcome these sub-threshold challenges, CNTFETs have emerged as strong alternatives because of their superior electrostatics and scalability[31]. In this section, a CNTFET-based LMT-SRAM cell is proposed that uses a reliable circuit-level leakage minimization technique. This approach introduces one n-channel and two p-channel transistors between the pull-up and pull-down networks of the cross-coupled inverters[32]. These added transistors induce the stacking effect, which increases the resistive path between power rails. Hence, cutting off the leakage currents in both idle and active states. The inserted transistors can be controlled dynamically via input logic dependent biasing. The proposed design is expected to maintain output stability while effectively reducing standby leakage, striking a balance between power consumption and speed of operation[32].

3.1.1Reliable Leakage Minimization Technique

The leakage minimization technique is a circuit-level design approach inserted between the pull-up and pull-down networks of the logic circuit to reduce leakage current in standby and active modes. Figure 2 represents the generalized logical structure for leakage minimization technique with one n-channel transistor (MN1) and two p-channel transistors (MP1, MP2) inserted between the pull-up and pull-down networks of a standard logic cell. These extra inserted transistors exert control over the conduction path between the pull-up and pull-down networks and induce the transistor stacking effect to minimize leakage current. In this configuration, MN1 connects the output node to the pull-down network and its gate is driven by the drain of MP1. The gate of MP1 is connected to the output node, and its source is connected to the power supply (VDD). Similarly, MP2 is connected between the pull-up network and the output node, and the bias voltage Vp is applied to the gate of MP2. The value of Vp is determined by the logic path, which decides whether MP2 is connecting or isolating the pull-up network to the output node

During the circuit operation, if the input is '0', node 2 is at logic '1', so the bias voltage Vp is set to '0' to turn MP2 ON and pull the output high. This high output then turns OFFMN1 and MP1, cutting off the leakage path and maintaining a stable logic high at the output node. Conversely, for input '1', the node 2 is at logic '0', the bias voltage, Vp, is set to '1', switching MP2 OFF. The transistors, MN1 and MP1,

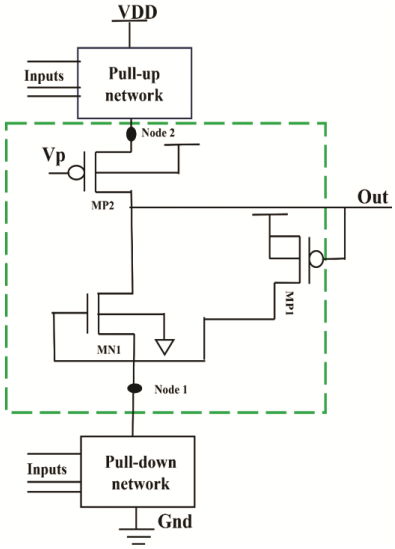

Fig. 2 — General implementation of leakage minimization technique[32]

turn ON, completing the discharge path to drive the output to logic '0'.

The key to balance leakage reduction with propagation delay is controlled by Vp. In sleep mode, Vp is held at logic '1', which blocks the leakage path by turning MP2 OFF. In active mode, Vp is set to logic '0', which allows normal logic propagation. The inserted transistor stack increases the resistance between VDD and GND in the off state to ensure substantial leakage minimization without compromising the execution speed.

3.1.2 6T SRAM Cell

The 6T SRAM cell is implemented using two cross-coupled inverters, where the output of one inverter is fed as the input to the other[33-36]. The transistor structure of 6T SRAM is shown in Fig. 3. The two inverter pairs (M1, M2) and (M3, M4) are connected to two access transistors (M5, M6), which connect the storage nodes (Q,QB) to the bitlines (BL, BLB) for read and write operations, respectively. The storage node Q holds the stored data, while QB stores its complement. The wordline (WL) is connected to the gate terminal of the M5 and M6. The drain terminals of M5 and M6 are connected to the BL and BLB. The WL controls the accessibility of the SRAM cell[37] during operation. The operation of the SRAM cell is divided into three modes, i.e., hold (idle) mode, read mode, and write mode[38,39], which are explained for understanding.

3.1.2.1 Hold Mode

When there is logic low at WL, M5 and M6 remain turned OFF, keeping BL and BLB disconnected from the cell. Hence, no read or write operation takes place, and the SRAM cell operates in hold mode, i.e. the stored value is maintained despite supply voltage[40].To understand the hold operation, consider two cases. For Q = 0, the pull-up transistor, M3 in the second inverter, connects to VDD, and QB stores a value of '1'. For QB = 1, the pull-down transistor, M2, in the first inverter connects to ground, maintaining Q = 0. Conversely, when Q = 1, the pull-down transistor, M4, in the second inverter turns ON and discharges QB = 0. Simultaneously, for QB= 0, the pull-up transistor, M1, in the first inverter turns ON, which connects the output to VDD and maintains Q = 1.

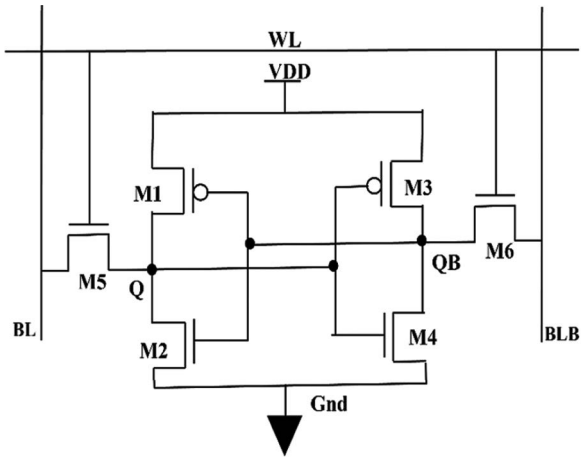

Fig. 3 — A schematic for 6T SRAM cell

3.1.2.2 Read Mode

For read operation, bitlines are pre-charged to a high logic level. When WL is asserted high, M5 and M6 turn ON, establishing a conductive path between the bitlines and the internal storage nodes via two access transistors. The stored data at Q and QB determines which bit line discharges slightly through the corresponding pull-down transistors.

For Q = 1 and QB = 0, the bit line BL remains high, while BLB discharges through transistors M6 and M4. Similarly, when Q = 0 and QB= 1, BL discharges via M5 and M2 and maintains BLB as high. This creates a small potential difference between BL and BLB, which determines the stored value. A sense amplifier is used to interpret the arising small potential difference between the two-bit lines. If voltage at BL > voltage at BLB, the stored value at node Q is 1, otherwise 0[28,35]. The read operation circuit for SRAM cell is shown in Fig. 4.

3.1.2.3 Write Mode

During the write operation, the stored values at storage nodes Q and QB are updated by charging the bit lines to desired logic levels through access transistors[28,35]. In the case of a write operation, WL is asserted logic high, which turns ON the M5 and M6, which ties the bit lines to the storage nodes Q and QB. To write logic '1', BL is charged to VDD, while BLB is discharged to '0'. The stored data is overwritten with the stronger drive current from the bit lines. When BL is charged to VDD, node Q is pulled up through M5. Simultaneously, BLB ='0'pulls down node QB through M6, storing logic '0'. Subsequently, to write '0', logic low on BL pulls down storage node Q to '0' through transistor M5, and a logic high on BLB pulls the storage node QB to '1' through transistor M6. The overwritten value is being held via cross-coupled inverter until the next transition. Figure 5 represents the SRAM circuit when in write mode

3.1.3 Proposed LMT-SRAM Design

The drain terminals of the access transistors are connected to bitlines, their gate terminals are tied to the wordline, and the source terminal is connected to the storage nodes Q and QB, respectively[28]. The extra inserted transistors form a regulated stack configuration that obstructs the static current flow between the pull-up and pull-down networks of the inverter circuit. As it is represented in Fig. 6, the circuit consists of two cross-coupled inverters. Inverter 1 and inverter 2 represented by the CNTFET pairs (X1, X2) and (X3, X4), respectively[32]. Between these two inverters, additional transistors are introduced as (XN1, XP1, XP2) and (XN2, XP3, XP4), respectively, to control the leakage between pull-up and pull-down networks.

The control input, Vp, applied to the gates of XP2 and XP4, plays a critical role in determining whether the transistor stack is switched ON or OFF, and this way, the leakage path is effectively isolated during the standby condition.

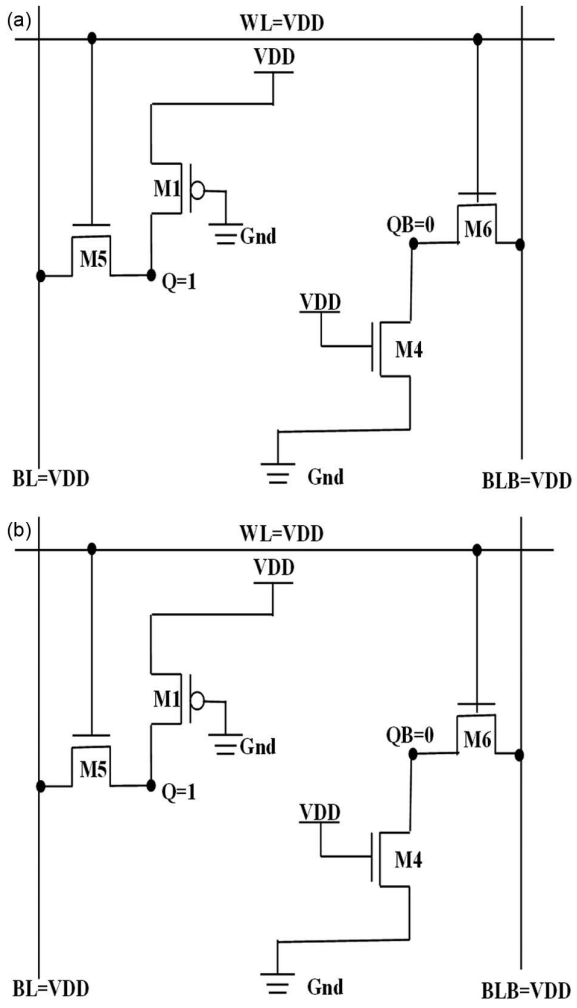

Fig. 4 — SRAM schematic during (a) read ‘0’; and (b) read ‘1

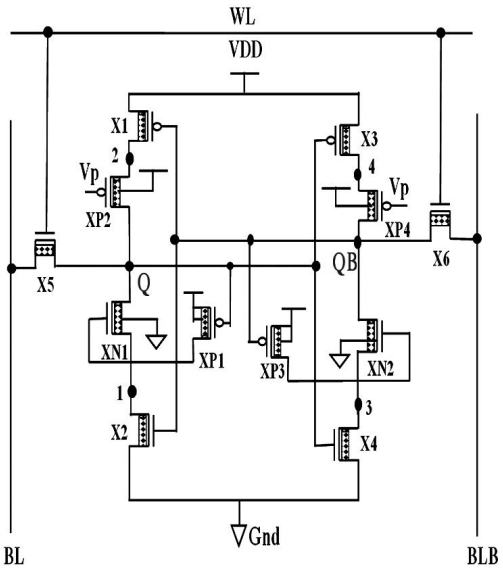

Fig. 6 — Proposed CNTFET-based LMT-SRAM cell

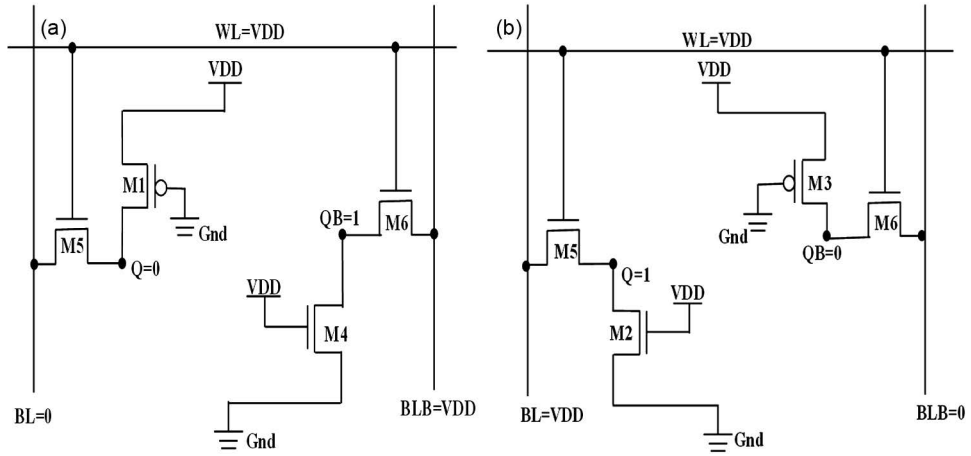

Fig.5 — SRAM schematic during (a) write ‘0’; and (b)write ‘1’

To understand the working operation, consider the case when Vin= '0', which turns ON transistor X1 and logic '1' at node 2, which sets Vp to logic '0' and transistor XP2 is turned ON, thereby connecting VDD to node Q. When Vin='1', X1 turns OFF and X2 turns ON. Consequently, node 2 acquires logic '0', which sets Vp to logic '1', switching XP2 OFF, while XP1 and XN1 provide a discharge path for the output.

The WL, when asserted high logic, activates X5 and X6 to perform read and write operations. During the write mode, the bitlines act as inputs that charge or discharge the storage nodes to store the desired logic values in the SRAM cell. During the read mode, the bitlines function as the outputs, transferring the stored information as a potential difference to the sense amplifier, which detects the output logic level. The data is being held in the SRAM cell if power is supplied.

For performing the read and write operations, WL must be asserted high to turn ON the access transistors X5 and X6, which connect the storage nodes Q and QB to the BL and BLB, respectively. To understand the read operation, consider the case where storage nodes Q = 0 and QB = 1. When QB = 1, the input to inverter 1 becomes Vin = 1, which switches transistor X1 OFF and transistor X2 ON. For logic '0' at node 2, control input Vp attains high logic, which keeps XP1 OFF. As a result, the storage node Q retains the value '0', which activates XP2. The ON state of XP2 pulls the XN1 high, forming a conduction path that discharges BL down to logic '0' through the series chain of conducting transistors X5 → XP2 → XN1 → X2 → Gnd.

Meanwhile, the other bitline, BLB, is charged high through access transistor X6, which connects QB to VDD through XP3 and X3. The sense amplifier detects the voltage difference between BL and BLB. Since the voltage level of BL is less than BLB, the stored value is read as logic '0', and likewise, when the voltage level is BL>BLB, the stored value is read as logic '1'. During the write operation, the WL is enabled, which turns ON the access transistors X5 and X6 ,while the bitlines BL and BLB are driven with new data to overwrite the stored value in the cross-coupled inverters. At this stage, the bit-lines, BL and BLB, are charged with the new data.

The charged bitlines overpower the stored data in cross-coupled inverters and update the storage nodes Q and QB. For writing '1' at node Q, BL is charged to VDD and BLB is driven to logic '0'. The high logic on BL turns ON access transistor X5, charging the storage node Q to '1'. As Q = 1, the complementary node QB attains logic '0' through the inverter feedback action. The low logic at QB = 0 will activate XP1 and X1, which together maintains Q = '1' by forming a conduction path from VDD to node Q through X1 and XP2.

For writing '0' at node Q, BL is driven to logic '0' and BLB is charged to VDD. The low voltage on BL pulls down storage node Q to '0' through access transistor X5. Consequently, QB is set high. When QB = 1, transistor X2, turns ON and Q = 0 activates XP1 enabling XN1, and forming a strong discharge path from Q to GND through XN1 and X2. This mechanism allows the proposed structure to performa write operation while simultaneously minimizing leakage current. The inserted leakage control transistors effectively achieve a balance between propagation delay and power consumption during both active and standby modes.

The LMT design introduces three extra transistors in an inverter, which doubles the total transistor count compared to6T SRAM cell. The area per CNTFET can be computed as Eq. (4).

$$Area = L_{ch} * (N * Pitch) \quad \ldots (4)$$

where, L_{ch} is the channel length, N is the number of CNTs, and Pitch is the spacing between two CNTs[16]. The total circuit area for the CNTFET-based circuit is given as the product of the number of CNTFETs used and the individual CNTFET area. The calculated area for CNTFET-based 6T SRAM is 0.112 μm^2, and for the proposed LMT-SRAM, it is 0.153 μm^2. This corresponds to an area overhead of 36.6%, which is quite moderate for a leakage optimized memory circuit. As far as layout is concerned, source and drain regions are shared to accommodate the extra devices within the same diffusion rows[13], which avoids additional routing tracks and limits the layout overhead to 30%.

4 Results and Discussion

The proposed CNTFET-based LMT-SRAM design is simulated to verify its functionality and evaluate the performance metrics for comparison with existing SRAM architectures. The design is simulated at room temperature with VDD= 0.9V and at room temperature conditions. The 32 nm Stanford University CNTFET Model technology file is used to

perform simulations with HSPICE tool[41]. The various CNTFET parameters being used while simulating is enlisted in Table 1.

The Stanford 32 nm CNTFET model is a widely used, physics-based compact model available for circuit-level simulations of CNTFETs. It is the first complete, circuit-compatible model that covers all major non-idealities relevant to real-time CNTFET performance analysis. It tackles almost all major non-idealities, such as elastic scattering in the channel, resistive source/drain regions, Schottky-barrier resistance, and parasitic gate capacitances and is the only model to support multiple CNTs per device. The model enables the HSPICE simulation of digital CNTFET-based circuits[19].

The proposed CNTFET-based SRAM with leakage minimization technique is evaluated for hold power, read power, and write power, as well as read delay and write delay. The design is also evaluated for SNM to determine its stability using both butterfly and N-curve methods. To further assess the design's reliability, MC simulations are performed considering the PVT variations. The CNTFETs used in the proposed design have a chirality vector of (19, 0) for CNTFETs, which ensures the constant threshold voltage throughout the SRAM circuit.

The higher number of tubes signifies higher drive strength and a larger area[42-44]. The transient analysis simulation waveform for the proposed CNTFET-based LMT-SRAM cell is shown in Fig. 7. The write and read operations waveforms for the proposed LMT-SRAM cell are shown explicitly in Figs 8-9, respectively.

The write '0' operation is shown in Fig. 8 (a) for writing '0'. The BL is driven to logic low, whereas BLB is driven to logic high, which updates Q as '0' and QB as '1'. The write '1' operation is shown in Fig. 8 (b), which is obtained by reversing the bitline values. Figure 9 (a) shows the read '0' operation. For obtaining the read '0' operation simulation,

Table1 — Design parameters for CNTFET[41]

Parameter	Parameter description	Value
L_{ch}	Channel length	32nm
$L_{S/D}$	Source/Drain length	32nm
L_{geff}	The mean free path in the intrinsic CNT	100nm
E_{fo}	Fermi level	0.6eV
T_{ox}	Oxide thickness	4nm
K_{ox}	Dielectric material for top gate	16
(m, n)	CNTs chirality vector	(19, 0)
V_{DD}	Supply voltage	0.9V
V_{th}	Threshold voltage	0.289V
Temp	Temperature	27° C
Tube	Number of CNTs	1 to 3
Pitch	Inter-tube distance between CNTs	20nm
V_{fn} and V_{fp}	n-channel& p-channel CNTFET flat-band voltage	0.15V & -0.15V

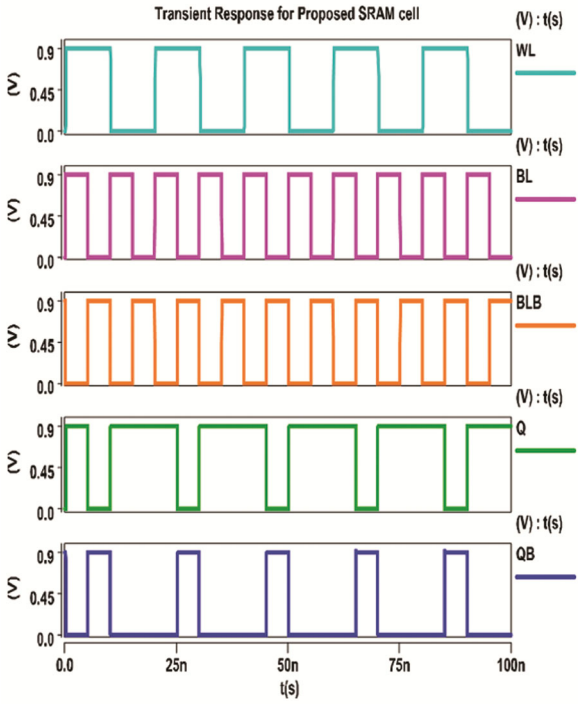

Fig. 7 — Simulation waveform for proposed LMT-SRAM cell

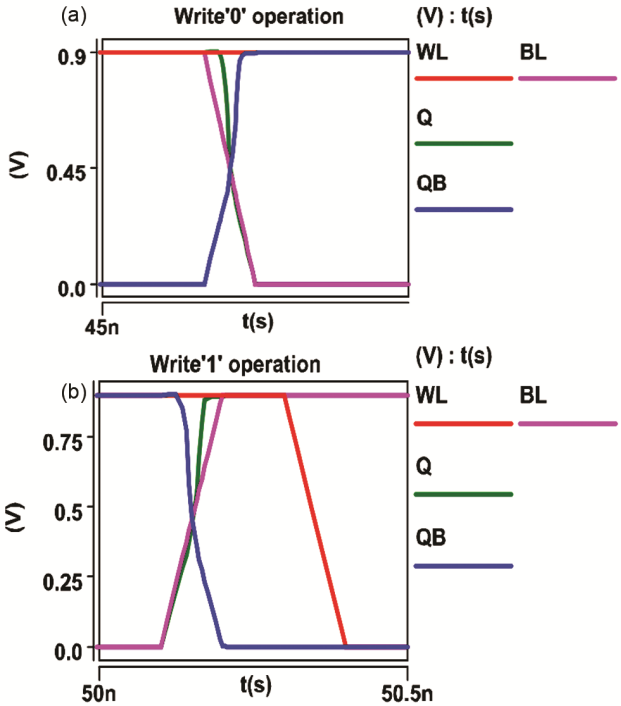

Fig. 8 — CNTFET-based SRAM (a) write '0'; and (b) write '1'

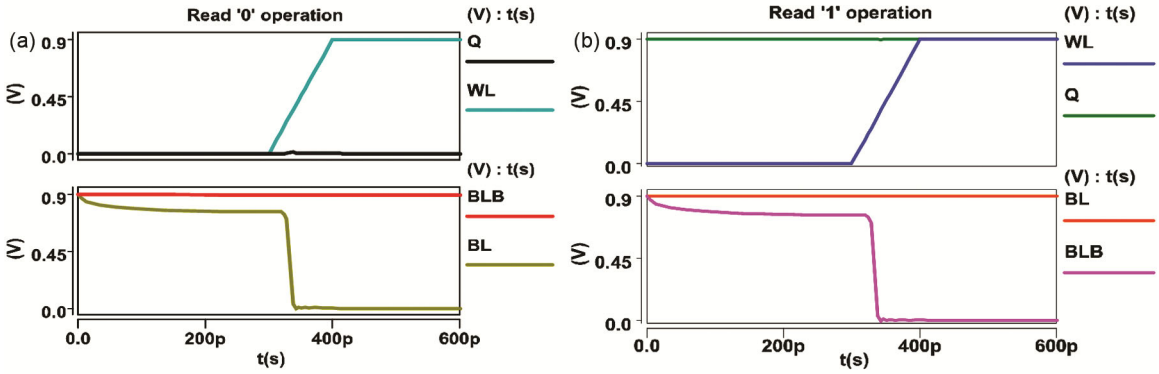

Fig. 9 — CNTFET-based SRAM (a) read '0' (b) read '1'

Table 2 — Performance metrics comparison for SRAM cell

Performance parameter	6T	10T [28]	11T [30]	9T [42]	11T [43]	7T [44]	LMT-SRAM
Hold power (uw)	18	5.35	4.56	1.08	0.052	8.64	0.049
Write power (nw)	0.4	0.15	1.58	12.45	29.59	0.20	0.027
Read power (uw)	12	1.07	4.57	9.53	0.053	9.23	0.059
Write delay (ns)	0.002	0.0265	0.272	0.167	0.188	0.0297	0.0228
Read delay (ns)	0.003	0.0234	0.045	0.65	0.336	0.0462	0.0299
Write energy (zJ)	0.9	4.05	431.83	2080	9974	5.94	0.616
Read energy (aJ)	28	25	206	6194	17.80	426	17.641

bitlines (BL and BLB) are charged to VDD. With the assertion of logic high at WL, the BL's potential starts to discharge, reading the node Q as '0'. Likewise, reading '1' is performed as BLB discharging to '0' as in Fig. 9 (b). The different performance metrics for the proposed design are evaluated when a transient analysis is performed. The simulation results for evaluated performance metrics are compared in Table 2 with existing SRAM designs. The designs considered for comparison are also evaluated under the same parameters of CNTFETs[42,43].

The obtained results on comparison with existing designs clearly demonstrate the effectiveness of the incorporated leakage minimization technique in the proposed SRAM design. Table 2 depicts the comparison results for the SRAM cell design. Compared with the 11T SRAM reported[30], the proposed LMT-SRAM design achieves remarkable reduction across power, delay, and energy metrics. The reduction in hold power is a98.9% when compared to the design proposed[30], which suggests a very good power saving while in standby mode. During active mode, write power is showing an improvement of 98.3%, and read power is improved by 98.7%, when compared to the design in paper[30]. During active mode, the proposed SRAM is 91.6% faster during write and 33.6% faster while read operation. The energy consumption due to the leakage minimization technique and the use of CNTFETs has shown a reduction of 99.86% when in write mode and a 99.14% reduction while in read mode.

4.1 Stability & Variability Analysis

Stability is another important criterion to determine the efficiency and reliability of SRAM cell. To determine stability, SNM is analyzed[45,46]. SNM represents the maximum DC noise voltage that the SRAM cell can tolerate so that it does not lose the stored data or reverse its state. SNM is more significant during hold and read operations, as the cell become more susceptible to disturbances caused by supply voltage fluctuations, process variation, and the external noise[47].

A higher SNM value indicates better stability and reliable operation under varying operating conditions[48]. The common method to determine SNM is the butterfly curve, which is obtained by plotting the voltage transfer characteristics (VTC) of two cross-coupled inverters forming the SRAM cell. Then the largest possible square is fitted inside the lobes of the butterfly curve, and the side length of the largest possible fitted square is the SNM value. In the case of SRAM, SNM is evaluated in three working modes, i.e., hold SNM (HSNM), read SNM (RSNM), and

write SNM (WSNM)[49]. Figure 10 shows the butterfly curve for different operating modes. The higher SNM value for determining superior stability. For calculating HSNM, WL is grounded, and BL and BLB are pre-charged to VDD. Then VTCs of both inverters are stacked, and a largest square is fitted inside the lobes to estimate the SNM equal to the fitted square side length. It is a graphical method of determining the SNM. Likewise, SRAM is operated in read and write modes to obtain the corresponding VTCs to determine RSNM and WSNM graphically[50].The SNM comparison of the proposed SRAM cell with other existing SRAM cells using leakage control techniques is compiled in Table 3. From the compiled Table 3 results, it is assessed that the proposed SRAM cell has shown a significant improvement over the conventional 6TSRAM design and other cited SRAM designs. The HSNM has improved by 43.4% compared to conventional 6T SRAM.

4.2 N-Curve Method

In addition to the conventional butterfly curve method, N-curve method offers a quantitative technique for evaluating the stability characteristics of SRAM cell[51]. N-curve method incorporates both voltage and current parameters, which enables simultaneous assessment of read and write stability[52]. The N-curve technique being able to capture current-based noise margins and help assess stability under process variations[53]. For obtaining N-curve, the SRAM circuit is simulated in the read mode by connecting word line and both bitlines to VDD. The circuit simulated for obtain N-curve is shown in

Table 3 — Simulation comparison for SRAM cells with leakage control circuits for SNM

Design	HSNM	RSNM	WSNM
6T SRAM	235	101	536
Sleep[16]	314	101	378
Sleep with header switch[16]	321	127	391
Sleep with footer switch[16]	320	112	392
Zigzag[16]	322	119	398
Stack[16]	321	100	404
Sleep stack[16]	325	118	402
INDEP[33]	285	201	638
Gating technique[38]	325	145	185
Proposed	337	242	830

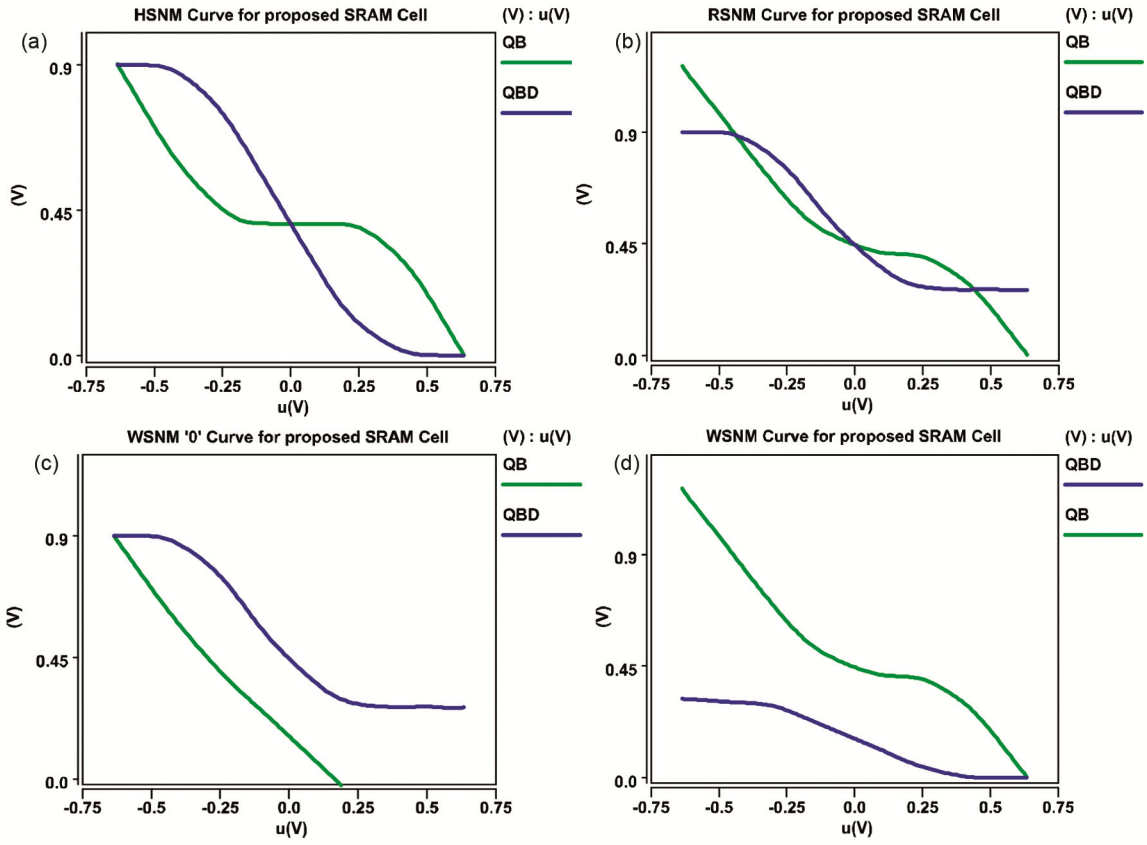

Fig. 10 — Butterfly curve for proposed LMT-SRAM cell (a) HSNM (b) RSNM (c) WSNM ‘0’ (d) WSNM ‘1’

Fig. 11 (a). The voltage sweep is provided at any of the storage node and then the sweep current from the voltage source is plotted to obtain N-curve[52]. The N-curve parameters include static voltage noise margin (SVNM), static current noise margin (SINM), write trip voltage (WTV), and write current noise margin (WINM)[52]. These parameters are annotated in Fig. 11 (b). The SRAM is said to be stable if it has higher SVNM and SINM values, whereas WTV and WINM indicate ease of writing. Lower value indicates enhanced write ability[52]. In Fig. 11 (c), a graphical comparison of obtained N-curve for proposed SRAM cell, 6T SRAM cell, and a simple CNTFET-based 6T SRAM cell is made.

The proposed SRAM cell circuit configuration for N-curve extraction was simulated under varying cell ratio (CR), pull-up ratio (PR), VDD, temperature, and chirality vector to assess the effect of PVT across SRAM stability[53]. The simulation waveforms for N-curve variations are depicted in Fig. 12, and the

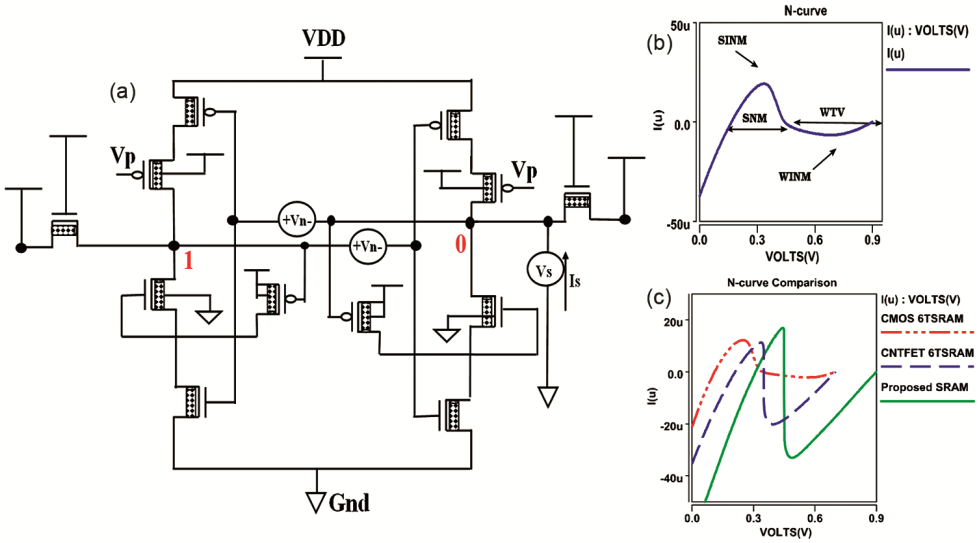

Fig. 11 — N-curve (a) circuit arrangement for measuring N-curve[52] (b) sample N-curve[51](c) N-curve comparison

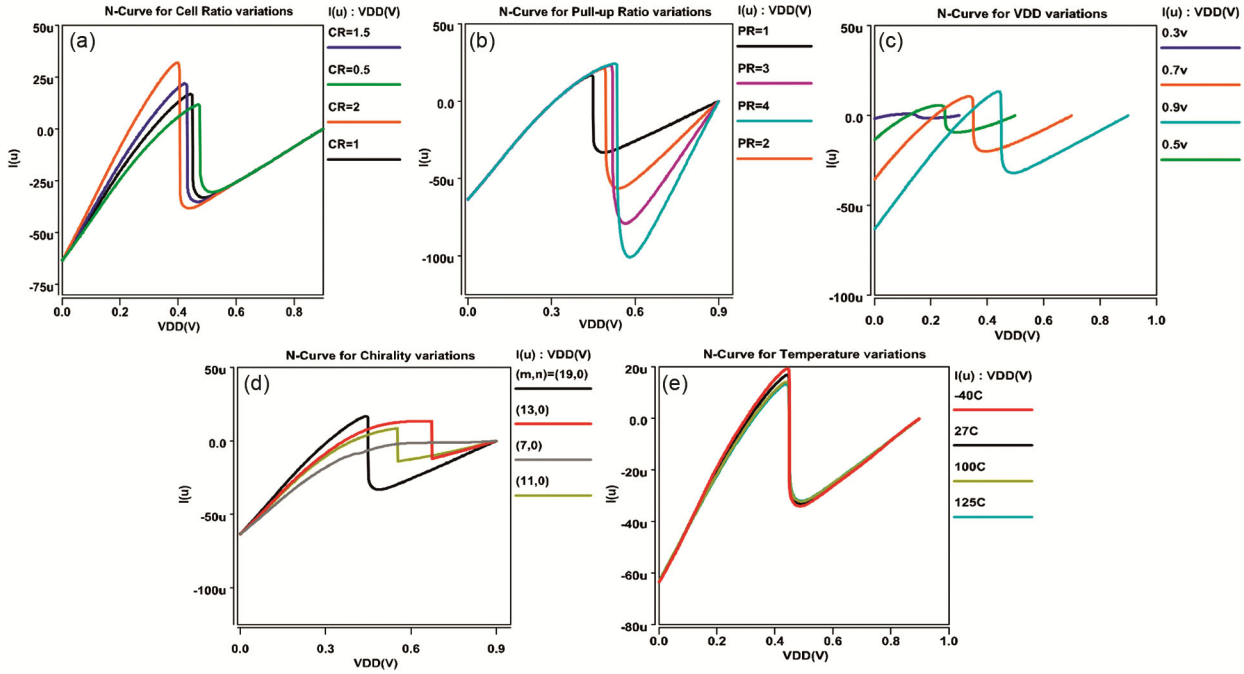

Fig. 12— N-curve variability analysis for proposed SRAM cell design (a) CR (b) PR (c) VDD scaling (d) temperature; and (e) chiralityvector

corresponding results are summarized in Table 4. The CR (Wn/Wa) is defined as the ratio between the width of n-channel pull-down transistors in the cross-coupled inverters (Wn) to the width of n-channel access transistors (Wa). The CR has a direct impact on the read stability of the SRAM cell. A higher CR indicates a stronger pull-down network, which indicates higher stability for logic '0' as SNM and SINM rise. The different CRs used for variations are 0.5, 1, 1.5, and 2. Figure 12 (a) demonstrates the effect of CR variations on the N-curve. The N-curve shows a rise in WTV and WINM, which implies that a higher current is required to alter the stored data. This implies read stability improves while write ability becomes more difficult[52-54]. The PR is defined as the ratio of pull-up transistor width to the pull-down transistor's width, i.e., (Wp/Wn). The PR values used for variations are 1, 2, 3, and 4. Higher PR means a stronger p-channel network, which results in an increased cell's ability to retain logic '1' even under higher noise or voltage fluctuations.

The higher PR implies the struggle to write '0' or tossing the high state of cell because the strong pull-up network resists being over powered by the access path[53]. It can be seen in Fig. 12 (b). The write current noise margin is increasing with increased PR, which implies that a larger current is required to flip the cell's state. The results summarized in Table 4 show an increased SNM with higher PR.

The supply voltage affects all the margins of N-curve[54]. The supply voltage scaling is required to minimize the power consumption in digital circuits. Therefore, it is important for the SRAM circuit to be variability tolerant. Lower VDD compresses SNM/SINM, reducing read margin and making read disturb, while higher VDD increases WINM, which impacts write operation. Figure 12 (c) shows the effect of power supply voltage scaling on the N-curve behaviour. The different supply voltages considered for variability analysis are 0.3V, 0.5V, 0.7V, and 0.9V. The N-curve for VDD variations in Fig. 12 (c) demonstrates that as the supply voltage increases, the magnitude of the WINM also increases, which signifies improved read stability due to a stronger pull-down network and higher current required to flip the stored bit.

Figure 12 (d) illustrates the effect of temperature variations from -40°C to 125°C. The rising temperature leads to a slight decrease in peak current, SINM decreases, and the overall curve shifts slightly towards lower current levels[53]. The minimal variations observed across temperature ranges demonstrate that the proposed SRAM cell maintains robust operation and reliable noise margins under extreme thermal conditions. The effect of chirality variation on the N-curve characteristics of proposed SRAM is significant[54]. Higher chirality values, such as (19,0) and (16,0), effectively enlarge the CNT diameter and reduce threshold voltage, which causes higher peak currents. This behaviour indicates stronger read stability and better SNM[53,54]. The results obtained from varying these PVT parameters are summarized in Table 4. The compiled results confirm the proposed design's robustness, and stability under diverse PVT conditions, which validates its suitability for reliable nanoscale memory applications.

Table 4 − PVT parameter variation on N-curve metrics

Metric			CR	
	0.5	1	1.5	2
SNM (mV)	246	283	286	292
SINM (uA)	11.65	16.52	21.78	31.9
WTV (mv)	224	255	267	289
WINM (uA)	-29.4	-33.07	-35.11	-38.17
			PR	
	1	2	3	4
SNM (mV)	283	426	492	498
SINM (uA)	16.52	21.2	23.07	23.93
WTV (mv)	255	212	192	174
WINM (uA)	-33.07	-56.32	-78.97	-100.27
			VDD	
	0.3V	0.5V	0.7V	0.9V
SNM (mV)	160	221	256	283
SINM (uA)	0.87	5.639	10.62	16.52
WTV (mv)	85.7	172	231	255
WINM (uA)	-1.49	-9.11	-19.95	-33.07
			Temp	
	-40°C	27°C	100°C	125°C
SNM (mV)	271	283	269	279
SINM (uA)	19.34	16.52	14.17	13.24
WTV (mv)	250	255	257	259
WINM (uA)	-34.00	-33.07	-31.44	-32.05
			Chirality	
	(19,0)	(13,0)	(11,0)	
SNM (mV)	283	371	239	
SINM (uA)	16.52	13.48	8.54	
WTV (mv)	255	223	202	
WINM (uA)	-33.07	-11.39	-13.26	

4.3 MC Analysis under PVT variation for SNM

The proposed SRAM design exhibits superior SNM in all three operating modes when compared to

existing SRAM designs. SNM is a critical indicator of a cell's stability and reliability under device mismatch conditions. To analyze and estimate the impact of PVT variations on the proposed SRAM design, MC analysis with 1000 simulation[55] runs was performed. For performing statistical analysis, key parameters such as VDD, temperature, and process parameters, i.e., n-channel CNTFET flat-band voltage (Vfn) and p-channel CNTFET flat-band voltage (Vfp), are varied for 1000 sample runs[56,57]. The VDD followed a Gaussian distribution centered at 0.9V with a 0.07V deviation, temperature is varied around 27°C$\pm$ 2.7°C. The flat-band voltages are randomly chosen within 0.1-0.2V with a deviation of $\pm$10% to emulate threshold voltage variations due to process parameter[58]. The results are summarized in Table 5.

MC simulations are executed in HSPICE tool and SNM values are extracted from the resulting. Csv files using the MATLAB software. Statistical metrics such as mean (μ) and standard deviation (σ) are used to quantify stability during variations. Also, the K-S normality test[59] is performed to determine whether the SNM datasets follow a normal distribution for p-values greater than 0.4. Figures 13-15, show the MC simulations for variability analysis for the HSNM, RSNM, and WSNM parameters.

For HSNM, the mean value (337-338mV) remained nearly constant across all the PVT corners, with the higher deviation observed only under VDD variations, σ=4.7mV, which indicates that VDD fluctuations most strongly influence hold stability. The standard deviation for HSNM under temperature is σ=0.21mV, and for process variation, it is σ=0.75mV. These minimal standard deviation values indicate higher robustness, and reliability during the hold mode.

Table 5 — Summarized statistical results obtained from MC simulations run

SNM	VDD			Temperature			Vfn and Vfp		
	μ	σ	p-value	μ	σ	p-value	μ	σ	p-value
HSNM (mV)	337	4.7	0.50	338	0.21	0.44	338	0.75	0.40
RSNM (mV)	242	29.9	0.79	241	0.13	0.51	242	2.78	0.91
WSNM(mV)	830	12.1	0.83	831	0.09	0.52	830	3.39	0.50

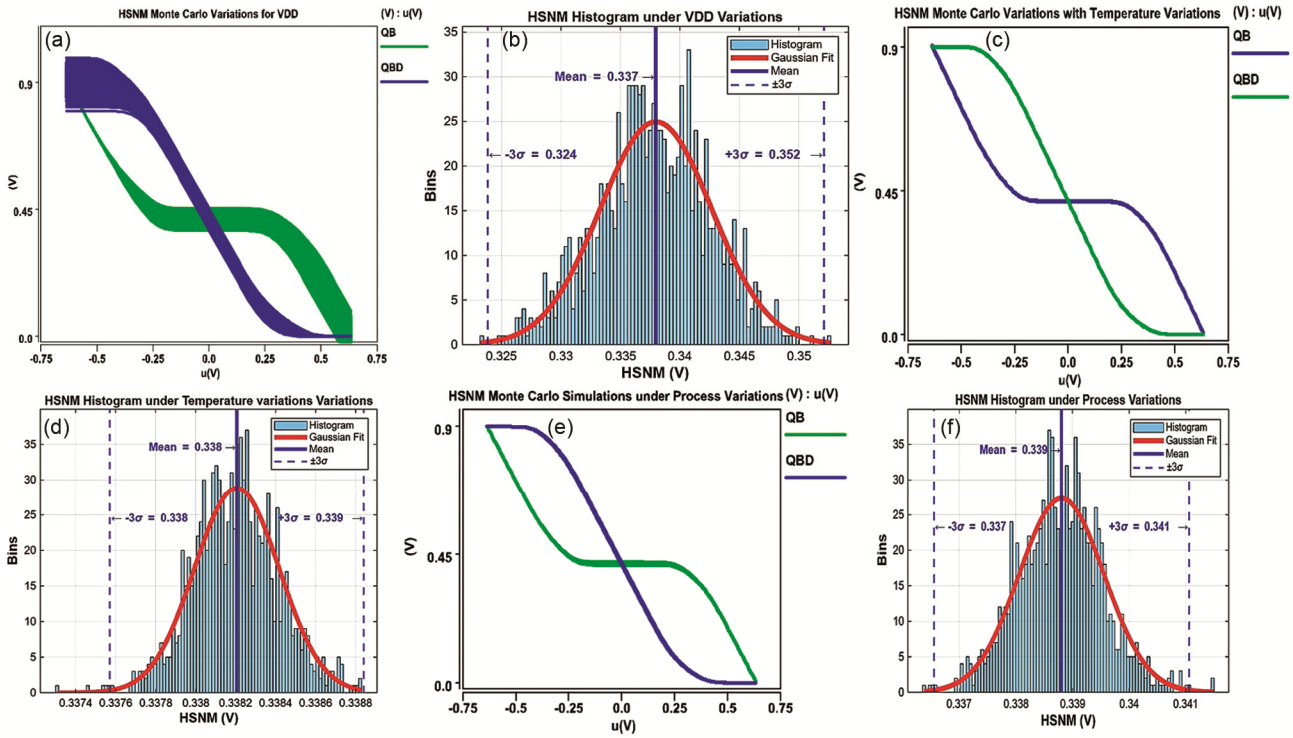

Fig. 13 — HSNM MC simulation for variability analysis of proposed SRAM cell design (a) HSNM butterfly curve with voltage variations (b) histogram HSNM voltage variations (c) HSNM butterfly curve with temperature variation (d) histogram HSNM temperature variation (e) HSNM butterfly curve with process parameters variations; and (f) histogram HSNM process parameters variations

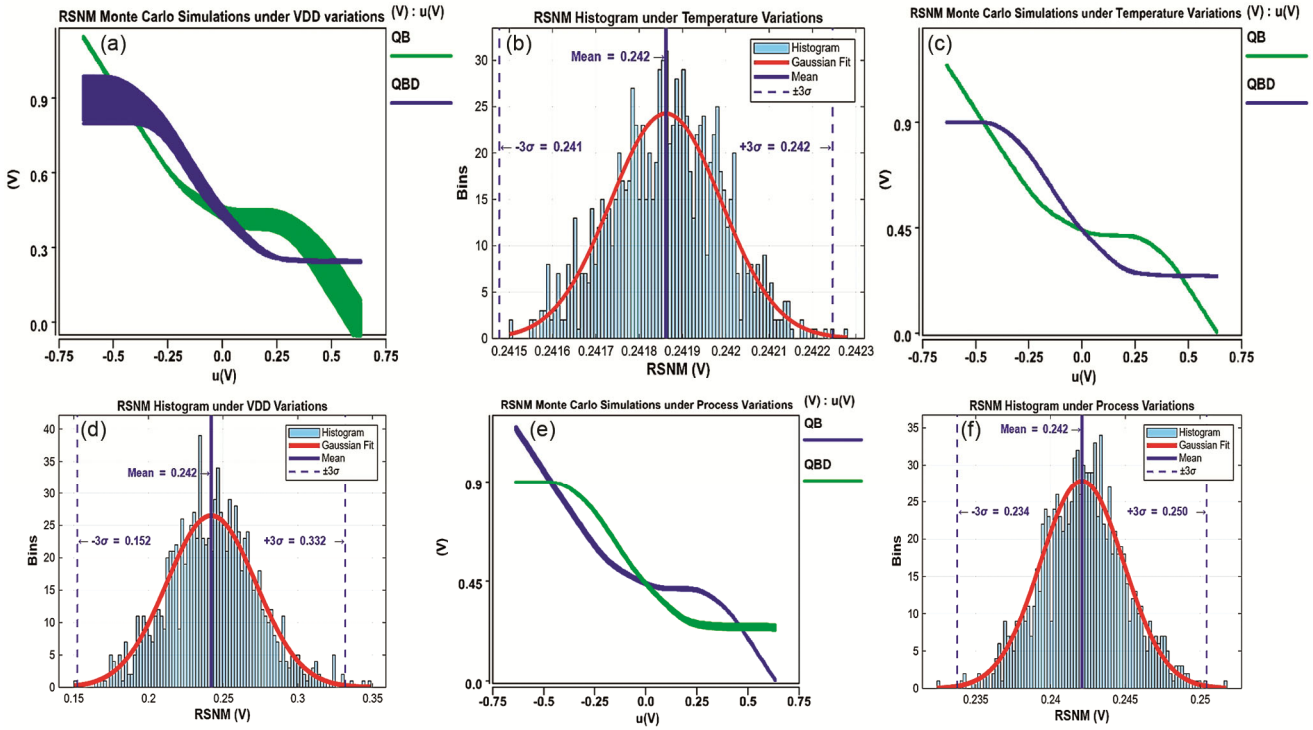

Fig. 14 — RSNM MC simulation for variability analysis of proposed SRAM cell design (a) RSNM butterfly curve with voltage variations (b) histogram RSNM voltage variations (c) RSNM butterfly curve with temperature variation (d) histogram RSNM temperature variation (e) RSNM butterfly curve with process parameters variations; and (f) histogram RSNM process parameters variations

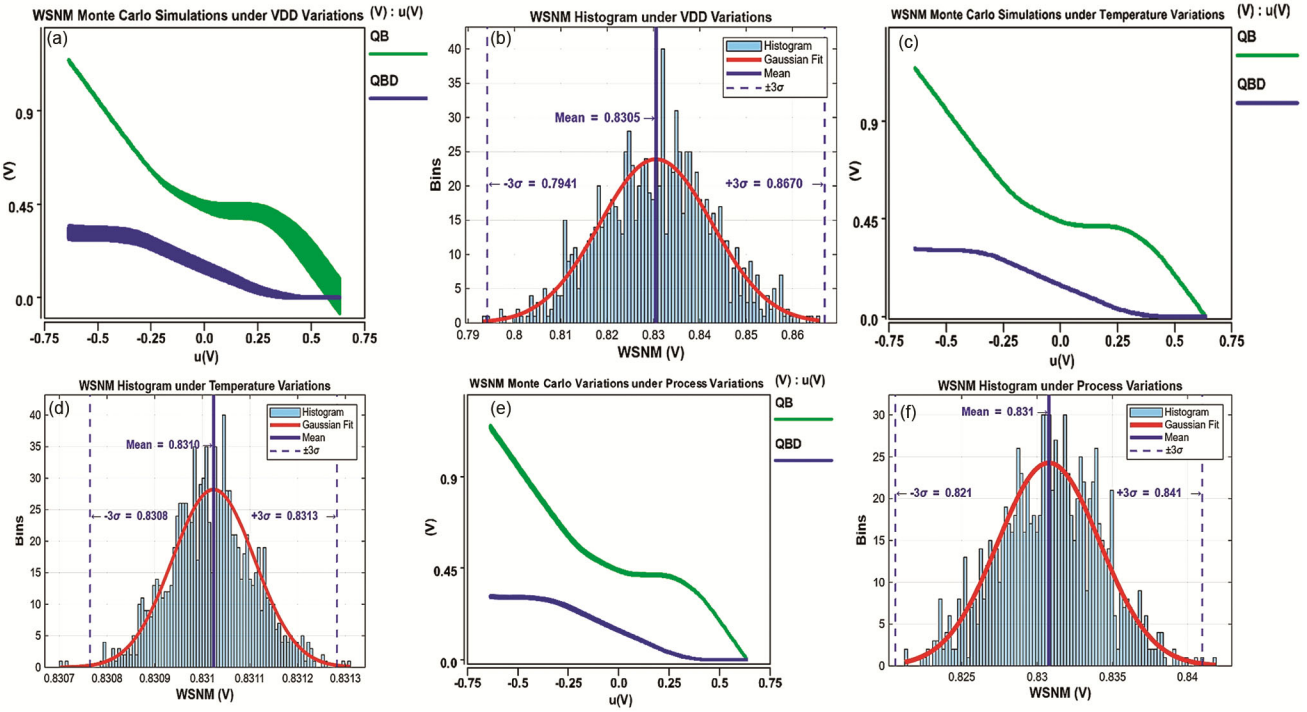

Fig. 15 —WSNM MC simulation for variability analysis of proposed SRAM cell design (a) WSNM butterfly curve with voltage variations (b) histogram WSNM voltage variations (c) WSNM butterfly curve with temperature variation (d) histogram HSNM temperature variation (e) WSNM butterfly curve with process parameters variations; and (f) histogram WSNM process parameters variations

Table 6 — Best-case and worst-case values

SNM	VDD		Temperature		Vfn&Vfp	
	(μ+3σ)	(μ-3σ)	(μ+3σ)	(μ-3σ)	(μ+3σ)	(μ-3σ)
HSNM (mV)	352	323	338.8	337.5	341	336
RSNM (mV)	332	152	242.2	241.8	250	233
WSNM (mV)	866.6	794.1	831	830	840	820.5

RSNM exhibited higher sensitivity to process fluctuations, as it shows a standard deviation of σ=29.9mV, whereas it remains almost unaffected by temperature variations for σ=0.13mV. WSNM demonstrated excellent stability across all PVT corners with a mean value approximately between 830-831mV and the highest standard deviation of 12.1mV for supply voltage variations and superior write operation under temperature and process changes.

The best-case and worst-case SNM limits (μ±3 σ) are summarized in Table 6. In case of HSNM, the best-case value is 352mV and the worst-case value dropped to 323mV. For RSNM, the best-case and worst-case values span from 332mV to 152mV. The WSNM values varied between 866.6mV and 794.1mV across corners. The smaller deviations range for WSNM shows the SRAM cell's strong immunity to PVT variations[60]. The proposed SRAM cell exhibits excellent tolerance to temperature and threshold variations (process variations), whereas the supply voltage is showing the dominance in affecting the SRAM's stability. The WSNM being the most stable metric under heavy variations, showcasing robust and reliable performance of the proposed SRAM.

5Conclusion

This research work presents a CNTFET-based SRAM cell using leakage minimization technique to enhance stability and minimize power dissipation. The design is simulated using the Stanford 32 nm CNTFET model in HSPICE, and its functionality was validated across hold, read, and write operations. The SNM was analyzed using both butterfly and N-curve methods to assess stability under various operating conditions. The PVT variations are evaluated through extensive MC simulations with 1000 runs. The statistical analysis of HSNM, RSNM, and WSNM, indicated near constant mean values and minimal standard deviations, confirming strong robustness and variation tolerance. The proposed LMT-SRAM demonstrates high read/write stability, reduced power dissipation, and reliable operation under nanoscale variability, making it highly suitable for next-generation low-power memory applications.

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