Indian Journal of Pure & Applied Physics
Vol. 64, April 2026, pp. 377-397
DOI: 10.56042/ijpap.v64i4.20713

RSOA-Based Reversible Logic Design: A Scalable Approach for Optical Gates and Multiplexers Using FRG Architecture

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Received: 16th June 2025; accepted: 10th February 2026

In this study, the design of fundamental all-optical logic circuits using reversible Fredkin gate architectures implemented with Reflective Semiconductor Optical Amplifiers (RSOAs) is proposed and investigated. A 2×1 multiplexer (MUX) forms the foundational element, from which key logic operations NOT, AND, OR, NAND, NOR, XOR and XNOR are derived. Additionally, a 4×1 MUX, half-adder and a half-subtractor circuits are constructed to demonstrate the scalability of the approach for complex combinational logic. All designs operate using Gaussian pulse inputs, and the switching dynamics of the RSOA-based circuits are analysed in detail. To evaluate the optical signal quality and performance, critical metrics including the Extinction Ratio (ER), Contrast Ratio (CR), and Relative eye opening (REOP) are calculated. The results confirm that the proposed circuits offer high-speed operation, low energy consumption, and excellent signal integrity, highlighting their potential for application in integrated photonic logic, Fiber-optic communication systems, and next-generation optical computing architectures.

Keywords: RSOA (reflective semiconductor optical amplifier), FRG (fredkin reversible gate), XGM (cross-gain modulation), Optical logic gates, Photonic multiplexer, Extinction ratio (ER)

1 Introduction

The ever-increasing demand for ultrafast, high-bandwidth, and energy-efficient information processing has motivated extensive research into photonic computing, where optical signals are exploited to perform logic and arithmetic operations directly in the optical domain. Compared to electronic counterparts, photonic systems offer inherent advantages such as large bandwidth, low latency, immunity to electromagnetic interference, and reduced heat dissipation. Consequently, all-optical logic gates and multiplexing structures have emerged as fundamental building blocks for next-generation optical communication systems and photonic integrated circuits (PICs)[1–3].

Over the past decade, a wide variety of conventional (irreversible) all-optical logic gates and multiplexers have been demonstrated using different photonic platforms, including Mach–Zehnder interferometers (MZI) micro-ring resonators (MRRs), photonic crystal structures, plasmonic waveguides, and semiconductor optical amplifier (SOA)-based switches[4–10]. While these approaches successfully realize high-speed optical logic functions, they suffer from notable limitations such as high input power requirements, complex fabrication processes, thermal sensitivity, limited scalability, and most importantly irreversible logic operation, which inherently leads to information loss and energy dissipation.

According to Landauer's principle, every irreversible bit operation dissipates a minimum amount of energy due to information erasure, which becomes a critical bottleneck as data rates and circuit densities continue to scale. To address this challenge, reversible logic computing has gained significant attention, as it preserves information by establishing a one-to-one mapping between input and output states, theoretically enabling computation with near-zero energy dissipation[11-12]. Reversible logic gates such as the Feynman, Fredkin, Toffoli, and Peres gates form the foundation of energy-efficient computing paradigms and have found applications in quantum computing, low-power VLSI, and emerging optical computing systems.

Despite the strong theoretical motivation, optical implementations of reversible logic gates remain relatively limited compared to conventional optical logic. Existing reversible optical designs have primarily relied on electro-optic MZI structures,

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lithium-niobate waveguides, or complex interferometric configurations[13–18], which often increase hardware complexity, optical loss, and integration overhead. Furthermore, only a few works have explored the realization of reversible logic using active optical devices capable of providing both switching and amplification.

In this context, Reflective Semiconductor Optical Amplifiers (RSOAs) offer a compelling platform for all-optical logic realization. Owing to their reflective configuration, compact footprint, and strong nonlinear gain dynamics, RSOAs support efficient all-optical switching through cross-gain modulation (XGM). Compared to conventional SOAs, RSOAs exhibit enhanced gain utilization, improved signal regeneration, wavelength conversion capability, and compatibility with dense wavelength-division multiplexing (WDM) systems. Consequently, RSOA-based architectures have been successfully employed to demonstrate high-speed conventional optical logic gates and arithmetic circuits[19–22]. However, these studies primarily focus on isolated logic or arithmetic functions and do not report a unified, multiplexer-centric reversible architecture using RSOAs.

Motivated by this research gap, the present work proposes a scalable and reversible all-optical logic architecture based on RSOA-driven Fredkin Reversible Gates (FRGs). Unlike existing RSOA-based approaches, the proposed design explicitly integrates reversible computing principles with photonic switching hardware, enabling information-preserving logic operations in the optical domain. A 2×1 FRG-based optical multiplexer is employed as the fundamental building block, from which a complete set of logic gates NOT, AND, OR, NAND, NOR, XOR, and XNOR along with higher-order circuits such as a 4×1 multiplexer, half-adder, and half-subtractor, are systematically realized. The design methodology leverages Shannon decomposition and Reduced Binary Decision Diagram (RBDD) concepts to ensure modularity, scalability, and minimal hardware overhead.

The performance of the proposed reversible logic circuits is evaluated using key optical metrics, including Extinction Ratio (ER), Contrast Ratio (CR), and Relative Eye Opening (REOP), under Gaussian pulse excitation. The obtained results demonstrate high signal integrity, fast switching response, and excellent noise resilience, confirming the suitability of the proposed architecture for high-speed and energy-efficient photonic computing applications.

The primary novelty of this work lies in the realization of a unified, RSOA-based reversible logic framework that combines FRG architecture, XGM-based switching, and MUX-centric scalability—an approach that has not been comprehensively reported in existing literature. This makes the proposed design a promising candidate for future low-power photonic integrated circuits and optical computing systems.

2 Material and Methods

2.1 Reflective Semiconductor Optical Amplifier (RSOA)

A Reflective Semiconductor Optical Amplifier (RSOA) is a nonlinear optical device designed with two reflective facets, which are typically located at both ends of the optical amplifier. This configuration enables the device to amplify and switch optical signals that pass through it, utilizing carrier density modulation in the semiconductor material.

In RSOAs, the input signal is injected into the device through one facet, where it undergoes amplification and interaction with the carrier population. The second reflective facet then reflects the amplified signal back through the same active region, where it can interact again with the semiconductor carriers, experiencing further amplification or modulation. This reflection-based amplification process enhances the efficiency of the device, making it highly suitable for use in optical communication systems and photonic computing.

Reflective Semiconductor Optical Amplifiers (RSOAs) are widely used for Cross-Gain Modulation (XGM) due to their nonlinear gain dynamics and compact, reflective structure. In XGM, a control pulse (or pump signal) modulates the gain of the RSOA, thereby affecting the amplification of another signal—typically a probe pulse that is simultaneously propagating through the same device. This interaction enables all-optical switching and logic operation without the need for optical-to-electrical conversion (Fig. 1).

When a high-power control signal (usually a Gaussian pulse) is injected into the RSOA, it depletes the carrier density N(t) in the active region through stimulated emission. This carrier depletion leads to gain saturation, which reduces the gain experienced by the probe signal. As a result, the output intensity of the probe pulse is modulated in accordance with the power of the control pulse a phenomenon known as cross-gain modulation[23-24].

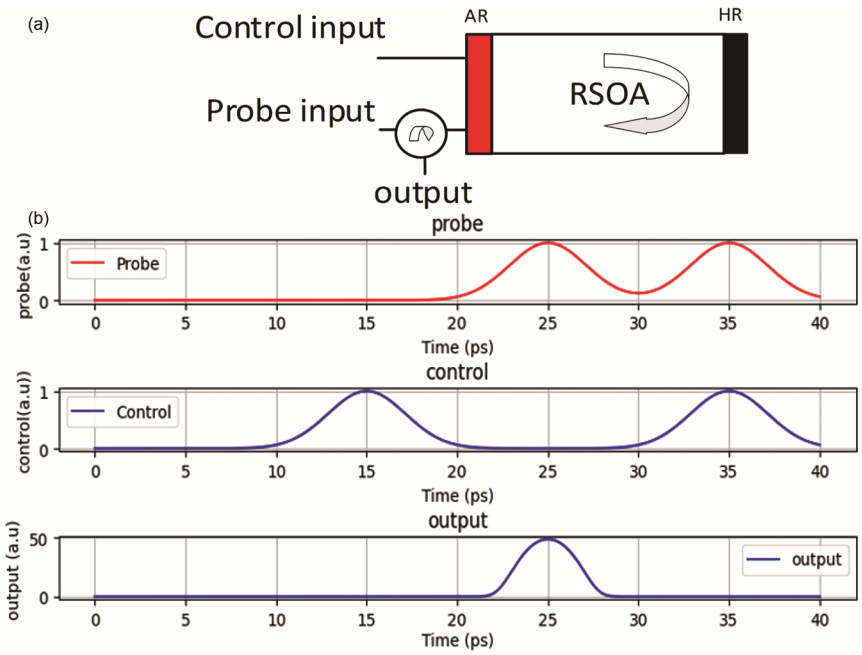

Fig. 1 — (a) RSOA (Reflective semiconductor optical amplifier); and(b) Simulation waveform of RSOA

2.1.1 Mathematical Model

The carrier dynamics in the Reflective Semiconductor Optical Amplifier (RSOA) under cross-gain modulation (XGM) can be modelled by the rate equation:

$$\frac{dN(t)}{dt} = \frac{I}{qV} - \frac{N(t)}{\tau_c} - \frac{g(N(t))|E(t)|^2}{\hbar\omega} \quad \ldots (1)$$

where:

i N(t) is the carrier density,
ii I is the bias current,
iii q is the elementary charge,
iv V is the active volume,
v τ_c is the carrier lifetime,
vi g(N) is the gain coefficient,
vii $|E(t)|^2$is the optical field intensity,
viii $\hbar\omega$ is the photon energy

The optical power P(t) inside the RSOA is related to the carrier density N(t) by the following equation:

$$P(t) = \eta * \text{Gain}(N(t)) * E(t) \quad \ldots (2)$$

Here, $\eta = R \cdot \eta_c^2 \cdot \Gamma \cdot e^{-2\alpha L}$ denotes the internal efficiency factor of the RSOA. The parameter Rrepresents the reflectivity of the RSOA facet, η_c is the fiber-to-RSOA coupling efficiency accounting for both the input and reflected optical paths, $\Gamma$is the optical confinement factor describing the overlap between the optical mode and the active region, and α is the internal waveguide loss coefficient of the RSOA active region, while L denotes the device length. The exponential term $e^{-2\alpha L}$ accounts for the double-pass propagation loss experienced by the optical signal due to the reflective operation of the RSOA.

In simulations, $\eta$is treated as a normalized constant derived from the structural and material parameters of the RSOA and its gain characteristics, consistent with standard RSOA modeling approaches reported in the literature. The term Gain$(N(t))$represents the optical gain of the RSOA, which depends on the carrier density and is typically modelled as:

$$G(N(t)) = 1 + G_o \frac{N(t)}{N_o} \quad \ldots (3)$$

Here, G_o is the small-signal gain coefficient and N_o is the reference carrier density at which small-signal gain is achieved. This expression captures the carrier-density-dependent gain, useful for understanding how electrical and optical signals interact within the device.

The output optical field is therefore given by:

$$E_{out}(t) = E(t) * \text{Gain}(N(t)) \quad \ldots (4)$$

This output field represents the result of optical amplification modulated by the internal carrier population.

However, when a strong optical control pulse is applied (typically a Gaussian pulse), it depletes the

carrier density via stimulated emission, leading to gain compression. This depletion directly impacts the gain experienced by a weaker co- or counter-propagating probe pulse, described by the gain compression model:

$$G(t) = \frac{G_O}{1+\frac{|E_c(t)|^2}{E_{sat}}} \quad \ldots (5)$$

where:

i G_O is the small-signal gain,

ii $|E_c(t)|^2$represents the instantaneous optical power (or intensity) of the control pulse.,

iii E_{sat} is the saturation energy.

This model is particularly relevant for XGM-based optical logic, as it characterizes how the presence of a control signal modulates the gain seen by the probe. As $|E_c(t)|^2$ increases, the available gain G(t) for the probe decreases, resulting in logic-level modulation of the probe output.

The corresponding probe output power under XGM can be expressed as:

$$P_{out} = P_p e^{(G-\alpha)L} \quad \ldots (6)$$

where P_p is the probe input power, α is the internal loss coefficient, and L is the length of the RSOA.

This exponential relationship highlights how the gain dynamics—modulated by the control pulse—directly influence the energy and power of the probe signal. As the control pulse compresses the gain, G decreases, resulting in a diminished Pout, enabling logic-level differentiation.

Gaussian pulses are used as input signals to investigate the dynamic performance of the RSOA in reversible logic applications. The Gaussian input field Ein(t) is given by:

$$E(t) = E_o e^{\left(-\frac{t^2}{2\sigma^2}\right)} \quad \ldots (7)$$

where E_o is the peak amplitude, and σ is the temporal pulse width related to full width at half maximum (FWHM) by $\sigma = \frac{\tau_{FWHM}}{2\sqrt{2\ln 2}}$. This results in a time-varying gain for the probe:

$$G(t) = \frac{G_O}{1+\frac{{E_o}^2}{E_{sat}}\exp\left(-\frac{t^2}{\sigma^2}\right)} \quad \ldots (8)$$

and the corresponding time-resolved output probe power becomes:

$$P_{out}(t) = P_p\, exp\left[\left(\frac{G_O}{1+\frac{{E_o}^2}{E_{sat}}\exp\left(-\frac{t^2}{\sigma^2}\right)} - \alpha\right)L\right] \quad \ldots (9)$$

This nonlinear interaction between the control and probe signals, governed by gain compression under XGM, enables all-optical logic functions such as XOR, AND, and signal switching. The ultrafast gain response and energy-efficient operation of RSOAs make them well-suited for implementing photonic reversible logic gates in high-speed computing applications[20,21].

In real-world implementations, the total output power accounts not only for the amplified signal but also includes noise contributions from Amplified Spontaneous Emission (ASE), which is inherently generated during the gain process. The ASE power is calculated using the expression:

$$\mathrm{P_{ASE}} = 2\mathrm{n_{sp}} * \mathrm{h\nu(G-1)\Delta f} \quad \ldots (10)$$

where $\mathrm{n_{sp}}$ denotes the spontaneous emission factor, hν represents the photon energy, and Δf is the optical bandwidth. ASE is considered an integral part of the output power, as it originates from spontaneous emission events amplified along with the signal, and is quantitatively modeled using the standard ASE formulation.

2.2 Optical Reversible Logic Gates

Reversible logic gates are a class of logic gates that, unlike conventional gates, do not lose any information during their operation. This means that every output of the gate can be uniquely mapped back to an input, which helps in minimizing power dissipation during computation. The theoretical foundation for reversible logic comes from Landauer's Principle, which states that energy is dissipated in irreversible computations due to the loss of information. However, with reversible logic, since no information is lost, no heat is generated, and hence, power dissipation is reduced significantly.

In reversible logic circuits, the number of outputs is equal to the number of inputs, ensuring that the information can be recovered by reversing the computation. These gates are particularly valuable in low-power applications, such as quantum computing and optical computing, where energy efficiency is paramount.

Reversible logic gates include well-known gates such as Fredkin, Toffoli, Peres, and Feynman gates. These gates can be combined to create complex reversible circuits, where energy-efficient and lossless information processing is required[23-26].

When designing reversible logic gates and circuits, certain parameters need to be considered to evaluate their efficiency.

i Garbage Output: This refers to the number of additional output bits that are required to implement a reversible gate. In many cases, reversible gates might require additional output bits, which do not contribute to the final computation but are necessary to preserve reversibility.

ii Constant Input: Some reversible gates may require constant input bits that do not change during the operation of the circuit. These inputs are used to ensure reversibility but do not contribute to the actual computation. Reducing the number of constant inputs is important for simplifying the design and improving performance.

iii Gate Count: This refers to the total number of gates used in the design of a reversible circuit. The gate count is a critical parameter in evaluating the efficiency of a reversible logic circuit. Minimizing gate count reduces the overall complexity and helps in reducing the size and power consumption of the circuit.

The optical cost and optical delay of the proposed RSOA-based gates have been analysed to evaluate their hardware efficiency and suitability for high-speed photonic logic applications. Optical cost is defined as the total number of active optical components specifically RSOAs, couplers, and related switching elements required to realize a logic operation. In this study, only the RSOAs are considered in the cost metric, each assigned a unit value of one. The proposed architecture employs a minimal number of RSOA-based FRG gates, leading to a significantly reduced optical cost compared to traditional multiplexer configurations based on MZI-SOA, TOAD, or photonic crystal ring resonator technologies. This reduction simplifies the circuit layout, reduces power consumption, and eases integration overhead. Optical delay, a key determinant of system performance, is defined as the product of the individual delay (Δ) and the number of RSOAs present along the critical path of the logic realization. The RSOA elements operate using cross-gain modulation (XGM), which enables fast carrier dynamics with response times typically ranging between 10–20 ps. Consequently, the proposed logic circuits demonstrate minimal optical delays, enabling high-speed operation exceeding 100 Gbps. These characteristics low optical cost and reduced latency confirm the feasibility and efficiency of the proposed design for scalable, energy-efficient, and high-performance photonic integrated circuits.

3 Implementation and Simulation

In RSOA (Reflective Semiconductor Optical Amplifier)-based optical circuits, the design of reversible logic gates involves manipulating optical signals through nonlinear switching characteristics of the RSOA. Here's a detailed description of two specific gates implemented using RSOAs.

3.1 FG Gate (Feynman Gate)

The Feynman gate (FG) is a 2-input reversible logic gate primarily designed to perform the exclusive-OR (XOR) operation. It can be physically realized using a pair of Reflective Semiconductor Optical Amplifier (RSOA) switches configured such that the control input modulates the switching behaviour of the target input. The resulting output corresponds to the XOR of the control and target inputs, with the RSOA switches facilitating both signal amplification and switching functionalities.

The logical behaviour and operational conditions of the FG gate are shown in Tables 1 and 2, respectively. The architectural schematic of the RSOA-based FG reversible gate is depicted in Fig. 2. Structurally, the FG gate comprises two RSOA switches and three beam splitters. This configuration not only enables XOR operation but also facilitates the duplication of the input signal, which is a desirable feature in reversible logic circuits.

The optical cost associated with the FG gate is 2, and the corresponding optical delay is 1Δ. The correctness of the logic operation has been verified through simulation waveforms, which confirm consistency with the theoretical truth table.

Table 1 — Truth table of FG gate

INPUTS		OUTPUTS	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 2 — Operation table of RSOA-Based FG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\overline{A}B$
RSOA2	A	B	$\overline{B}A$

P = A
Q = RSOA1 + RSOA2 = A $\oplus$ B

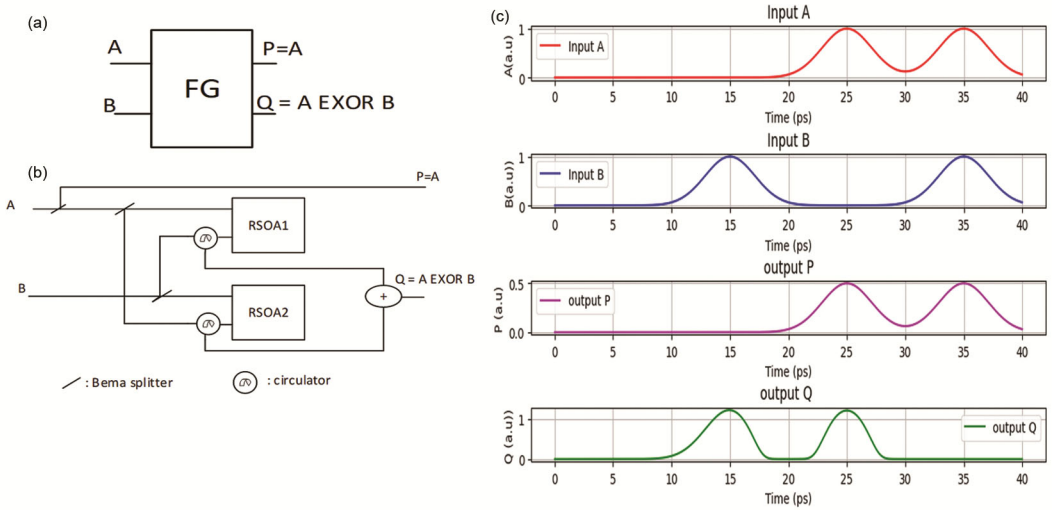

Fig. 2 — (a) Block diagram of FG gate (b) RSOA implementation of FG gate; and (c) Simulation waveform of FG gate

Table 3 — Operational table of RSOA-Based FRG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\overline{A}B$
RSOA2	C	A	$\overline{A}C$
RSOA3	'high'	A	$\overline{A}$
RSOA4	B	$\overline{A}$	AB
RSOA5	C	$\overline{A}$	AC

P = A

Q = RSOA1 + RSOA5 = $\overline{A}B$+ AC

R = RSOA2 + ROSA4 =$\overline{A}C$ + AB

Table 4 — Truth table of FRG gate

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

The functional model of the FG gate is defined as follows: Output 1 (P) = A, Output 2 (Q) = A $\oplus$ B, where A and B are the gate inputs and $\oplus$ denotes the XOR operation[27-29].

3.2 FRG Gate (Fredkin-Reversible Gate)

The Fredkin gate (FRG), also referred to as the Controlled-Swap gate, is a fundamental 3×3 reversible logic gate that performs a conditional exchange of its two target inputs based on the value of a control input. It preserves the principles of reversibility by maintaining a bijective mapping between its input and output vectors. In the optical implementation, the FRG gate leverages the nonlinear gain characteristics of Reflective Semiconductor Optical Amplifiers (RSOAs), where the control signal modulates the gain dynamics of the RSOA, thereby determining whether the target signals are transmitted directly or interchanged.

The operational behaviour of the FRG gate is summarized in Table 3. The optical realization of the gate comprises five RSOA switches and six beam splitters.

The corresponding optical cost and optical delay are evaluated as 5 and 2Δ, respectively[30].

Let the input vector be denoted as (A, B, C), where A serves as the control input and B and C are the target inputs. The outputs are defined as: Output 1 (P) = A, Output 2 (Q) = $\overline{A}B$ + AC,Output 3 (R) = $\overline{A}C$ + AB.

These expressions realize the controlled swap operation

i When A = 0, the gate outputs Q = B and R = C, indicating no swap

ii When A = 1, the gate outputs Q = C and R = B, thereby swapping B and C

These outputs can be equivalently expressed using 2×1 multiplexer logic as: Output 2(Q) = $\overline{A}B \oplus AC$, Output 3(R) = $\overline{A}C \oplus AB$, where $\oplus$ denotes the XOR operation. These forms uphold the condition of logical reversibility, enabling the unique reconstruction of the input vector from the output values[26-30].

Table 4 presents the corresponding truth table, while the simulated waveforms shown in Fig. 3 further corroborate the correctness of the reversible

operation of the FRG gate. Figure 4 shows the mapping of output Q using a 2×1 multiplexer structure, clearly illustrating its equivalence to multiplexer logic. The truth table of the 2×1 multiplexer is provided in Table 5 for reference. A Variable Optical Attenuator (VOA) was also used at the input to regulate the optical power entering the RSOA, ensuring it operates within its optimal gain range for accurate and stable logic performance.

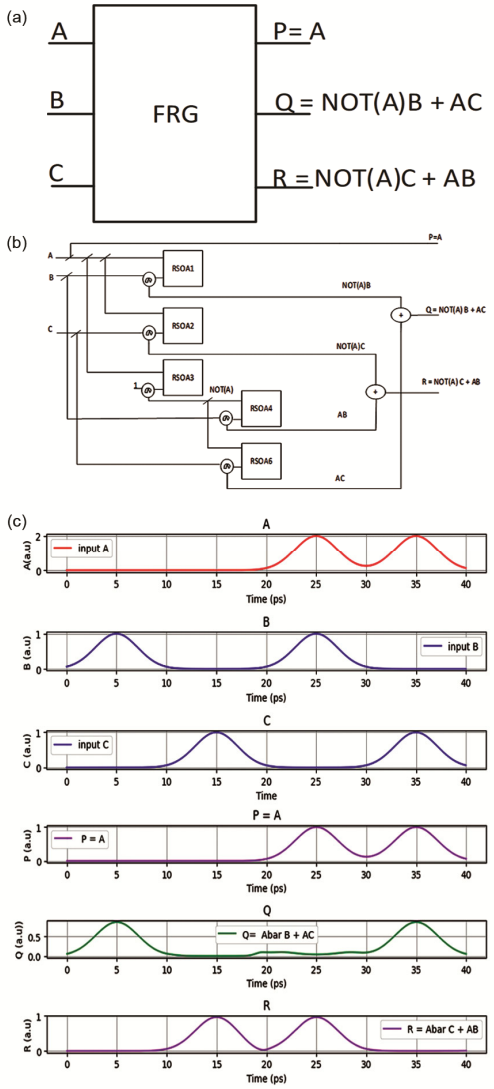

Fig. 3 — (a) Block diagram of FRG gate (b) RSOA implementation of FRG gate; and (c) Simulation waveform of FRG gate

To design combinational logic functions such as AND, OR, NOT, NAND. NOR, XOR and XNOR using 2×1 MUX-based optical circuits, we employ a dual approach that combines both direct logic expressions and theoretical modelling using the Shannon Decomposition Theorem (SDT) and Binary Decision Diagrams (BDD). While basic gates can be efficiently implemented by directly mapping Boolean equations onto MUX control and data inputs, the SDT provides a systematic framework to decompose any Boolean function into a MUX-like structure of the form: $f = A' \cdot I0 + A \cdot I1$. This decomposition directly corresponds to the behaviour of a 2×1 MUX where the variable A acts as the select line and *I0* and *I1* are the data inputs. Additionally, Binary Decision Diagrams (BDDs) and their reduced form (RBDDs) enable optimized representation of Boolean functions, minimizing logic redundancy and guiding efficient gate-level realization in large-scale designs. In our optical implementation, BDD- driven logic synthesis is particularly beneficial in reducing the number of RSOA switches, thereby improving power efficiency, speed, and layout compactness. Thus, both theoretical and practical considerations are harmonized in our proposed design methodology[31-42].

Table 5 — Truth table 2X1 MUX

SELECT LINE S	I0	I1	f(Z)
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

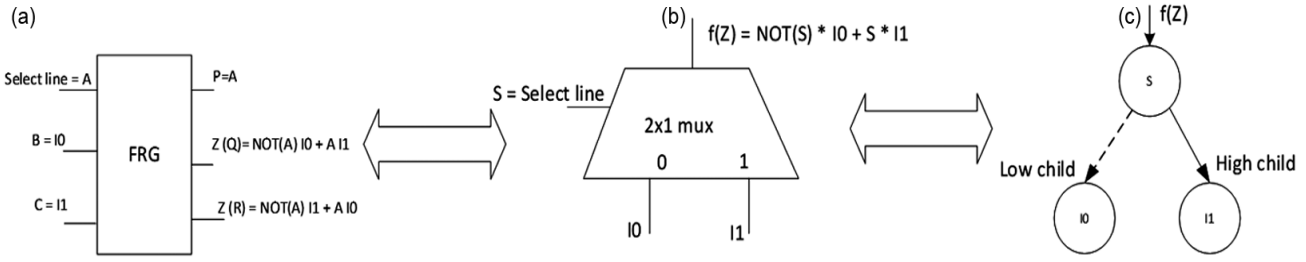

Fig. 4 — (a) Block diagram of FRG gate, (b) 2X1 MUX mapping of FRG gate; and (c) BDD diagram of 2X1 MUX[30-36]

3.3 Application in RSOA-based 2:1 MUX Design

3.3.1 NOT Gate sing 2:1 MUX

A special case of 2×1 multiplexer logic can also be configured to realize a NOT gate by selecting fixed logic inputs and utilizing the select line as the control input. In this configuration, the select line A acts as the control signal, while the multiplexer inputs are fixed at logical '1' and '0' as shown in Fig. 5. The resulting logic is as follows

i When A = 0, the output is '1'.
ii When A = 1, the output is '0'.

Thus, the output effectively corresponds to $\overline{A}$, i.e., the logical inversion of input A. This operation is implemented using a single RSOA-based multiplexer, where the nonlinear switching behaviour of the RSOA enables toggling of the output depending on the control pulse applied at input A.

The functional operation of the RSOA-based MUX acting as a NOT gate is detailed in Table 6, and the corresponding simulation results are illustrated in Fig. 6. The complete truth table of the NOT gate is summarized in Table 7, confirming the correct logical behaviour and reversibility of the design.

Table 6 — Operational table of RSOA-Based 2x1 MUX -NOT gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	1	A	$\overline{A}$
RSOA2	0	A	0
RSOA3	'high'	A	$\overline{A}$
RSOA4	1	$\overline{A}$	A
RSOA5	0	$\overline{A}$	0

P = A
Q = RSOA1 + RSOA5 = $\overline{A}$
R = RSOA2 + ROSA4 =A

Table 7 — Truth table NOT gate

INPUTS A	OUTPUT Y
0	1
1	0

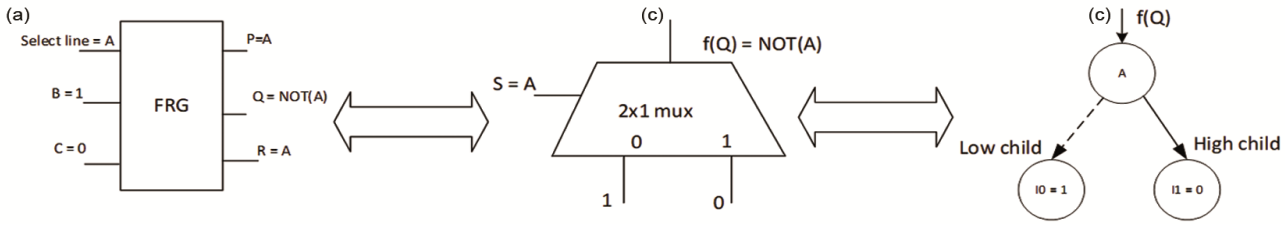

Fig. 5 — (a) FRG gate as NOT gate, (b) 2X1 MUX -NOT gate; and (c) BDD diagram of NOT gate

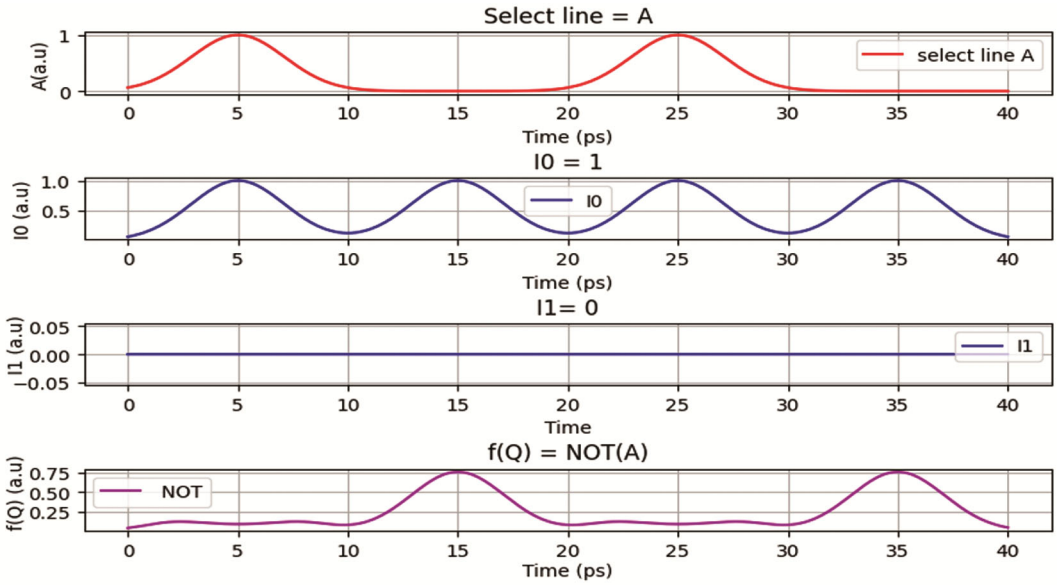

Fig. 6 — Simulation waveform of 2X1 MUX-NOT gate

3.3.2 AND Gate using 2:1 MUX

An AND gate can also be implemented by configuring a 2×1 multiplexer with specific input assignments, allowing the multiplexer to perform the logical AND operation between two signals. In this configuration:

i The select line is assigned to input A
ii The multiplexer inputs are set as 0 and B

The logical behaviour can be described as: When A = 0, the output is '0' and When A = 1, the output is B.

This operation effectively realizes the Boolean Function A·B (logical AND between A and B), Fig. 7. The AND gate thus exploits the control functionality of the MUX structure, where the RSOA-based switching selectively routes the probe signal depending on the control input A.

The operational behaviour of the AND gate using a 2×1 MUX is summarized in Table 8, and the corresponding simulation results are depicted in Fig. 8. The truth table confirming the logical correctness of the AND gate is presented in Table 9.

3.3.3 OR Gate using 2:1 MUX

An OR gate can be realized using a 2×1 multiplexer by assigning appropriate values to the multiplexer inputs and the select line. In this implementation:

i The select line is connected to input A
ii The MUX inputs are assigned as B and logic '1'

The logical operation follows:

Table 8 — Operational table of RSOA-Based FRG 2X1- MUX AND gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	0	A	0
RSOA2	B	A	$\bar{A}B$
RSOA3	'high'	A	$\bar{A}$
RSOA4	0	$\bar{A}$	0
RSOA5	B	$\bar{A}$	AB

P = A
Q = RSOA1 + RSOA5 = AB
R = RSOA2 + ROSA4 = $\bar{A}B$

Table 9 — Truth table AND gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	0
1	0	0
1	1	1

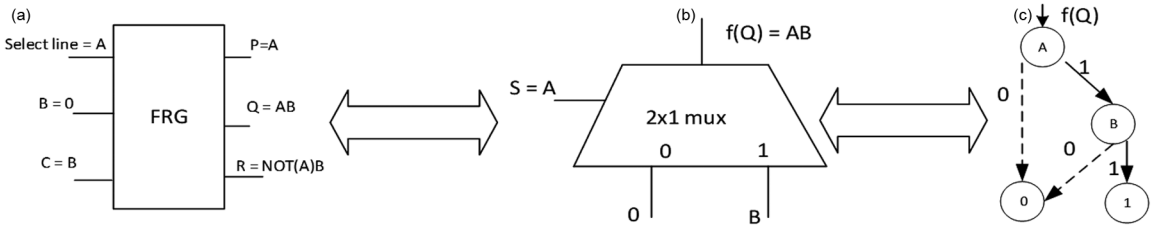

Fig. 7 — (a) FRG gate as AND gate (b) 2X1 MUX -AND gate; and (c) RBDD diagram of AND gate

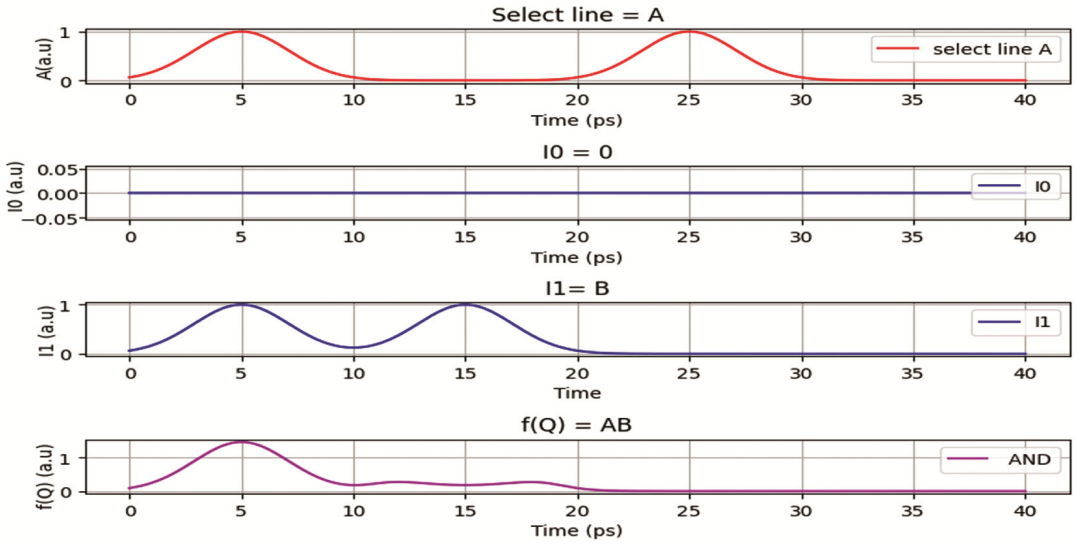

Fig. 8 — Simulation waveform of 2X1 MUX-AND gate

i When A = 0, the output is B
ii When A = 1, the output is '1'

This configuration effectively performs the Boolean function A + B (logical OR) shown in Fig. 9. The RSOA-based MUX leverages the gain-switching behaviour to direct the output based on the control input, thus enabling all-optical realization of the OR function. The operational mapping of this OR gate configuration is detailed in Table 10, while the simulation results are presented in Fig. 10. The truth table verifying the logical behaviour is provided in Table 11.

3.3.4 2X1 MUX as NAND Gate

A NAND gate can also be constructed using a 2×1 multiplexer by setting the select and input lines appropriately to reflect the NAND logic. In this configuration:

i The select line is assigned to input A
ii The multiplexer inputs are set as logic '1' and $\overline{B}$ (i.e., inputs = 1, $\overline{B}$,)

The resulting behaviour of the circuit can be described as follows: when input A is set to '1', the output corresponds to the logical complement of B (i.e., $\overline{B}$), whereas when A is '0', the output remains fixed at logical high ('1'). To achieve this functionality, an FG gate is employed, where the input A of the FG gate is held at logic '1' in order to produce $\overline{B}$ at the output. This configuration effectively leverages the reversible nature of the FG gate to implement a controlled NOT operation based on the value of A

Table 10 — Operational table of RSOA-Based FRG 2X1 MUX- OR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\overline{A}B$
RSOA2	1	A	$\overline{A}$
RSOA3	'high'	A	$\overline{A}$
RSOA4	B	$\overline{A}$	AB
RSOA5	1	$\overline{A}$	A

P = A
Q = RSOA1 + RSOA5 = $\overline{A}B$+ A = A + B
R = RSOA2 + ROSA4 =$\overline{A}$+ AB = $\overline{A}$ + B

Table 11 — Truth table OR gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	1

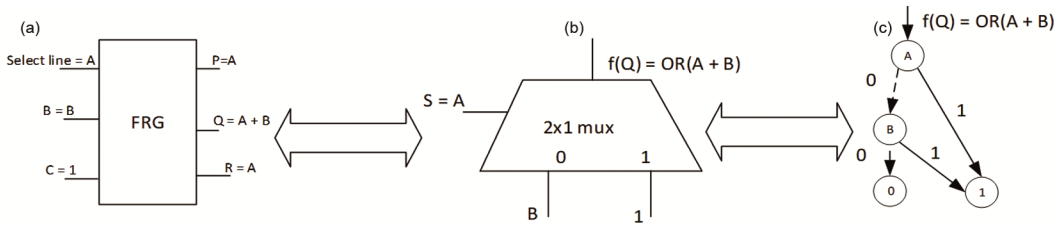

Fig. 9 — (a) FRG gate as OR gate (b) 2X1 MUX -OR gate; and (c) RBDD diagram of OR gate

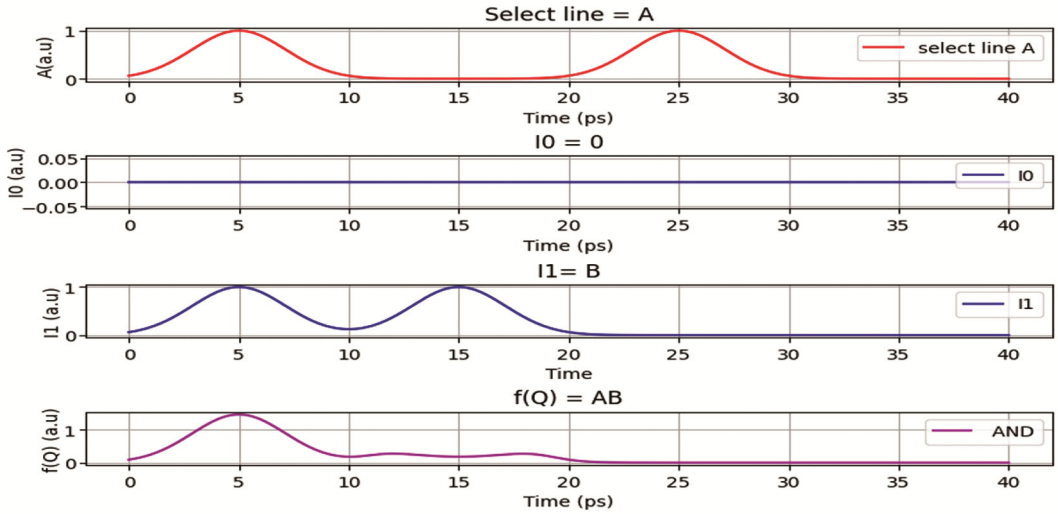

Fig. 10 — Simulation waveform of 2X1 MUX-OR gate

This configuration yields the logical expression ($\overline{AB}$), which defines the NAND function as shown in Fig. 11. The RSOA-based MUX enables dynamic switching between probe inputs based on the control signal A, and with fixed optical logic levels, realizes the NAND function in an all-optical domain.

The detailed operation of the NAND gate using a 2×1 MUX is presented in Table 12, and the corresponding simulation waveform is illustrated in Fig. 12. The associated truth table validating this logic is shown in Table 13.

3.3.5 2X1- MUX FRG – NOR Gate

A NOR gate can be implemented using a 2×1 multiplexer by properly assigning the select and input lines to reflect NOR logic behaviour. In this configuration:

i The select line is connected to input A.

ii The MUX inputs are assigned as $\overline{B}$ and logic '0' (i.e., inputs = $\overline{B}$, 0).

The functional behaviour is as follows:

i When A = 0, the output is $\overline{B}$.

ii When A = 1, the output is '0'.

Table 12 — Operational table of RSOA-Based FRG 2X1 MUX – NAND gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	1	A	$\overline{A}$
RSOA2	$\overline{B}$	A	$\overline{A}\overline{B}$
RSOA3	'high'	A	$\overline{A}$
RSOA4	1	$\overline{A}$	A
RSOA5	$\overline{B}$	$\overline{A}$	$A\overline{B}$

P = A

Q = RSOA1 + RSOA5 = $\overline{A}$+ $A\overline{B}$ = $\overline{AB}$

R = RSOA2 + ROSA4 =$\overline{A}\overline{B}$ + A = A + $\overline{B}$

Table 13 − Truth table NAND gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	1
1	0	1
1	1	0

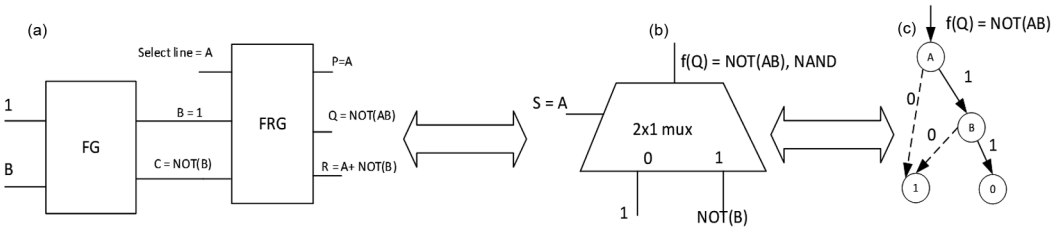

Fig 11 — (a) FRG gate as NAND gate, (b) 2X1 Mux -NAND gate; and (c) RBDD diagram of NAND gate

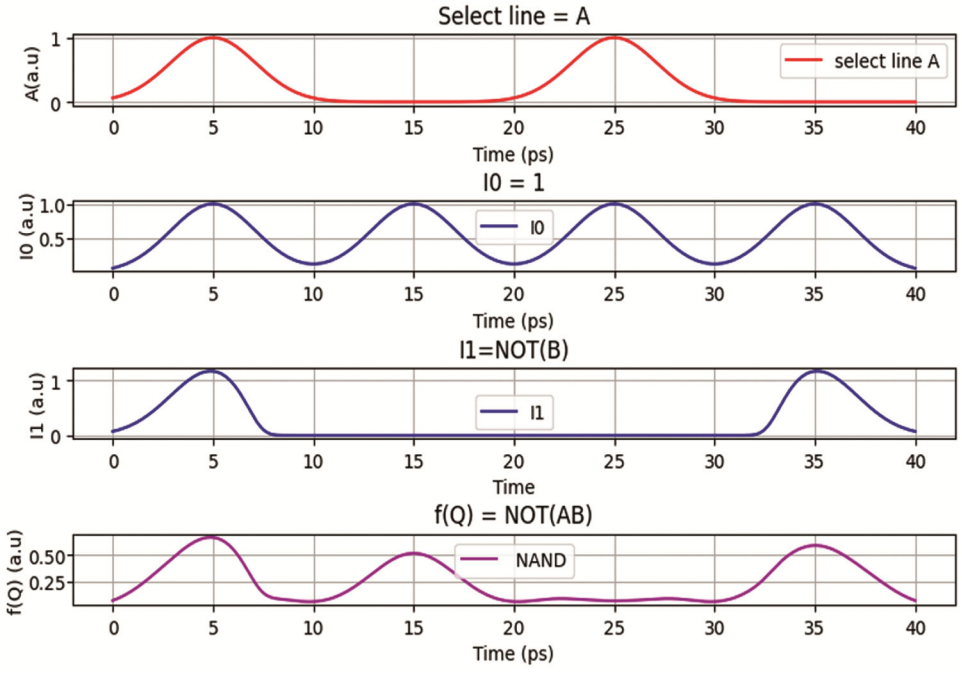

Fig. 12 — Simulation waveform of 2X1 MUX-NAND gate

This arrangement realizes the Boolean function ($\overline{A+B}$), corresponding to the NOR operation illustrated in Fig. 13. The RSOA-based implementation takes advantage of optical gain modulation, where the control input A dynamically routes the appropriate optical signal to achieve NOR logic in an all-optical environment. In this configuration, the FG gate is again employed to generate the complement of B, enabling the construction of the NOR logic function through reversible and energy-efficient optical switching, leveraging the fast carrier dynamics of RSOA devices.

The operational characteristics of the NOR gate using a 2×1 MUX is listed in Table 14, and the corresponding simulation results are illustrated in Fig. 14. The truth table confirming the NOR logic behaviour is shown in Table 15.

3.3.6 FRG-XOR and FRG-XNOR Gate Using 2×1 MUX

The Fredkin Reversible Gate (FRG) can be configured to realize XOR and XNOR logic operations by employing a 2×1 multiplexer with appropriate input assignments. The logic mapping is designed such that the FRG behaviour is maintained while facilitating XOR/XNOR operations through optical switching.

Table 14 — Operational table of RSOA-Based FRG 2X1 MUX-NOR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	$\overline{B}$	A	$\overline{AB}$
RSOA2	0	A	0
RSOA3	'high'	A	$\overline{A}$
RSOA4	$\overline{B}$	$\overline{A}$	$A\overline{B}$
RSOA5	0	$\overline{A}$	0

P = A

Q = RSOA1 + RSOA5 = $\overline{AB}$ = $\overline{A+B}$

R = RSOA2 + ROSA4 = $A\overline{B}$

Table 15 — Truth table NOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	0
1	0	0
1	1	0

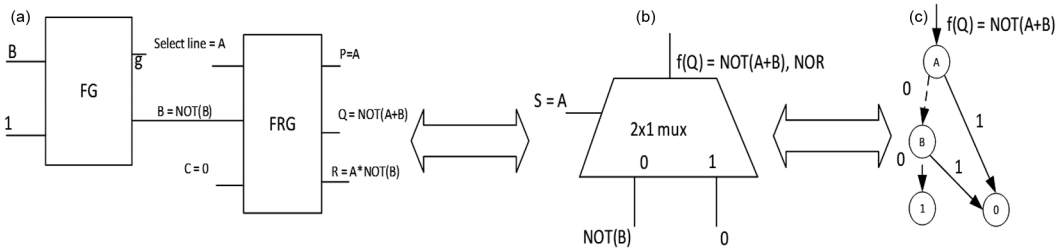

Fig 13 — (a) FRG gate as NOR gate, (b) 2X1 Mux -NOR gate; and (c) RBDD diagram of NOR gate

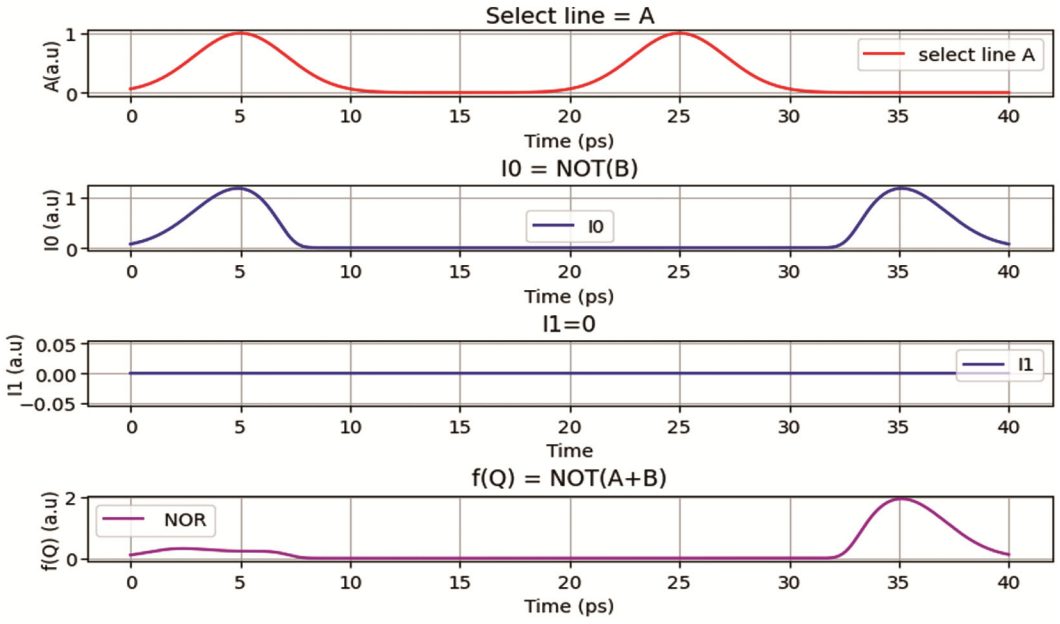

Fig 14 — Simulation waveform of 2X1 MUX-NOR gate

FRG-XOR Gate Configuration:

i Select line: A (control input)
ii MUX inputs: B and $\overline{B}$

The logic operation is as follows:

i When A = 0, output = B
ii When A = 1, output = $\overline{B}$

This structure realizes the logical function: Output Q = A $\oplus$ B. The MUX thereby performs the XOR operation with input A serving as the control bit. The RSOA-based design supports switching between the true and complemented input states based on control input modulation.

FRG-XNOR Gate Configuration:

i Select line: A (control input)
ii MUX inputs: $\overline{B}$ and B

The output behaviour is:

i When A = 0, output = $\overline{B}$
ii When A = 1, output = B

This results in the logical expression: Output Q = A $\odot$ B = $(\overline{A \oplus B})$. This setup effectively implements the XNOR function, maintaining logical reversibility and consistent with the Fredkin gate structure. The operation behaviour of these gates is listed in Table 16. The FG gate is again used to generate the complement of input signal B as depicted in Fig. 15.

Tables 17 and 18 summarize the truth tables for the FRG-XOR and FRG-XNOR configurations, respectively. The corresponding simulation waveforms validating these functions are illustrated in Fig. 16.

3.3.7 4×1 MUX using Three 2:1 MUXes

A 4×1 multiplexer (MUX) selects one of four input signals based on two select lines and directs it to a single output. It can be efficiently implemented using a cascade of three 2×1 MUXes, which provides a modular and scalable design for all-optical logic systems.

Design Configuration:

i Let the four inputs be: I_0, I_1, I_2, I_3
ii Let the select lines be: A_0 (LSB), A_1 (MSB)

The hierarchical implementation uses:

i MUX1: Select line = A_0, inputs = I_0 and I_1 → output = Y_0

Table 16 — Operational table of RSOA-Based 2X1-MUX FRG-XOR/ XNOR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\overline{A}B$
RSOA2	$\overline{B}$	A	$\overline{A}\overline{B}$
RSOA3	'high'	A	$\overline{A}$
RSOA4	B	$\overline{A}$	AB
RSOA5	$\overline{B}$	$\overline{A}$	$A\overline{B}$

P = A
Q = RSOA1 + RSOA5 = $\overline{A}B$+ $A\overline{B}$
R = RSOA2 + ROSA4 =$\overline{A}\overline{B}$ + AB

Table 17 — Truth table XOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 18 — Truth table XNOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	0
1	0	0
1	1	1

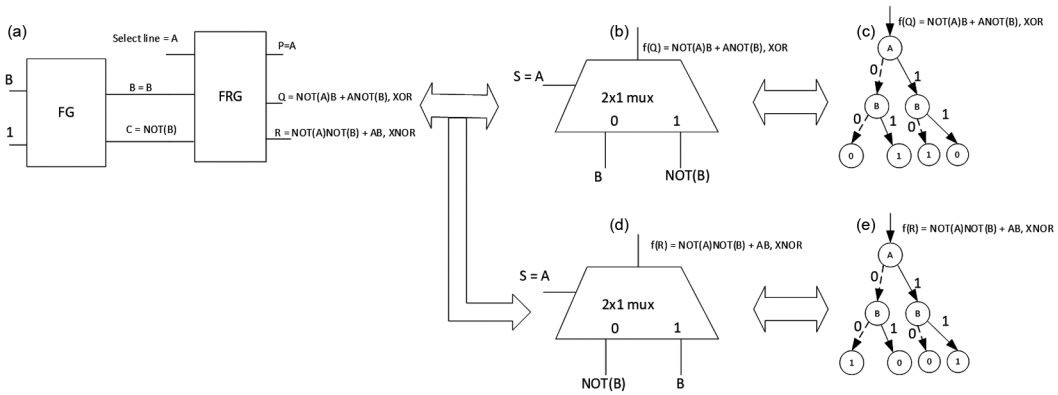

Fig 15 — (a) FRG gate as XOR and XNOR gate, (b) 2X1 Mux -XOR gate, (c) BDD diagram of XOR gate, (d) 2X1 Mux -XNOR gate; and (e) BDD diagram of XNOR gate

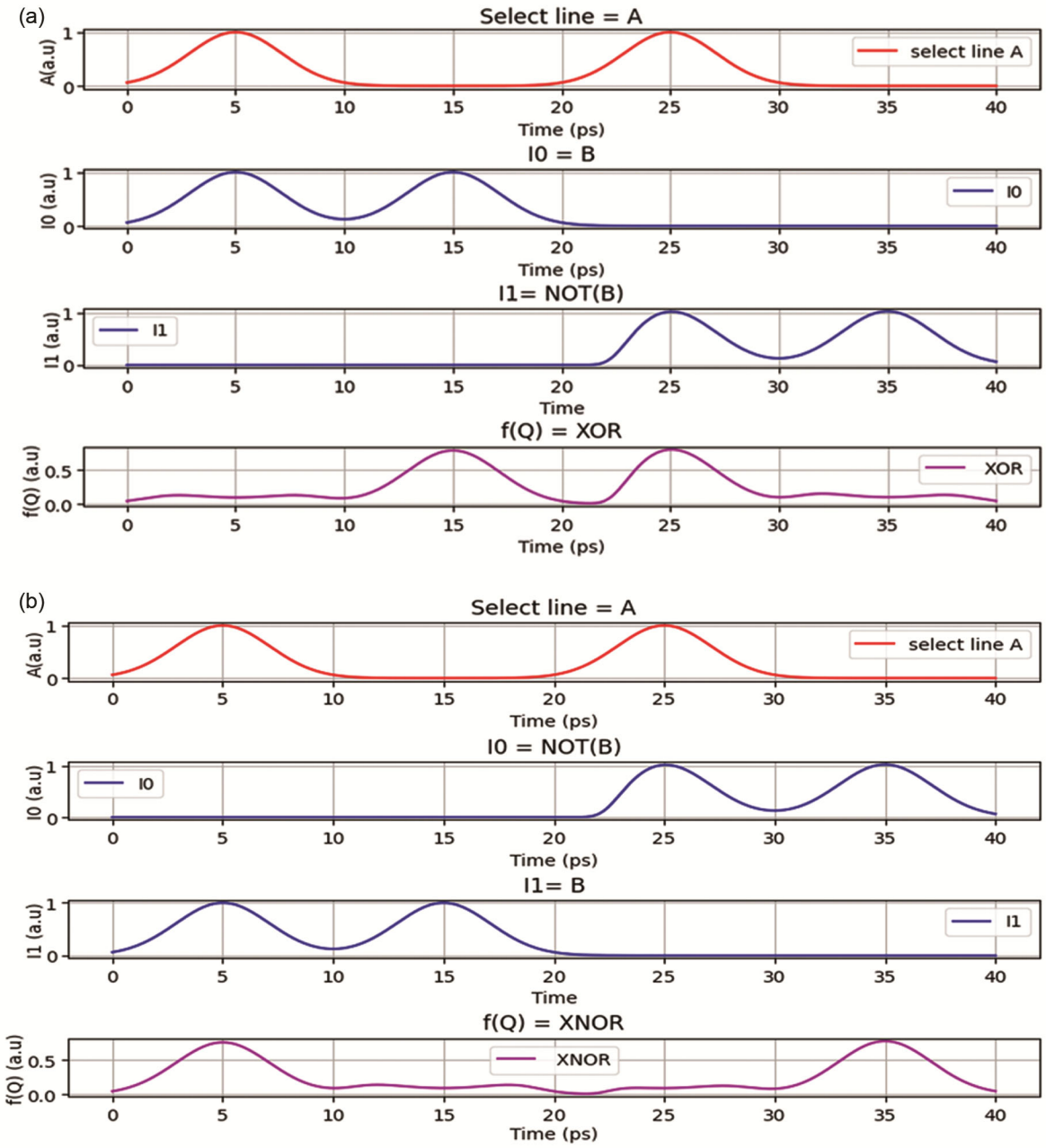

Fig. 16 — Simulation waveform of (a) 2X1 MUX-XOR; and (b) 2X1 MUX-XNOR gate

ii MUX2: Select line = A_0, inputs = I_2 and I_3 → output = Y_1

iii MUX3: Select line = A_1, inputs = Y_0 and Y_1 → output = Final Output (Z)

Functional Behaviour:

i If $A_1A_0 = 00$ → Output $Z = I_0$

ii If $A_1A_0 = 01$ → Output $Z = I_1$

iii If $A_1A_0 = 10$ → Output $Z = I_2$

iv If $A_1A_0 = 11$ → Output $Z = I_3$

This configuration ensures minimal gate count and optical delay while maintaining the logical integrity and reversibility of the circuit when implemented in an all-optical platform using RSOA-based switching elements.

Table 19 presents the truth table of the 4×1 MUX, and Fig. 17 illustrates the block diagram of its implementation using three 2×1 MUXes and Fig. 18 illustrate the corresponding simulation waveforms validating the function.

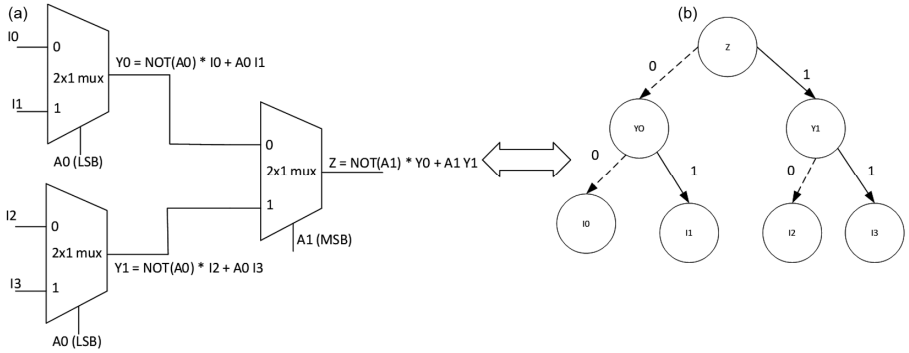

Fig 17 — (a) 4 X 1 MUX realization using 2X1 MUX; and (b) BDD diagram of 4X1 MUX

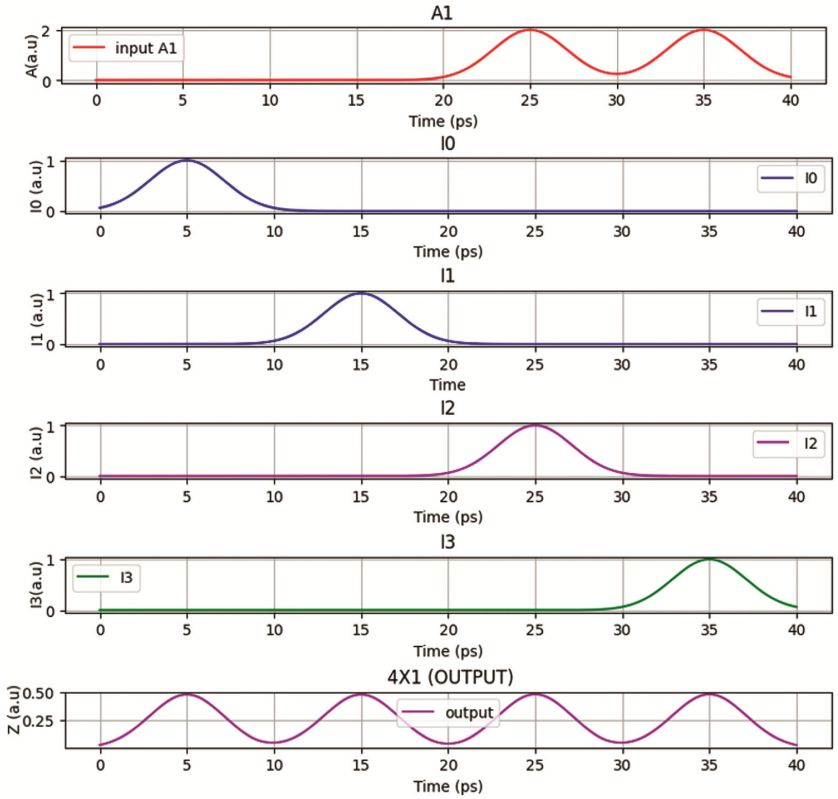

Fig. 18 — Simulation waveform of 4X1 MUX

Table 19 — Truth table 4X1 MUX

SELECT LINE A1	SELECT LINE A0	OUTPUT Z
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Table 20 — Truth table HALF-ADDER

INPUT A	INPUT B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.3.8. 2:1 MUX as Half Adder

A 2×1 multiplexer (MUX) can be effectively utilized to implement a half adder by appropriately configuring its selection and data input logic. A half adder computes the sum and carries outputs for two binary inputs, A and B. The corresponding truth table of the half adder is presented in Table 20. The sum output (A ⊕ B) can be realized by setting the select line to B and configuring the MUX inputs as $I_0 = A$ and $I_1 = \bar{A}$, thereby emulating the XOR operation. Two alternative methods for generating the complement input $I_1 = \bar{A}$ are depicted in Fig. 19; either method can be adopted based on design requirements. For the carry output (A·B), a second 2×1 MUX can be employed with suitable control settings to realize the logical AND operation

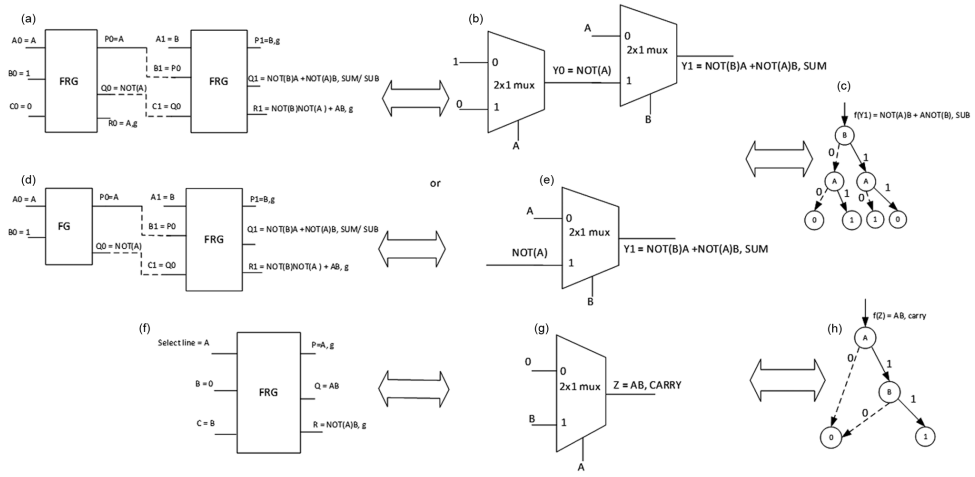

Fig. 19 — (a) FRG –XOR (SUM) gate, (b) 2X1- MUX-XOR (SUM) gate, (c) BDD diagram of XOR(SUM), (d) FG-FRG-XOR (SUM) gate, (e) 2X1 MUX XOR (SUM) gate, (f) FRG-AND (CARRY) gate, (g) 2X1-MUX AND (CARRY) gate; and (h) BDD diagram of AND (CARRY)

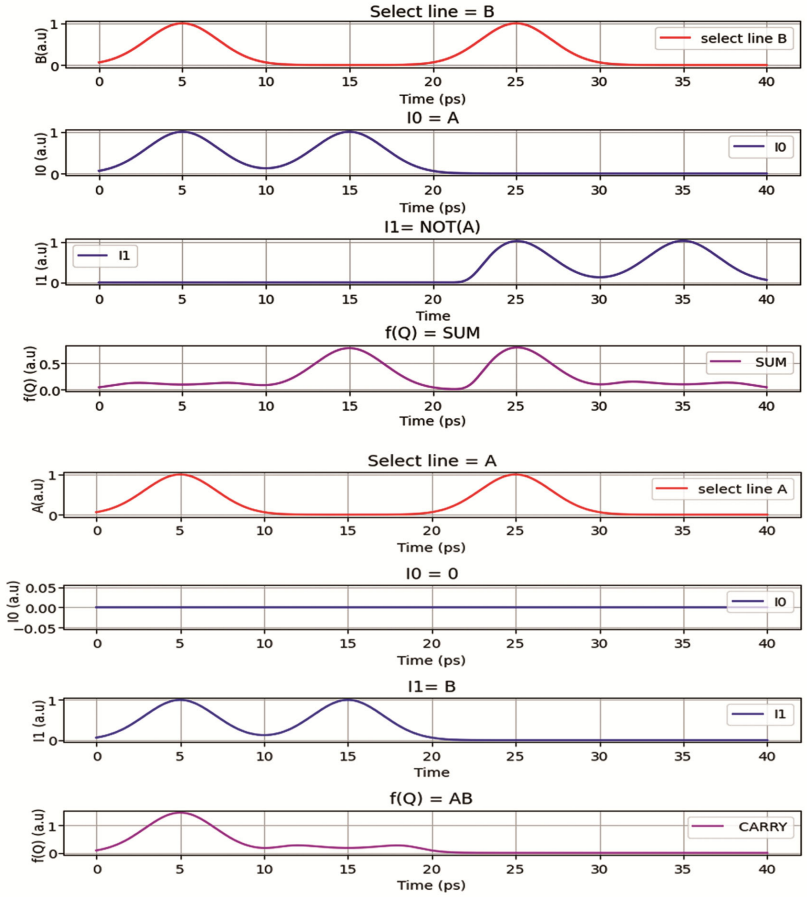

Fig. 20 — Simulation waveform of 2X1 MUX-half adder (a) SUM; and (b) CARRY

By cascading these MUX-based designs, the complete half adder circuit achieves an all-optical implementation with minimized hardware complexity, offering significant advantages for ultrafast and low-energy photonic computation within RSOA-MUX-based logic architectures. The simulation results validating the operation of the half adder are shown in Fig. 20[43].

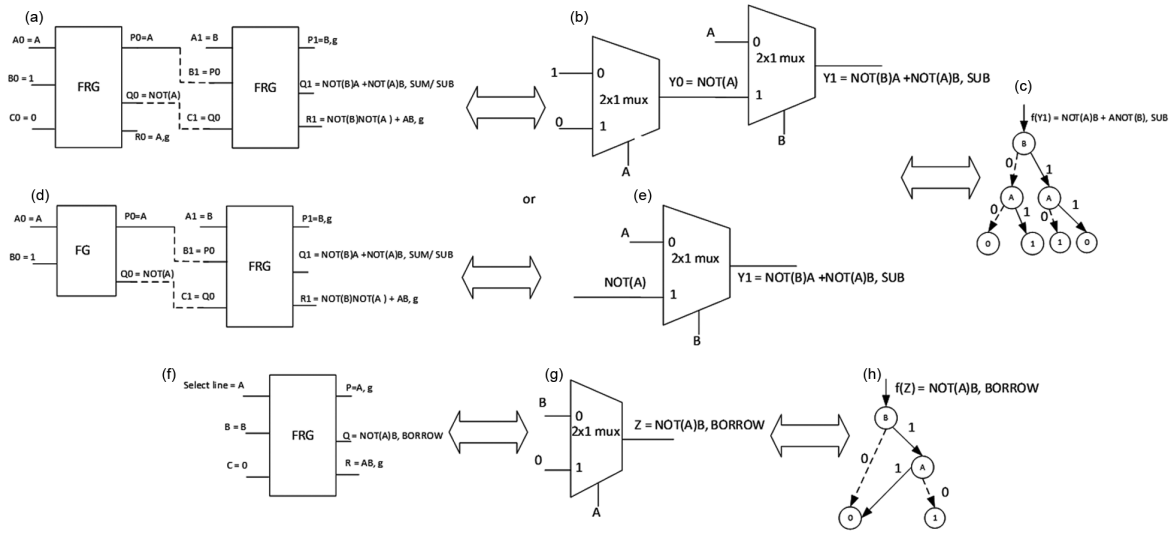

Fig. 21 — (a) FRG –XOR (SUB) gate, (b) 2X1- MUX-XOR (SUB) gate, (c) BDD diagram of XOR(SUB), (d) FG-FRG-XOR (SUB) gate, (e) 2X1 MUX XOR (SUB) gate, (f) FRG-AND (BORROW) gate, (g) 2X1-MUX AND (BORROW) gate; and (h) RBDD diagram of AND (BORROW)

3.3.9 2X1 MUX as Half-Subtractor

A 2×1 multiplexer (MUX) can also be configured to implement a basic binary subtractor by strategically selecting the data and control inputs. A subtractor computes the difference (SUB = A ⊕ B) and the borrow (Borrow = $\bar{A}$ · B) for two binary inputs, A and B. The truth table of the 1-bit subtractor is presented in Table 21. The difference output can be implemented using a 2×1 MUX by assigning the select line as B, and configuring the inputs as I_0 = A and I_1 = $\bar{A}$, thereby replicating the XOR operation. This is identical to the sum output in a half adder. Two methods for generating $\bar{A}$ are illustrated in Fig. 21, and either method can be employed depending on the circuit design.

For the borrow output ($\bar{A}$·B), the MUX is configured to behave as an AND gate with the input I0 = B, I1= 0 and select line A. This configuration enables the realization of a subtractor using compact all-optical hardware with minimal gate count. Such a design is well-suited for high-speed, energy-efficient computing platforms based on RSOA-MUX logic. The simulation results for the subtractor are shown in Fig. 22, confirming the correctness of the design[43].

Table 21 — Truth table Half-Subtractor

INPUT A	INPUT B	SUB	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 22 — RSOA Parameter

Symbol	Parameter	Value
Γ	Confinement factor	0.48
c	Velocity of light	3×10^8m/s
I	Injection current	220 mA
αN	Differential gain	$3.3 \times 10^{-20} m^2$
N_t	Carrier density at transparency	$1 \times 10^{24} m^{-3}$
w	Width of the active region	1.5 µm
d	Depth of the active region	250 nm
L	Active length	150 µm
α_D	Internal loss of the waveguide	2700 m^{-1}
λ	Wavelength of light	1550 nm
E_c	Control pulse energy	20fJ
τ_{FWHM}	Full-width at half-maximum	5 ps
n_2	Nonlinear coefficient	$2.6 \times 10^{-20} m^2/w$
D	Dispersion constant	1 ps/(nm km)
A_{eff}	Fiber effective area	$5 \times 10^{-13} m^2$
Es	Saturation energy	30 fJ
b0	Optical bandwidth	3 nm
n_{sp}	ASE factor	2
B	data rate	100 Gbps
R	Reflectivity of the RSOA reflective facet	0.6
η_c	Fiber-to-RSOA coupling efficiency	0.7

4 Results

The performance of various all-optical logic circuits, implemented using the Fredkin Reversible Gate (FRG) within an RSOA-based architecture, was evaluated under a small-signal gain condition of 20 dB, employing Gaussian pulse inputs. Table 22

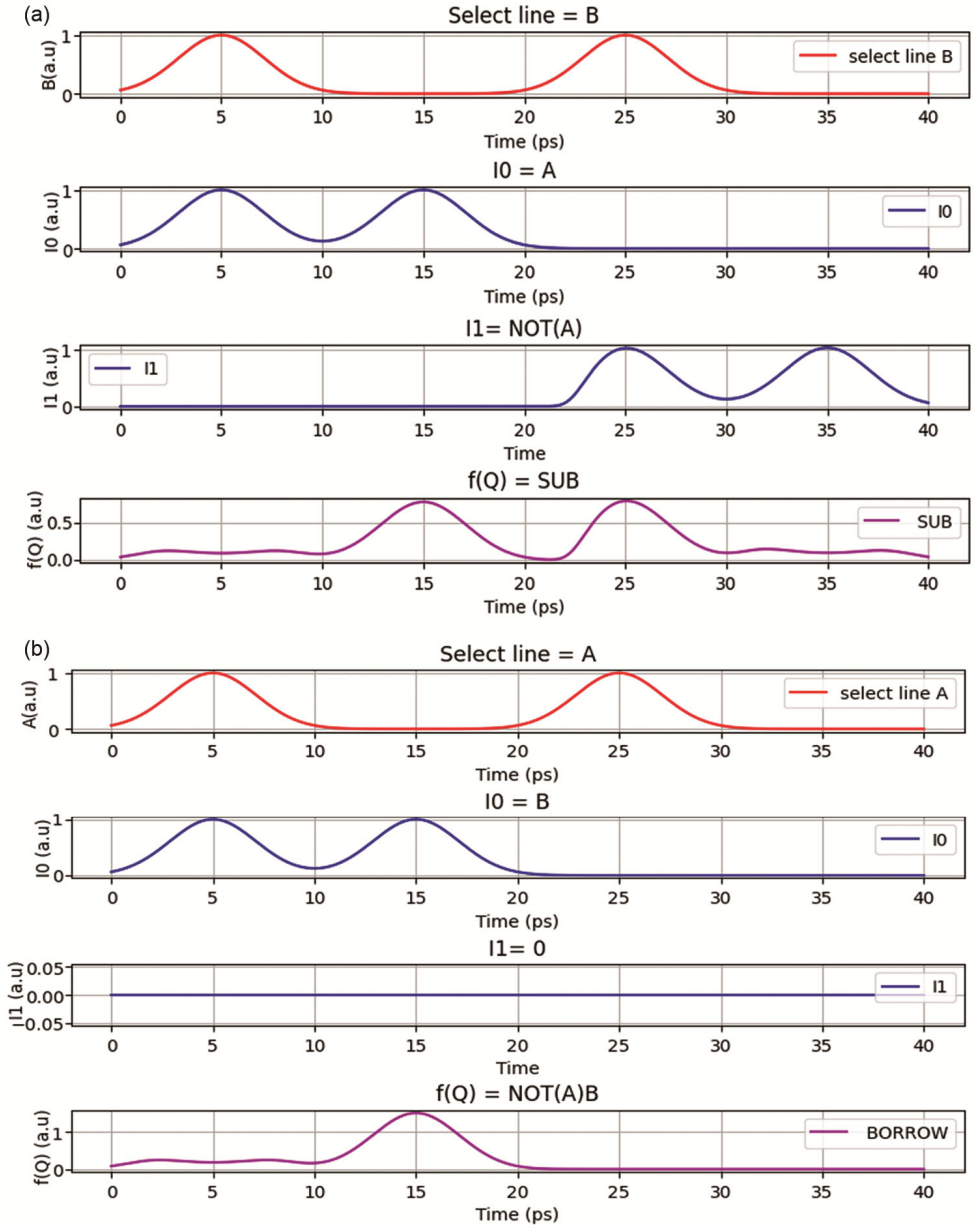

Fig. 22 — Simulation waveform of 2X1 MUX-half subtractor (a) SUB; and (b) BORROW

present the parameter used in the designing of the logic gate. Simulations conducted in Python verified distinct logical functionality across all designed circuits, including NOT, AND, OR, NOR, NAND, XOR, XNOR, Half-Adder, Half-Subtractor, and a 4×1 multiplexer.

The response of the FRG-based multiplexer (FRG-MUX) was analysed in terms of key optical performance metrics: Extinction Ratio (ER), Contrast Ratio (CR), and Relative Eye Opening (REOP). The CR, expressed in decibels (dB), quantifies the optical mean power ratio between logic '1' and logic '0', calculated as $CR = 10\log_{10}\left(\frac{P_1}{P_0}\right)$ where P_1 and P_0 represent the mean optical powers for logic '1' and '0', respectively. The ER assesses the distinguishability between logic levels by comparing the minimum power in the logic '1' state and the maximum power in the logic '0' state, given by $ER = 10\log_{10}\left(\frac{P_{min}}{P_{max}}\right)$. The REOP is defined as $REOP(\%) = \left(\frac{P_{min}-P_{max}}{P_{min}}\right) \times 100$ where P_{min} and P_{max} denote the minimum and maximum values of the logic '1' and '0' states, respectively.

Fig. 23 illustrates the pseudo eye diagram obtained by superimposing Gaussian output pulses corresponding to logic '1' and logic '0' states, providing a visual confirmation of the eye opening that complements the quantitative extinction ratio (ER), contrast ratio (CR), and relative eye-opening penalty (REOP) analysis. As illustrated in Fig. 24, at a bias current I = 220 mA and control energy of 20 fJ, the ER reaches approximately 18 dB, the CR is around 22 dB, and the REOP approaches 99 %. These results confirm that the proposed FRG-based MUX achieves high extinction and contrast ratios, along with excellent eye opening, thereby establishing its suitability for high-speed photonic integration.

Table 23 summarizes the performance parameters of the proposed 2×1 MUX-based logic gates in terms of constant inputs (CI), garbage outputs (GO), gate count (GC), optical cost (OC), and optical delay (OD).

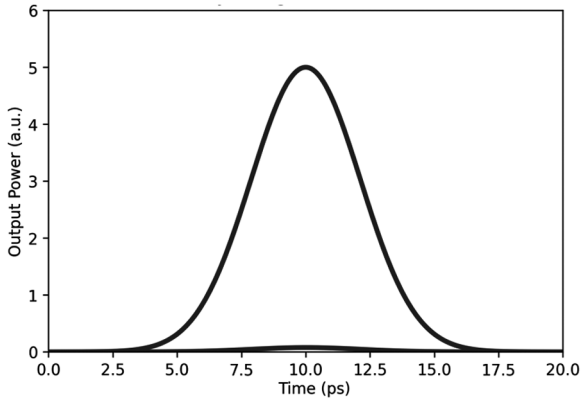

Fig. 23 — Illustrates the pseudo eye diagram obtained by superimposing Gaussian output pulses corresponding to logic '1' and logic '0' states, providing a visual confirmation of eye opening that complements the quantitative ER, CR, and REOP analysis

Table 24 provides a comparative analysis with existing designs, including those based on hybrid plasmonic waveguides, electro-optic Mach Zehnder interferometers (MZI), and photonic crystal ring resonators[44-48]. The proposed RSOA–FRG-based multiplexer demonstrates superior CR and ER values while utilizing a more compact and simplified structure. It is important to note that, to the best of the authors' knowledge, optical

Table 23 — Performance parameter of proposed work

GATE	CI	GC	GO	OC	OD
FRG-2X1 MUX	0	5	1	3	2
NOT	2	5	2	3	2
AND	1	5	2	3	2
OR	1	5	2	3	2
NAND	1	7	2	5	3
NOR	2	7	3	5	3
XOR	1	7	2	5	3
XNOR	1	7	2	5	3
4X1 MUX	0	15	6	9	4

Table 24 — Comparison table of proposed work with the other optical devices

Reference	ER(dB)	CR(dB)	REOP (%)	reversible
[5]	Not calculated	10.84	Not calculated	no
[44]	8.71	11.67	Not calculated	no
[45]	21.61	31.61	Not calculated	no
[46]	Not calculated	21.22	Not calculated	no
[47]	Not calculated	Not calculated	Not calculated	no
[48]	18.6	17.3	85.33	no
[49]	26	26.95	96	no
Our work	18.21	22.18	99.45	yes

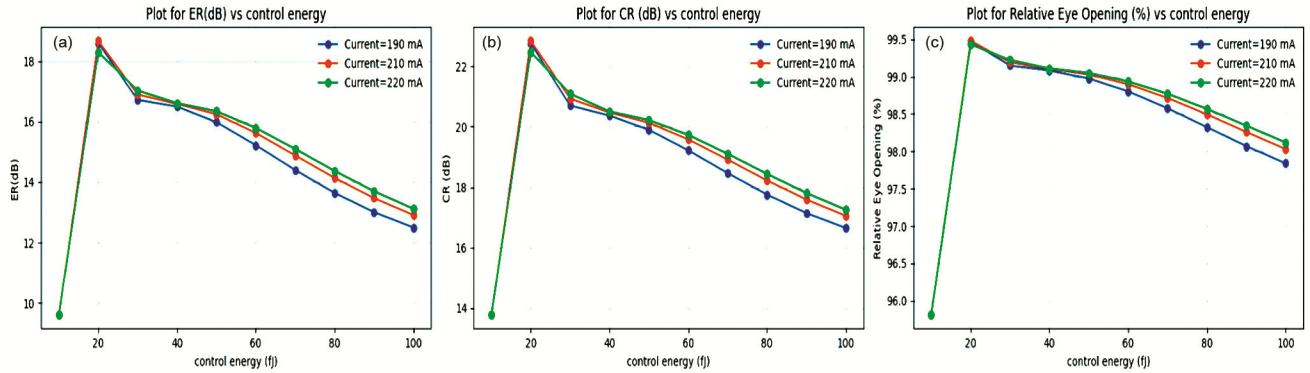

Fig. 24 — Performance analysis of the proposed RSOA-FRG-based 2×1 multiplexer under varying control energy and injection currents using cross-gain modulation (XGM) (a) Extinction Ratio (ER in dB), (b) Contrast Ratio (CR in dB), and (c) Relative Eye opening (%) versus control energy for injection currents of 190 mA, 210 mA, and 220 mA. These plots correspond to the FRG output Q, which functions as the primary output of the 2×1 multiplexer. The results clearly indicate improved optical performance with increasing bias current, with performance saturation observed beyond 30pJ due to gain compression and carrier heating effects

multiplexer implementations explicitly based on Reflective Semiconductor Optical Amplifiers (RSOAs) have not been reported in the existing literature, in either reversible or conventional domains. Therefore, a direct comparison with RSOA-based multiplexers is not feasible. The proposed design is consequently compared with state-of-the-art optical multiplexers realized using alternative photonic technologies, while reversibility and RSOA-based implementation are highlighted as key novel contributions of this work.

Additionally, the impact of RSOA input current on optical performance was investigated comprehensively. Figure 24 shows the variation in ER, CR, and REOP as a function of control energy ranging from 10 fJ to 100 fJ, across different bias currents (190 mA, 210 mA, and 220 mA). The results indicate that increasing the bias current enhances ER, CR, and REOP due to stronger carrier modulation and improved gain response. However, a saturation in performance was observed beyond 40 fJ, likely due to gain compression and carrier heating effects. These observations underscore the importance of optimizing both control energy and bias current to achieve energy-efficient and robust optical logic performance in RSOA-based circuits.

Overall, the simulation results affirm that the proposed FRG–XGM–RSOA framework offers a promising foundation for scalable, ultrafast, and low-loss photonic computing.

5 Conclusion

In this work, a reversible 2×1 multiplexer based on the Fredkin Reversible Gate (FRG) was proposed and utilized to implement a set of fundamental logic gates along with half-adder and half-subtractor circuits, making this work the first reported RSOA-based reversible multiplexer-centric optical logic framework. The simulation results confirmed high ER, CR, and REOP values, indicating the suitability of the design for high-speed and low-loss optical logic applications. While the ER and CR values are slightly lower than those reported[45,49], the proposed design offers significant advantages in terms of compactness and reversibility—an aspect absent in micro ring- and MZI- based multiplexer designs.

Reversibility in optical circuits contributes to energy-efficient computation by preserving information and minimizing energy dissipation, making it highly relevant for emerging photonic computing platforms. The analysis of varying RSOA input current and control energy further demonstrated the performance scalability of the design, with clear improvements in optical metrics up to saturation thresholds. These results validate the potential of the FRG-XGM-RSOA framework as a promising approach for scalable, ultrafast, and energy-efficient photonic logic integration.

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