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Design Voltage-Controlled Oscillator using I-MOS Varactor for Selective Tuning for UHF Band Applications

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To optimize frequency tuning, noise performance, and power efficiency under various process, voltage, and temperature (PVT) conditions, the study investigates the design, implementation, and evaluation of two novel voltage-controlled oscillators (VCOs) for Ultra High Frequency (UHF) applications. The first design is a 180-nm CMOS, five-stage Current-Starved Voltage Controlled Oscillator (CSVCO) with improved tuning via an Inversion mode MOS (I-MOS) varactor. Fine-grained frequency modulation is made possible by an exact bias current control method. Monte Carlo simulations and extensive PVT analysis verify the circuit's robustness. Power-sensitive applications benefit greatly from the CSVCO's broad tuning range (0.119–2.91 GHz), low power consumption (1.16 mW), and phase noise of -91.80 dBc/Hz at a 1 MHz offset.

In order to improve tuning and spectrum purity, the second design is an LC-VCO with a current-controlled tail biasing structure. The LC tank balances low noise, efficiency, and stability for UHF wireless systems by improving phase noise, attaining -128.37 dBc/Hz at 1 MHz offset throughout a tuning range of 2.418–2.439 GHz with a 5.66 mW power consumption.

These ideas improve the efficiency and dependability of contemporary UHF circuits by introducing innovative tuning methods and optimizations.

Keywords: Current Starved, Delay stage, I-MOS, Monte Carlo, PVT analysis, Varactor, VCO

1 Introduction

In contemporary wired and wireless communication systems, the voltage-controlled oscillator (VCO) is essential[1]. With the growing need for wireless PDAs with high precision and low power consumption, RF designers face many technological obstacles[2]. Recent developments show that VCOs are being carefully developed to suit these expectations. Additional parasitic capacitance decreases bandwidth and increases chip area[3]. Usually, switched capacitor banks or switched inductors are used to tune wide-band VCO integrated circuits. These circuits use transistors as switches, each of which is controlled by a different digital voltage[4]. Moreover, large tuning ranges have been achieved by using switched active cores, which necessitates multiple control voltages for each switch. Varactors or varactor banks are often added to these methods for coarse and fine frequency adjustments to get around the discrete frequency tuning limitations of switches.

Using a switched capacitor bank, switched inductor, and varactors, a previous study required 64 possible combinations of digital control signals for coarse tuning and an analog control voltage adjustment for fine-tuning[5]. Another method introduced complexity and possible frequency coverage gaps by using dual cores with 10 control voltages for frequency adjustment. In recent years, considerable attention has been given to achieving a broad tuning range, low power consumption, and reduced phase. Noise in inductance-capacitance voltage-controlled oscillator (LC-VCO). Achieving high-tuning linearity, however, has received comparatively less attention.

Recent advancements in voltage-controlled oscillator (VCO) design highlight the rise of hybrid architectures that integrate both analog and digital tuning methods. For example, digitally controlled oscillators (DCO) hybrids now use fractional-N phase-locked loops (PLLs) to deliver jitter performance below 100 femtoseconds in 5G millimeter-wave applications. Meanwhile, the use of MEMS-based reconfigurable inductors has demonstrated a 35% increase in tuning within 28 nm CMOS technology. Novel materials such as ferroelectric hafnium-zirconium oxide (HZO) are also gaining attention for their ultra-linear capacitance-voltage (C-V) characteristics, enabling 2–3 dB reductions in phase noise. Looking ahead, future developments are expected to be AI-assisted self-calibration systems, where machine learning algorithms dynamically adjust the

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VCO gain (Kvco) for manufacturing variations[5-6]. Additionally, terahertz VCOs built on III-V compound semiconductors are being explored for 6G network systems. In the IoT space, ultra-low-power VCOs are aiming to operate under 100 μW by employing piezoelectric-based tuning mechanisms that support energy harvesting.

The VCO gain (K_{vco}) is one significant parameter that has a significant impact on phase noise, frequency lock range, and loop stability. Several methods have been suggested by earlier research to address this, such as using differently biased varactor banks and integrating varactor banks inside the LC tank[7].

To keep K_{vco} constant, varactor arrays or linear MOS varactor banks have become popular. Additionally, the varactor's main structure in LC-VCO circuits has gradually been standardized throughout research studies[8–11].

VCOs play a crucial role in today's high-speed communication systems, contributing significantly to phase/frequency synchronization circuits while also being essential in generating phase noise and jitter [12].

These versatile components extend their application to medical equipment such as MRI, ultrasound, and wireless data telemetry[13-15]. Designing VCOs for modern communication devices presents a considerable challenge, demanding a balance between a broad tuning range, low power consumption, and compact size.

To meet the demands of modern communication devices, choosing the right VCO architecture is crucial. While an ideal VCO should provide an infinite tuning range and zero phase noise, achieving this is challenging. The performance of VCOs is typically assessed based on tuning spectrum and phase noise.

1.1 Research Gap and Motivation

For contemporary communication systems, Voltage-Controlled Oscillators (VCOs) must be designed and optimized. Current-Starved VCOs (CSVCOs) and cross-coupled LC VCOs are two well-known topologies that offer special difficulties as well as chances for improvement. Because of their dependence on ring oscillator architecture, CSVCOs have high phase noise, which makes design strategies to improve signal integrity, like using D Flip Flops to lower jitter—necessary. Furthermore, reducing power consumption is essential for portable devices, which motivates research into better CMOS scaling and low-power circuit approaches. Achieving a broad and linear frequency tuning range in CSVCOs is another difficulty that calls for creative linearization strategies to guarantee system component compatibility. In contrast, cross-coupled LC VCOs inherently offer better phase noise performance but require further reduction for high-frequency applications, with techniques like post-fabrication selection of cross-coupled transistors achieving significant improvements. The integration of high-Q inductors and capacitors remains a research focus to enhance LC VCO performance without design trade-offs, while ensuring stable start-up conditions through negative resistance and feedback approaches is essential for reliable operation. Addressing these research gaps in phase noise reduction, power efficiency, frequency tuning linearity, and integration of high-quality passive components will be instrumental in developing VCOs that meet the stringent requirements of modern high-speed communication systems.

2 Ring Voltage Controlled Oscillator

Figure 1 illustrates the two primary types of integrated oscillators: ring oscillators and LC oscillators. LC oscillators provide excellent in phase noise performance but suffer from a limited tuning range. In contrast, ring oscillators are favored for their compact chip size and low power consumption, though they exhibit poorer noise performance[16].

2.1 Design Considerations for Ring VCO

2.1.1 Oscillation Condition

For a Ring VCO to sustain oscillation, its open-loop transfer function must fulfill the Barkhausen criteria, as specified in Eq (1):

$$|H(j\omega_0)| \geq 1$$
$$|\angle H(j\omega_0)| = 2\Pi \quad \ldots (1)$$

In this context, the symbol ω_0 denotes the angular frequency of the oscillator in a fully closed loop,

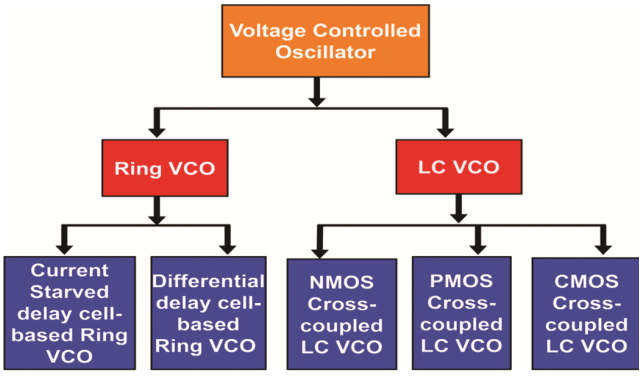

Fig. 1 — Classification of voltage-controlled oscillators

meeting the specified conditions in equation (1). Notably, configurations with an odd number of stages consistently fulfil the oscillation criterion[17].

2.1.2 Oscillation Frequency

The ring oscillator's period is defined by the signal transition propagation time (t_d) across the entire chain, as indicated by Eq (2):

$$T = 2 \times N \times t_d \quad \ldots (2)$$

N represents the chain's total number of inverters (delay stages). Completing a full cycle requires transitions from low to high and high to low, thus resulting in a factor of 2. Equation (2) holds only under the condition $2 \times N \times t_d >> t_r + t_f$ where t_r and t_f denote the rising and falling periods. Consequently, the oscillation frequency (f_o) can be expressed as per Eq (3):

$$f_0 = \frac{1}{T} = \frac{1}{2 \times N \times t_d} \quad \ldots (3)$$

Therefore, it is possible to tune the oscillation frequency of an N-stage ring oscillator by modifying the time delay of each stage[18].

2.2 I-MOS Varactor

Inversion-mode (I-MOS) varactors enable precise frequency tuning in voltage-controlled oscillators (VCOs) by varying their capacitance through gate-voltage-induced inversion layers. Applying a voltage to the gate of a MOS structure induces an inversion layer of minority carriers—electrons in NMOS or holes in PMOS—at the oxide-semiconductor interface. This affects the capacitance between the gate and other terminals (drain, source, or substrate). Incorporated into the LC tank of the VCO, this variable capacitance directly affects the resonant frequency: a higher capacitance leads to a lower oscillation frequency, while a lower capacitance increases it. This mechanism allows for a larger tuning range, improved linearity, and lower operating voltage, making it ideal for RF circuits, such as voltage-controlled oscillators (VCOs), phase-locked loops (PLLs), and tunable filters. Its compatibility with CMOS technology facilitates integration into modern ICs, making it a promising solution for next-generation communication systems, including 5G and millimeter-wave applications. However, challenges such as excess noise and nonlinearity require careful design considerations. Overall, the I-MOS varactor is a valuable advancement in tunable capacitor technology, addressing the growing demand for high-performance, low-power tunable components in advanced communication systems[4].

2.3 Design of Current Starved VCO using I-MOS varactor

An oscillator circuit where the oscillation frequency can be adjusted by varying the voltage input is called a current-starved voltage-controlled oscillator, VCO. It functions by adjusting the current supplied to the oscillator at each step, which modifies the delay time and oscillation frequency. Precise frequency tuning is made possible by modulating the amount of current passing through the oscillator stages through changes in the control voltage. Applications requiring tunable oscillation frequencies, like phase-locked loops, frequency synthesizers, and communication systems, frequently use this design. A five-stage voltage-controlled oscillator is part of the suggested Current Starved VCO design that uses an I-MOS varactor. It has one buffer stage shown in Fig. 2 (b) and delay

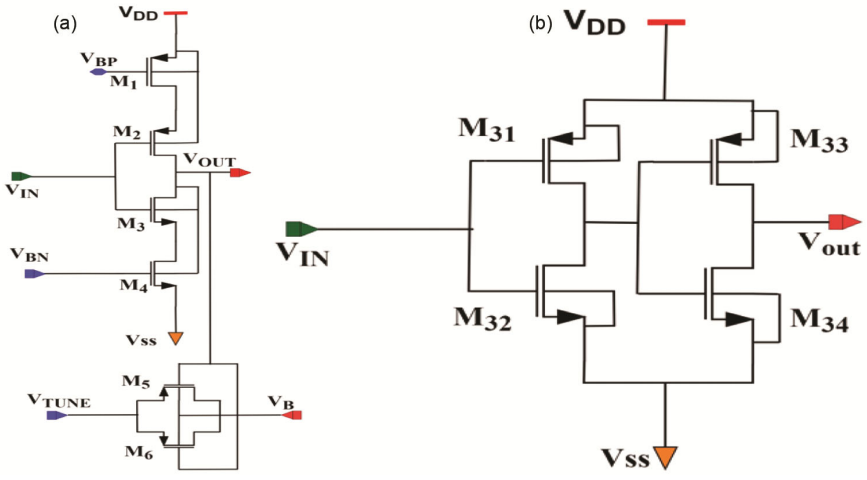

Fig. 2 — (a) The delay stage of the current-starved voltage-controlled Oscillator, and (b) Buffer stage of the current-starved voltage-controlled oscillator.

stages shown in Fig. 2 (a). Figure 3 shows the circuit diagram of a 5-stage current-starved voltage-controlled oscillator using I-MOS, and Fig. 4 shows the block diagram of a 5-stage current-starved voltage-controlled oscillator. While the current-starved voltage-controlled ring oscillator uses cascaded inverter stages to oscillate, it differs from a traditional ring oscillator in that it can be adjusted by varying the control voltage (V-control),

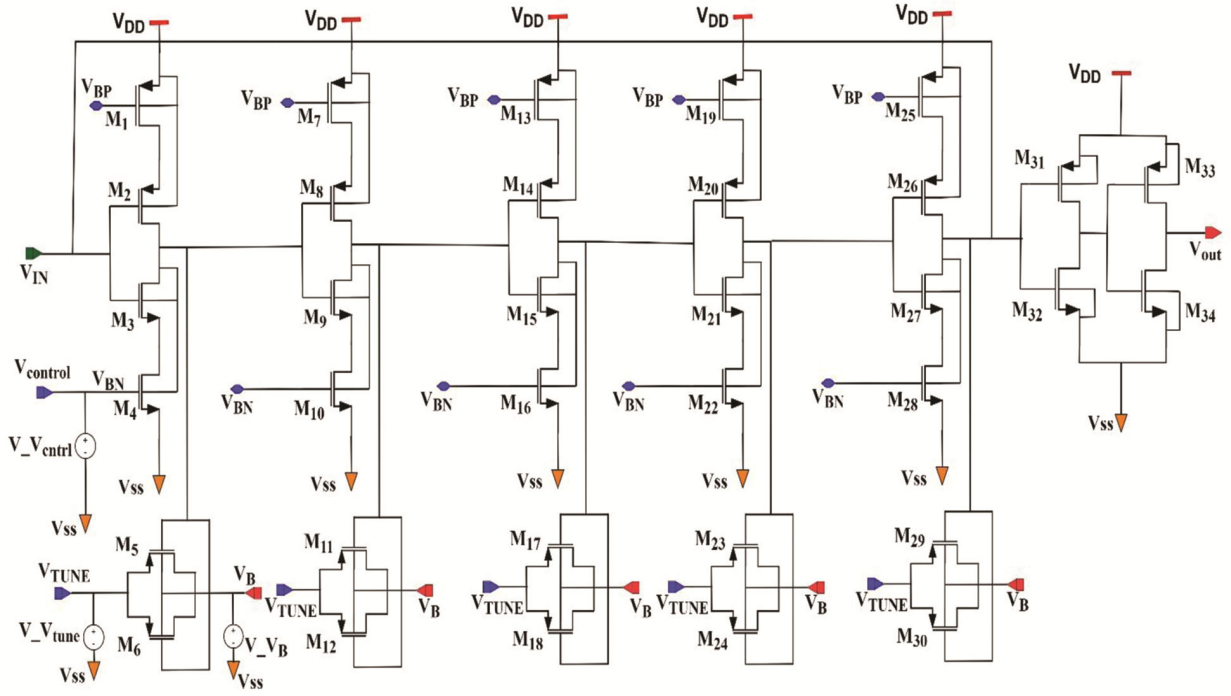

Fig. 3 — Circuit diagram of 5-Stage current-starved voltage-controlled oscillator using I-MOS

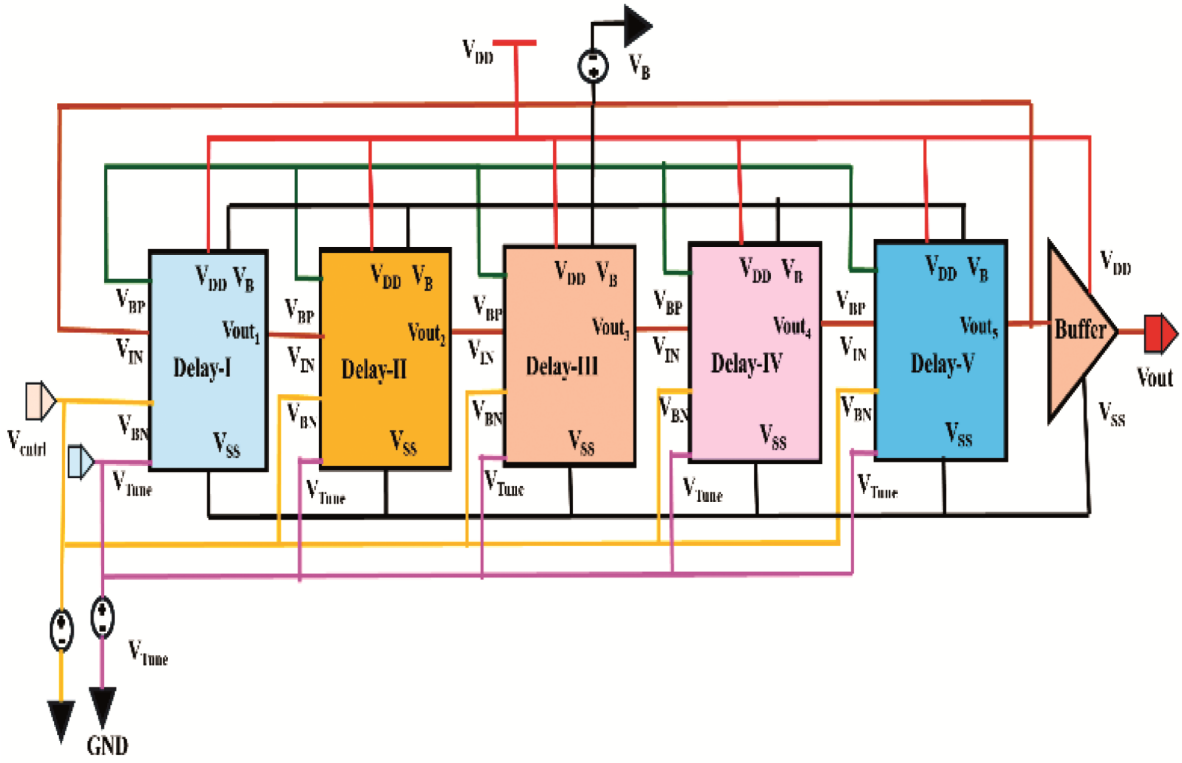

Fig. 4 — Block diagram of 5-Stage current-starved voltage-controlled oscillator using I-MOS

as shown in Fig. 3, to change the delay time of each inverter stage and, in turn, the oscillation frequency. Modulating the current that charges or discharges the load capacitance of each inverter stage allows for this adjustment.

In this circuit arrangement, referred to as a current-starved voltage-controlled ring oscillator, the quantity of current passing through each stage holds significance. Increased control voltage permits a higher current flow, diminishing resistance and reducing delay. Figure 2 (a) depicts the roles of transistors M_1 and M_4, acting as a current source and sink, respectively, to control the current provided to the inverter stage.

The amount of current available to the inverter stage is essentially controlled by the current sink transistor M_4 and the current source transistor M_1. Because of this configuration, the inverter is "starved" for current, which means that the controlled current flow limits how well it operates. To ensure a balanced current distribution, the NMOS transistor M_4 and PMOS transistor M_1 first supply current to the inverter stage via a current mirror circuit. The voltage-controlled oscillator (VCO) can have its frequency tuning range modified and its linearity improved by varying the control voltage[19]. There are disadvantages to this strategy, though. The voltage swing in the VCO rises and falls over longer periods when the biasing current is low. On the other hand, a higher bias current causes the current source MOS transistors' voltage headroom to decrease [20]. The VCO's overall performance may be impacted by this decrease in voltage headroom.

To enable frequency tuning, this study makes use of MOS varactors operating in inversion mode. Altering the voltage across the varactor modifies its capacitance. When an NMOS or PMOS transistor is in inversion mode, its bulk terminal is connected to either the circuit's highest or lowest voltage, respectively. Positioned at the output of each stage, these MOS varactors serve as variable load elements. Manipulating the load component enables the proposed VCO to achieve a wider range of tunable frequencies.

The oscillation frequency can be calculated by considering the combined capacitance on the drain's regions of transistors M_3 and M_4. This capacitance significantly influences the oscillation frequency of the VCO [21].

Equations (4 - 6) give the total capacitance on the drain terminal for a simplified single-stage inverter circuit as follows:

$$C_{tot} = C_{out} + C_{in} \quad \ldots (4)$$

$$C_{tot} = C_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C_{ox}(W_p L_p + W_n L_n) \quad \ldots (5)$$

$$C_{tot} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n) \quad \ldots (6)$$

C_{tot} stands for the total capacitance of the single delay stage, where C_{out} is the output capacitance and C_{in} is the inverter's input capacitance. The terms W_p, L_p, W_n, and L_n denote the P- and N-MOSFETs' respective widths and lengths.

Equation (7) provides a common expression for the oscillation frequency of an N-stage current-starved voltage-controlled oscillator (CSVCO):

$$f_{osc} = \frac{I_D}{V_{DD} \times N \times C_{tot}} \quad \ldots (7)$$

Where I_D represents the drain current, N denotes the number of stages, C_{tot} signifies the total capacitance, and V_{DD} stands for the supply voltage. Table 1 displays the transistor sizing of the CSVCO utilizing I-MOS.

3 Design of Cross-Coupled LC Oscillator using I-MOS Varactor

The cross-coupled LC-tank oscillator is widely used in digital isolators, isolated power supplies, and transceivers, among many other fully integrated electronic devices[22-24]. Two popular configurations are the NMOS cross-coupled and NMOS/PMOS complementary cross-coupled designs. A center-tapped inductor is typically required for NMOS cross-coupled LC-tank oscillators, and this is frequently accomplished by using two consecutive inductors. However, the NMOS/PMOS complementary cross-coupled LC-tank oscillator requires a single inductor, saving a substantial amount of chip area. Therefore, the NMOS/PMOS complementary cross-coupled

Table 1 — Displays the transistor sizing of the CSVCO utilizing I-MOS

Transistor	Width	Length (nm)
$M_1, M_7, M_{13}, M_{19}, M_{25}$	5 µm	180
$M_2, M_8, M_{14}, M_{20}, M_{26}$	1.75 µm	180
$M_3, M_9, M_{15}, M_{21}, M_{27}$	700 nm	80
$M_4, M_{10}, M_{16}, M_{22}, M_{28}$	700 nm	80
$M_5, M_{11}, M_{17}, M_{23}, M_{29}$	500 nm	80
$M_6, M_{12}, M_{18}, M_{24}, M_{30}$	500 nm	80
M_{31}, M_{33}	1.75 µm	80
M_{32}, M_{34}	700 nm	180

LC-tank oscillator is suggested for applications requiring strict area constraints[25].

3.1 Cross-Coupling

Figure 5 depicts a VCO that is a complementary NMOS-PMOS cross-coupled LC. In this design, cross-coupled pairs from PMOS and NMOS are integrated. Since the bias current that flows through PMOS and NMOS devices is the same, efficiency increases twice for a given power consumption when negative resistance is employed. The combined negative resistance of the NMOS-PMOS cross-coupled structure can be represented by the parallel combination of the NMOS and PMOS negative resistances Eq (8), referred to as R_{inn} and R_{inp}, respectively[26].

$$R_{negative} = R_{inn} \parallel R_{inp} = \frac{-2}{g_{mn} + g_{mp}} = \frac{-2}{g_m} \quad \ldots (8)$$

As shown in Eq (8), g_{mn} and g_{mp}, respectively, stand for the transconductance of the NMOS and PMOS cross-coupled transistors. Due to the NMOS and PMOS transistors operating in a mutually switching scheme for half of the arrangement's duration, the voltage amplitude across the LC tank is raised[27]. The design incorporates negative resistance in the cross-coupled transistors to offset the losses associated with the LC tank. To sustain oscillation, a tail current is employed to maintain a negative resistance level with an absolute value smaller than the equivalent tank loss, effectively suppressing flicker and thermal noise[28].

To achieve a linear oscillation design, it is imperative to adhere to the following conditions[29]:

If R_{tank} is greater than $R_{negative}$, oscillations will attenuate.
If R_{tank} is less than $R_{negative}$, oscillations will amplify.
If R_{tank} equals $R_{negative}$, it ensures the sustenance of a constant oscillation amplitude.

3.2 VCO Modeling

Figure 5 shows the configuration of the suggested cross-coupled LC-VCO. An LC tank and a cross-

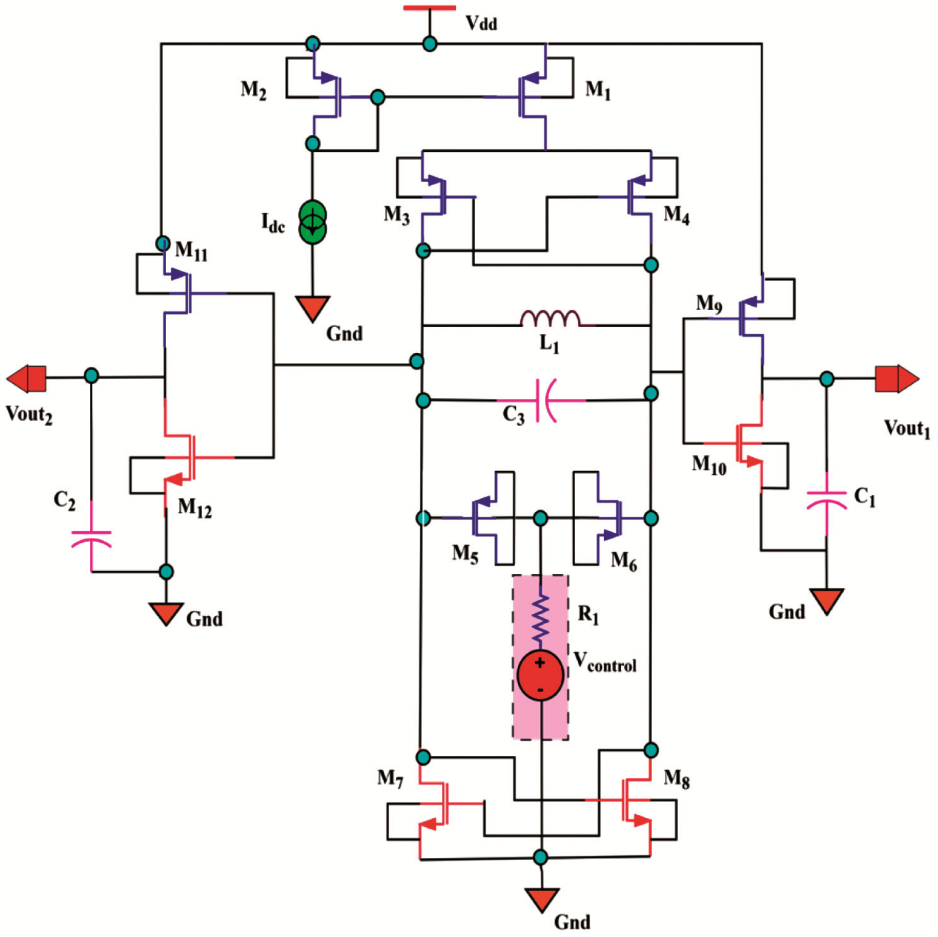

Fig. 5 — Cross-coupled LC oscillator using I-MOS

coupled complementary VCO are part of this setup. A PMOS current mirror facilitates biasing by effectively channeling the current towards the LC-VCO. Choosing a PMOS structure over an NMOS structure of the same size is motivated by its better flicker noise performance[30]. Cross-coupled transistors offer crucial negative feedback, and the complementary P-MOSFET, N-MOSFET structure boosts

VCO transconductance while keeping the quiescent drain current I_D constant, where Eq (9) below:

$$I_{bias} = 2 \times I_D \quad \ldots (9)$$

The cross-coupled voltage-controlled oscillator (VCO) depicted in Fig. 5 consists of an LC tank circuit and a cross-coupled transistor pair that enables stable oscillations. The LC tank, composed of inductors and capacitors, sets the circuit's resonant frequency. The cross-coupled transistor pair generates negative resistance, counteracting energy losses in the tank circuit to maintain continuous oscillations. Frequency tuning is achieved using varactor diodes, where an applied voltage controls their capacitance, enabling fine adjustments to the oscillation frequency. Biasing elements, like current sources or resistors, establish the proper operating point for the transistors. Output coupling components, usually capacitors, facilitate the transfer of the oscillation signal to other circuit elements while preserving the integrity of the LC tank. Table 2 presents cross-coupled LC-VCO component parameters. This VCO design is crucial for applications that demand tunable and stable frequency output, such as frequency modulation or synthesis in phase-locked loops for RF communication systems. The oscillation frequency of the proposed VCO is given in Eq (10), which represents the natural frequency of an LC circuit, determined by the relationship between inductance and capacitance. The LC tank circuit functions on the principle of energy exchange between the inductor's magnetic field and the capacitor's electric field. When the capacitor discharges, the inductor stores energy in its magnetic field, and vice versa, leading to oscillations at the resonance frequency.

Table 2 — Component value of LC -VCO

Device Component	Value
M_1 to M_4	W=10 µm
M_5 and M_6	W=600 n
M_7 to M_9 and M_{11}	W=5 µm
M_{10} and M_{12}	W=2.5 µm
L_1	9.25 nH
C_1 and C_2	53 fF
C_3	414.08 fF
R_1	50 Ω
I_{dc}	2.25 mA
V_{DD}	1.8 V
$V_{control}$	1 V

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind} \times C_{tank}}} \quad \ldots (10)$$

And

$$g_{tank} \leq \frac{g_{m,p}}{2} + \frac{g_{m,n}}{2} = g_m \quad \ldots (11)$$

Where,

$$C_{tank} = C_{var} + \frac{C_P MOS + C_n MOS}{2} + C_{load} \quad \ldots (12)$$

$$g_{tank} = g_{ind} + g_{var} + \frac{gds,p}{2} + \frac{gds,n}{2} \quad \ldots (13)$$

Taking into account the output conductance of the N-MOSFET and P-MOSFET transistors as $g_{ds,n,}$ and $g_{ds,p}$, respectively, and the parasitic conductance of the inductor and varactor as $g_{ind} = 1/R_{ind}$ and g_{var}, within the context of the five-capacitance model of the MOSFET, Eqs (11-14) represents the g_{tank}, C_{tank}, $g_{tank,}$ and equivalent cross-coupled transistor capacitance, respectively, which applies to both N-MOSFET and P-MOSFET.

$$C_{MOS} = 4C_{gd} + (C_{gs} + C_{gb} + C_{db} + C_{ds}) \quad \ldots (14)$$

3.3 Optimization of an LC Voltage-Controlled Oscillator

Optimizing an LC Voltage-Controlled Oscillator (VCO) requires carefully balancing key performance metrics, including frequency range, phase noise, power consumption, and tuning linearity. The first step in this process is defining the target oscillation frequency, which is primarily dictated by the LC tank circuit. Choosing high-quality inductors and capacitors is critical to achieving the desired resonance frequency while minimizing losses. This, in turn, helps reduce phase noise, a crucial factor in VCO performance.

After selecting the LC components, the varactor diode responsible for frequency tuning must be carefully optimized. To achieve a broad and linear tuning range, it is crucial to balance tuning sensitivity with frequency span. This balance ensures stable oscillations across the desired frequency range while adapting to variations in control voltage.

Bias current and transistor sizing are crucial factors in optimizing LC-VCO performance. Carefully adjusting the bias circuitry minimizes power

consumption while ensuring adequate oscillation amplitude. Furthermore, adjusting transistor sizes minimizes flicker noise, resulting in better phase noise performance.

Advanced design techniques, like differential topologies, can significantly boost performance by reducing common-mode noise and enhancing signal integrity. Furthermore, meticulous layout practices such as minimizing parasitic components and reducing substrate noise coupling — are essential for achieving optimal performance in practical applications. Lastly, comprehensive simulation and iterative fine-tuning are crucial to ensuring the design meets performance standards across process, voltage, and temperature (PVT) variations.

The LC-VCO design process follows a systematic and iterative approach to satisfy critical performance targets, such as tuning range, power consumption, supply voltage, and phase noise. It starts with establishing user requirements, which inform the initial selection of critical components like transistors, varactors, and inductors[50-51].

The next step involves optimizing transistor design to achieve a balance between low power consumption and stable oscillation characteristics. The varactor and inductor are carefully adjusted to extend the tuning range and reduce phase noise. A feasibility check is conducted to verify that the initial design meets critical performance criteria. If required, parameters are adjusted, and the process is repeated to further refine the design.

Optimization is further improved through equation-based methods, which use analytical expressions to link component values with performance parameters. After the design passes the feasibility and specification validation stages, it is finalized and prepared for layout, fabrication, and testing. This iterative process ensures the LC-VCO achieves optimal tuning range, phase noise, power efficiency, and reliability for its intended application, as illustrated in Fig. 6.

4 Results and Simulation Analysis

The designs of CSVCO and LC-Voltage Controlled Oscillators (VCOs) are demonstrated in Cadence's Virtuoso analog design environment with 180nm CMOS technology to showcase their functionality.

4.1 Layout Design of VCOs

The layout design of a current-starved VCO demands meticulous attention to symmetry, parasitic reduction, noise isolation, and power supply routing. Proper placement of components, especially transistors and current mirrors, is essential to ensure uniform current control across the VCO stages. Techniques like implementing guard rings, deep n-well isolation, and precise control voltage routing can greatly enhance noise immunity and improve phase noise performance. Following these best practices in layout design optimizes the current-starved VCO's performance, ensuring reliable operation in integrated circuits. Figure 7 (a) shows the layout design of the proposed current-starved voltage-controlled oscillator, covering an area of 58.605 × 51.545 μm².

Designing the layout of a VCO is a complex task that requires careful attention to several key factors, including parasitic minimization, noise isolation, power supply integrity, and symmetry. Adopting best practices — such as optimizing LC tank placement, incorporating noise shielding, and ensuring efficient signal routing — can greatly enhance VCO performance, leading to reduced phase noise, a broader tuning range, and improved frequency stability. Considering that these layout techniques are essential to meet the strict design specifications of high-frequency applications. Figure 7 (b) presents the layout design of the proposed cross-coupled LC-VCO, covering an area of 572.325 × 405.610 μm².

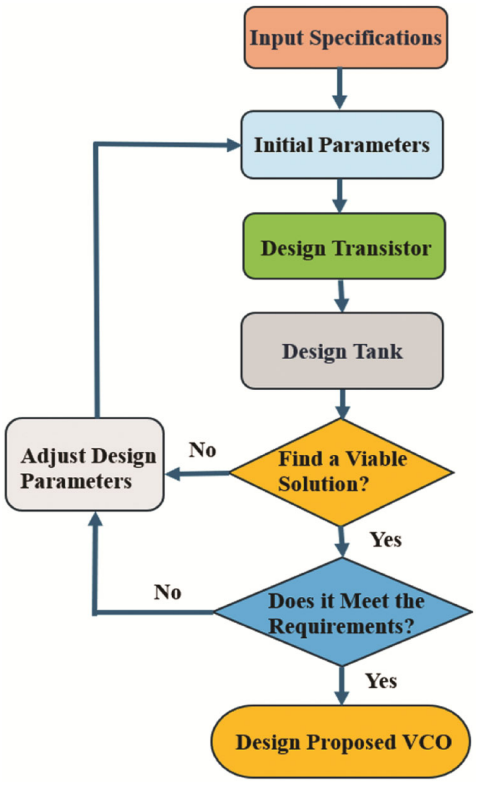

Fig. 6 — Design flowchart of proposed design

4.2 Transient Analysis

Figure 8 (a - b) show the transient analysis of Current current-starved VCO and the cross-coupled LC VCO, respectively. At supply voltage 2.4 V, CSVCO oscillates between 0 V to 2.4 V, and at supply voltage 1.8 V LCVCO oscillates between -0.01 V to 1.778 V.

4.3 Process Corner Analysis

Process Corner Analysis is a critical component of integrated circuit (IC) design and verification. It helps ensure that a design meets both performance and reliability standards across a range of manufacturing and environmental fluctuations. This analysis involves simulating and evaluating the performance of an IC under varying process, voltage, and temperature conditions, often referred to as PVT variations [31-33].

Process corners refer to specific points representing different variations in the semiconductor fabrication process. These variations occur because it is challenging to achieve perfect control during manufacturing, resulting in minor deviations in the properties of transistors and other components. To assess how a

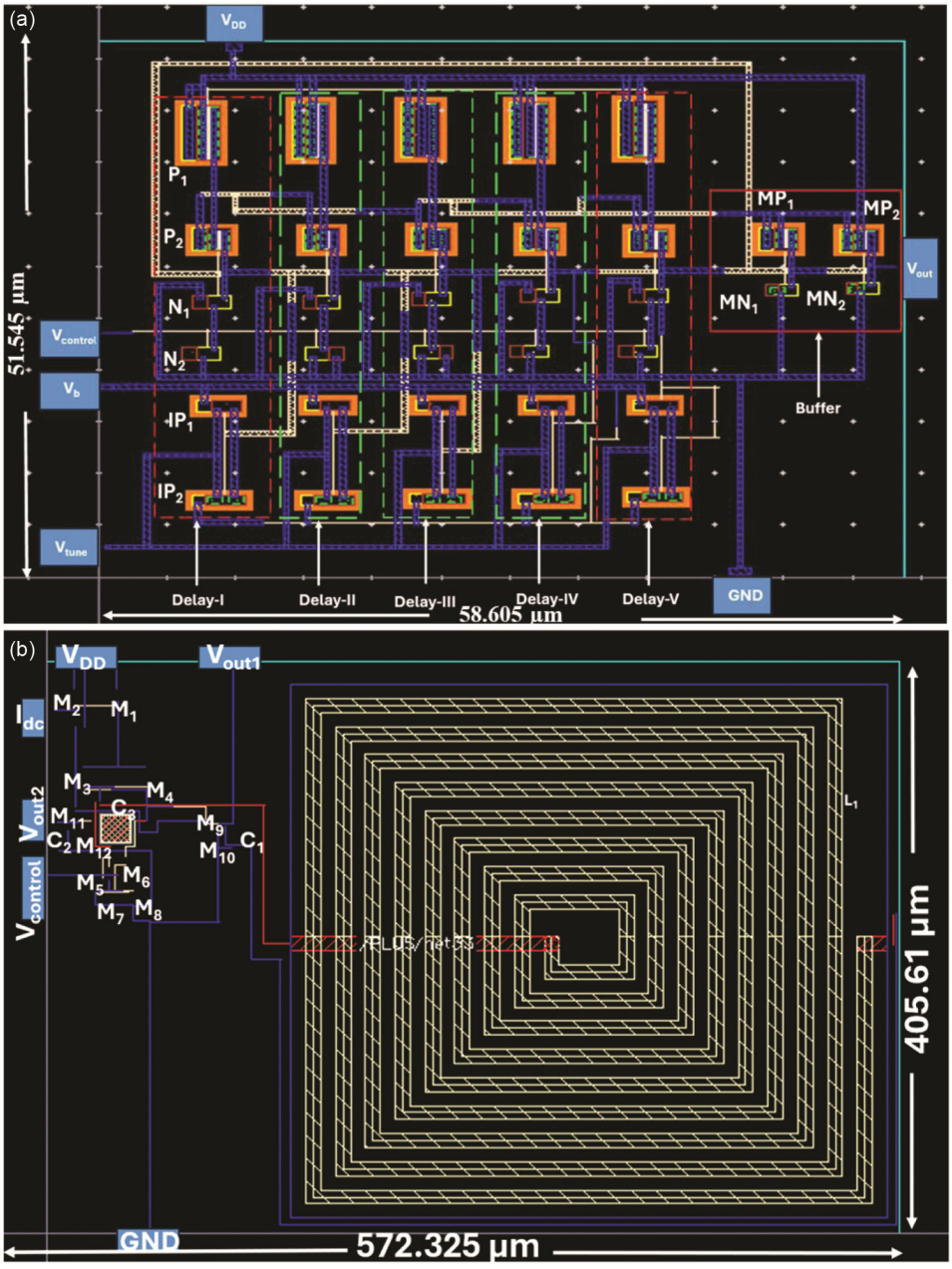

Fig. 7 — Layout of (a) Current-starved VCO, and (b) Cross-coupled LC-VCO

circuit performs under optimal, worst-case, and nominal conditions, engineers use process corners. The five most common process corners include:

Typical-Typical (TT) or Nominal-Nominal (NN): Represents the average or nominal behavior of devices when manufactured. This is the baseline corner where all process parameters (e.g., transistor thresholds, oxide thicknesses) are within normal limits.

Slow-Slow (SS): Both NMOS and PMOS transistors are slower than average, representing the worst-case scenario for speed but the best-case for power consumption.

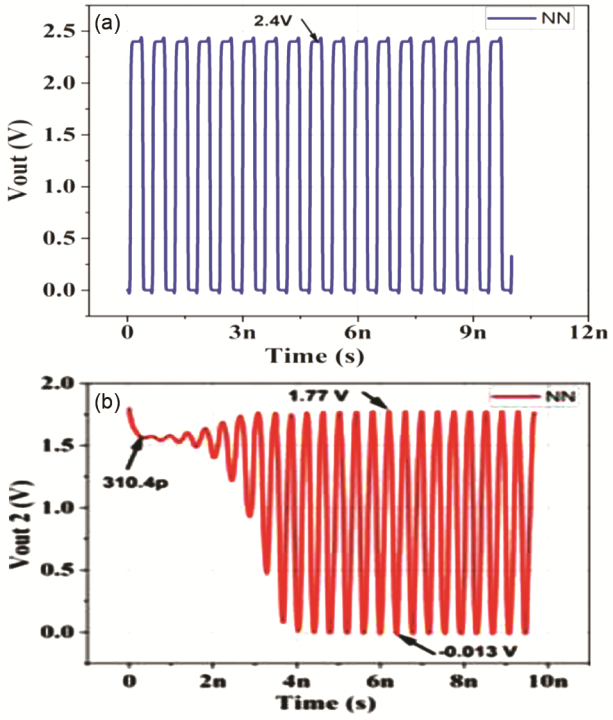

Fig. 8 — (a) Transient Analysis of Current Starved VCO, and (b) Transient Analysis of LC VCO

Fast-Fast (FF): Both NMOS and PMOS transistors are faster than average, representing the best case for speed but the worst case for power consumption.

Fast-Slow (FS): The NMOS transistors are faster than average, while the PMOS transistors are slower. This corner highlights any imbalances between the transistor types.

Slow-Fast (SF): The NMOS transistors are slower, and the PMOS transistors are faster. Like FS, this corner emphasizes imbalances in transistor behavior.

These variations can significantly affect the performance of ICs, including timing, power, and reliability metrics.

Figure 9 (a) illustrates the output frequency variations for all process corners as a function of the tuning voltage in the Voltage-Controlled Current-Starved Oscillator (CSVCO). The frequency range for the FF corner is from 0.673 GHz to 2.905 GHz. The frequency ranges for the FS, NN, SF, and SS corners are 0.526 GHz to 2.48 GHz, 0.326 GHz to 2.45 GHz, 0.119 GHz to 2.42 GHz, and 0.711 GHz to 2.057 GHz, respectively. The Fast-Fast (FF) process corner achieves the highest frequency performance, reaching up to 2.91 GHz at 3.0V, due to the significantly increased carrier mobility of both NMOS and PMOS transistors compared to other process corners, as shown in Fig. 9 (a). This improved mobility enables faster transitions by accelerating the charging and discharging of parasitic capacitances, leading to shorter gate delays and faster switching. As a result, devices at the FF corner have higher resonance frequencies. However, this performance boost comes at the cost of increased power consumption, driven by leakage currents that are nearly 30 times larger than those in the Slow-Slow (SS) corner.

In Fig. 9 (b), the power consumption for each of the five process corners is depicted, showing that the FF

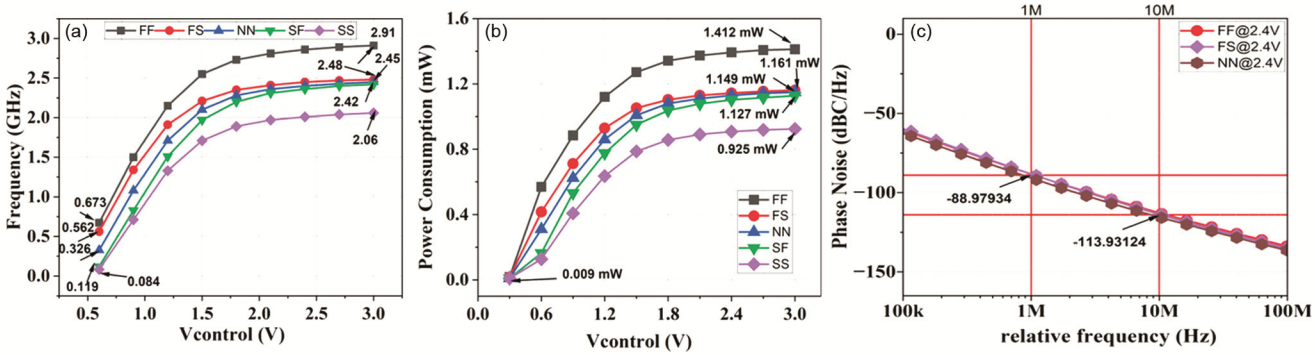

Fig. 9 — variation in (a) frequency, (b) power consumption, and (c) phase noise as a function of the tuning voltage across different process corners for the Voltage-Controlled Current-Starved Oscillator (CSVCO)

corner uses the most power at 1.412 mW compared to the others. Additionally, Fig. 9 (c) presents the phase noise performance, where the FF corner exhibits the worst phase noise at -83.879 dBc/Hz, while the NN corner shows the best phase noise performance at -91.802 dBc/Hz. The difference in phase noise performance between the FF and NN corners can be attributed to variations in process, voltage, and temperature (PVT) conditions. In the FF (fast-fast) corner, transistors tend to have higher speeds and lower threshold voltages, which can lead to increased current noise and reduced device control, thus worsening phase noise. Conversely, the NN (nominal-nominal) corner represents typical conditions where transistor performance is more balanced, resulting in lower noise generation and improved phase noise performance. This explains why the NN corner exhibits the best phase noise, while the FF corner shows the worst.

Table 3 presents the frequency and power consumption (P_{DC}) variations of the current-starved voltage-controlled oscillator (CSVCO) across different process corners—Fast-Fast (FF), Fast-Slow (FS), Nominal-Nominal (NN), Slow-Fast (SF), and Slow-Slow (SS)—for control voltages (Vcontrol) ranging from 0.6V to 3V. The FF corner exhibits the highest frequency performance, reaching 2.91 GHz at 3V, but also has the highest power consumption (1.412 mW). Conversely, the SS corner shows the lowest frequency (2.06 GHz at 3V) and the least power consumption (0.9248 mW). The NN process, representing typical conditions, achieves a balanced frequency range from 0.326 GHz at 0.6V to 2.45 GHz at 3V, with power consumption increasing from 0.3101 mW to 1.149 mW. The SF and FS process corners demonstrate intermediate performance, with SF showing lower frequencies and FS slightly higher due to variations in transistor speed. In CSVCO, power consumption increases sharply with Vcontrol, with the FF corner consuming the most power due to higher switching speed, and SS the least. In the CSVCO, as Vcontrol increases, it boost current flow through the delay stages, causing to faster charging and discharging of load capacitances, which consequently raises power consumption from 0.009 mW to approximately 1.412 mW as shown in Fig. 9 (b). As the control voltage increases, frequency consistently rises across all process corners, while power consumption also increases but at different rates depending on the process variations. These results highlight the CSVCO's robustness in maintaining a broad tuning range and relatively low power consumption despite fabrication-induced variations.

Table 4 presents the frequency and power consumption variations of the LC-VCO across different process corners—Fast-Fast (FF), fast-Slow (FS), Nominal-Nominal (NN), Slow-Fast (SF), and Slow-Slow (SS)—for control voltages ranging from 0.3V to 3V. Unlike the CSVCO, the LC-VCO exhibits a much narrower frequency tuning range, with frequencies varying slightly around 2.429 GHz in the FF corner and decreasing to around 2.418 GHz in the SS corner. The process variations have minimal impact on frequency tuning, indicating the LC-VCO's strong frequency stability. In contrast, LCVCO shows a slight decrease or nearly constant power trend, where SS consumes the most and FF the lowest, due to bias current differences across corners. In the LC-VCO, a higher Vcontrol reduces the varactor capacitance in the LC tank, lowering the overall load capacitance. This decreases the bias current needed to sustain oscillations, resulting in reduced power consumption—from about 5.974 mW down to 5.169 mW as shown in Fig. 10 (b). Notably, frequency remains nearly constant for different control voltages, suggesting that the tuning range is

Table 3 — Frequency and Power Consumption of CSVCO at Process Corner variations

Vcontrol	FF		FS		NN		SF		SS	
	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}
(V)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)
0.6	0.673	0.5698	0.562	0.4161	0.326	0.3101	0.119	0.1644	0.71	0.1269
0.9	1.5	0.8849	1.34	0.7114	1.08	0.624	0.829	0.5317	0.711	0.4077
1.2	2.15	1.121	1.91	0.9296	1.71	0.8597	1.51	0.7756	1.33	0.6355
1.5	2.55	1.272	2.21	1.052	2.1	1.008	1.97	0.9501	1.71	0.7868
1.8	2.73	1.342	2.35	1.103	2.28	1.08	2.2	1.037	1.89	0.8574
2.1	2.81	1.374	2.41	1.129	2.36	1.11	2.31	1.078	1.97	0.891
2.4	2.86	1.393	2.45	1.144	2.4	1.129	2.36	1.102	2.01	0.9078
2.7	2.89	1.407	2.47	1.154	2.43	1.143	2.4	1.116	2.04	0.9189
3	2.91	1.412	2.48	1.161	2.45	1.149	2.42	1.127	2.06	0.9248

Table 4 — Frequency and Power Consumption of LC VCO at Process Corner variations

Vcontrol	FF		FS		NN		SF		SS	
	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}	Frequency	P_{DC}
(V)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)	(GHz)	(mW)
0.3	2.429	5.171	2.439	5.478	2.439	5.572	2.437	5.661	2.425	5.974
0.6	2.429	5.171	2.439	5.478	2.439	5.572	2.437	5.661	2.425	5.974
0.9	2.429	5.171	2.439	5.478	2.438	5.572	2.437	5.661	2.425	5.974
1.2	2.427	5.171	2.438	5.478	2.437	5.571	2.435	5.661	2.424	5.974
1.5	2.426	5.171	2.436	5.477	2.436	5.572	2.434	5.661	2.422	5.973
1.8	2.424	5.17	2.434	5.476	2.434	5.571	2.432	5.66	2.42	5.973
2.1	2.422	5.169	2.433	5.476	2.433	5.571	2.431	5.66	2.419	5.973
2.4	2.421	5.169	2.433	5.476	2.432	5.571	2.43	5.66	2.418	5.973
2.7	2.42	5.168	2.432	5.475	2.431	5.57	2.43	5.66	2.418	5.972
3	2.419	5.169	2.431	5.475	2.43	5.57	2.43	5.66	2.418	5.972

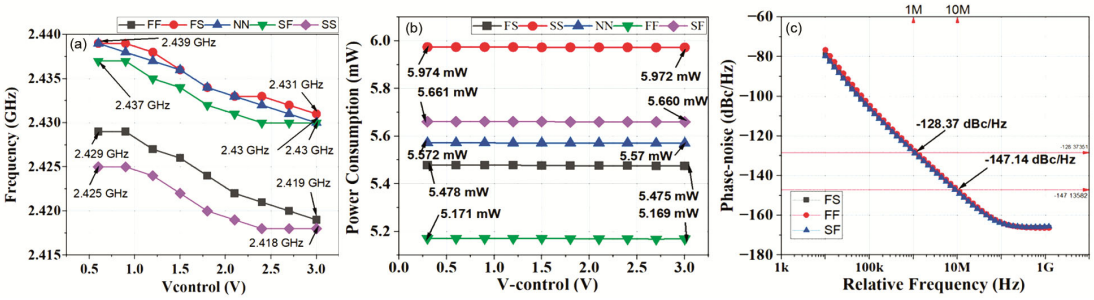

Fig. 10 — Variation in (a) frequency, (b) power consumption, and (c) phase noise with tuning voltage for different corners of the LC-VCO

highly constrained by the LC tank circuit. This table highlights the LC-VCO's excellent frequency stability across process variations but also its limited tuning capability compared to the CSVCO.

Figure 10 (a) illustrates the output frequency variations across all process corners as a function of the tuning voltage in the LC-VCO. In the SS corner, the frequency range spans from 2.425 GHz to 2.418 GHz. The frequency ranges for the FF, FS, NN, and SF corners are 2.429 GHz to 2.419 GHz, 2.439 GHz to 2.431 GHz, 2.439 GHz to 2.43 GHz, and 2.437 GHz to 2.43 GHz, respectively. Among these, the LC-VCO shows the widest tuning range in the FF corner.

Figure 10 (b) highlights power consumption across all four process corners, with the FS corner consuming more power than the others. Figure 10 (c) presents the phase noise performance for three corners, where the FF corner exhibits the worst phase noise among them.

Process corner analysis is an essential step in IC design, ensuring that the circuit maintains reliable performance across various manufacturing and environmental variations. By simulating different PVT conditions, designers can predict real-world behavior, improve reliability, enhance yield, and meet performance targets.

In CSVCO, power consumption increases sharply with Vcontrol, with the FF corner consuming the most power due to higher switching speed, and SS the least. In the CSVCO, as Vcontrol increases, it boosts current flow through the delay stages, causing faster charging and discharging of load capacitances, which consequently raises power consumption from 0.009 mW to approximately 1.412 mW as shown in Fig. 9 (b). In contrast, LCVCO shows a slight decrease or nearly constant power trend, where SS consumes the most and FF the lowest, due to bias current differences across corners. In the LC-VCO, a higher Vcontrol reduces the varactor capacitance in the LC tank, lowering the overall load capacitance. This decreases the bias current needed to sustain oscillations, resulting in reduced power consumption, from about 5.9 mW down to 5.2 mW as shown in Fig. 10 (b).

4.4 PVT Variations (Process, Voltage, Temperature)

In addition to the process variations, IC behavior is also affected by changes in voltage and temperature:

Voltage Variations: The supply voltage may vary from the nominal value during operation due to power distribution issues, load changes, or design constraints. These voltage fluctuations can affect circuit speed and power consumption.

Temperature Variations: Electronic devices operate in various environments, from cool data centers to hot automotive environments. Temperature can influence carrier mobility, resistance, and leakage currents, affecting timing and power dissipation [34].

By combining process, voltage, and temperature (PVT) variations, designers simulate extreme conditions like "FF at high voltage and high temperature" or "SS at low voltage and low temperature" to determine the limits of acceptable performance. Various process parameters, such as MOSFET threshold voltage and mobility, are influenced by temperature, so designs must be robust enough to handle temperature fluctuations. To assess how the VCO's characteristics change with temperature, a sweep analysis was conducted at three different temperatures: -40°C, 27°C, and 140°C.

Table 5 presents the frequency variations of the current-starved voltage-controlled oscillator (CSVCO) under different process, voltage, and temperature (PVT) conditions. The table shows frequency values at five process corners (FF, FS, NN, SF, and SS) for three supply voltages (1.8V, 2.4V, and 3V) across a temperature range from -40°C to 140°C. In general, frequency decreases with increasing temperature due to reduced carrier mobility and transistor performance degradation. The FF corner exhibits the highest frequencies, reaching 2.37 GHz at -40°C with V_{DD} = 2.4V, while the SS corner shows the lowest, dropping to 1.02 GHz at 140°C with V_{DD} = 1.8V. Similarly, higher supply voltages result in increased frequency across all process corners. The nominal NN process follows an intermediate trend, with frequencies ranging from 1.91 GHz at -40°C to 1.33 GHz at 140°C for V_{DD} = 1.8V. These results highlight the CSVCO's sensitivity to temperature and process variations, with significant frequency shifts observed across different conditions. However, the design maintains a broad tuning range, demonstrating its adaptability to varying operating environments.

Figure 11 (a-c) illustrate the output frequency, power consumption, and phase noise of the proposed current-starved oscillator (CSVCO) at different tuning voltages, with temperature varying in three steps from -40°C to 140°C. In Fig. 11 (a), the highest frequency is observed in the FF corner at a 2.4 V power supply, while Fig. 11 (b) shows that the SS corner consumes the least power at a 1.8 V supply at elevated temperatures. As temperature increases, phase noise improves, showing better performance at higher temperatures as shown in Fig. 11 (c). Both output frequency and power dissipation exhibit significant shifts with rising temperatures, whereas higher temperatures have a positive effect on phase noise.

Table 5 — PVT variations of Frequency of CSVCO

			Temperature (°C)		
			-40	27	140
Frequency (GHz)	FF	V_{DD} 1.8 V	2.32	2.06	1.71
		V_{DD} 2.4 V	2.37	2.15	1.81
		V_{DD} 3 V	2.18	2.01	1.73
	FS	V_{DD} 1.8 V	1.94	1.72	1.43
		V_{DD} 2.4 V	2.12	1.91	1.59
		V_{DD} 3 V	1.98	1.81	1.54
	NN	V_{DD} 1.8 V	1.82	1.61	1.33
		V_{DD} 2.4 V	1.91	1.71	1.43
		V_{DD} 3 V	1.76	1.61	1.37
	SF	V_{DD} 1.8 V	1.66	1.46	1.22
		V_{DD} 2.4 V	1.68	1.51	1.27
		V_{DD} 3 V	1.55	1.41	1.21
	SS	V_{DD} 1.8 V	1.4	1.23	1.02
		V_{DD} 2.4 V	1.49	1.33	1.11
		V_{DD} 3 V	1.38	1.25	1.06

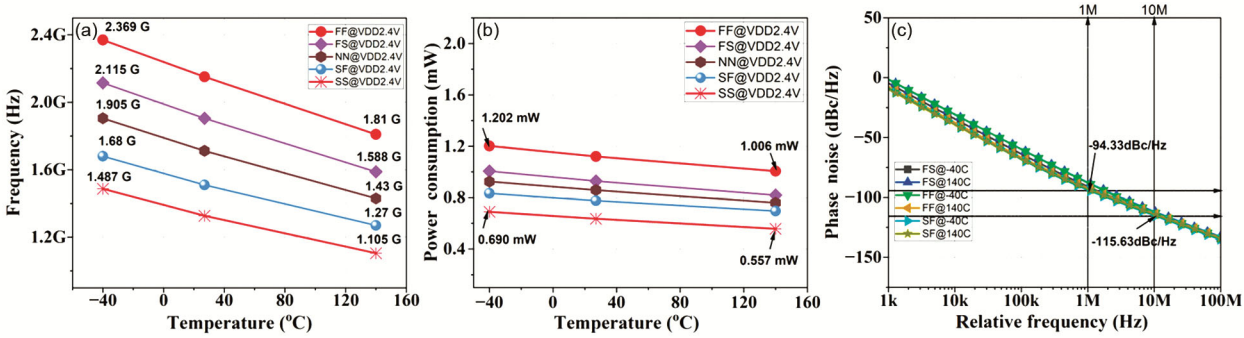

Fig. 11 — Variation in (a) frequency, (b) power dissipation, and (c) phase noise with tuning voltage of the Voltage-controlled current-starved oscillator (CSVCO) for various temperatures

Table 6 presents the frequency variations of the LC-VCO under different process, voltage, and temperature (PVT) conditions. The table shows frequency values at five process corners (FF, FS, NN, SF, and SS) for three supply voltages (1.8V, 2.4V, and 3V) across a temperature range from -40°C to 140°C. Overall, frequency decreases with increasing temperature due to the degradation of transistor mobility and the LC tank's reduced resonance efficiency. The highest frequency is observed at -40°C in the FF corner (2.499 GHz at V_{DD} = 1.8V), while the lowest occurs at 140°C in the SS corner (2.304 GHz at V_{DD} = 1.8V). Across all process corners, the frequency remains relatively stable, with only minor variations between voltage levels, indicating strong PVT robustness. Unlike the CSVCO, the LC-VCO exhibits a much narrower frequency variation, with frequency differences typically within 0.2 GHz across different conditions.

Table 6 — PVT variations of Frequency of LCVCO

			Temperature (°C)			
			-40	27	50	140
Frequency (GHz)	FF	V_{DD} 1.8 V	2.499	2.428	2.416	2.321
		V_{DD} 2.4 V	2.493	2.427	2.393	2.323
		V_{DD} 3 V	2.494	2.417	2.405	2.32
	FS	V_{DD} 1.8 V	2.513	2.439	2.408	2.302
		V_{DD} 2.4 V	2.504	2.433	2.401	2.324
		V_{DD} 3 V	2.497	2.429	2.4	2.324
	NN	V_{DD} 1.8 V	2.512	2.438	2.408	2.325
		V_{DD} 2.4 V	2.504	2.433	2.402	2.322
		V_{DD} 3 V	2.497	2.429	2.398	2.322
	SF	V_{DD} 1.8 V	2.513	2.436	2.407	2.322
		V_{DD} 2.4 V	2.505	2.433	2.402	2.321
		V_{DD} 3 V	2.498	2.429	2.396	2.321
	SS	V_{DD} 1.8 V	2.506	2.425	2.41	2.304
		V_{DD} 2.4 V	2.51	2.434	2.401	2.315
		V_{DD} 3 V	2.504	2.434	2.404	2.322

This highlights the LC-VCO's superior frequency stability, making it well-suited for applications requiring precise frequency control under varying environmental and fabrication conditions.

Figure 12 (a) demonstrates that as temperature increases, the frequency decreases, while Fig. 12 (b) shows a rise in power consumption with increasing temperature. Figure 12(c) presents that phase noise improves with higher temperatures, with the SF corner exhibiting phase noise of -129.36 dBc/Hz at 1 MHz and -149.36 dBc/Hz at 10 MHz.

4.5 Monte Carlo Analysis

Monte Carlo Analysis is a widely employed statistical method in integrated circuit (IC) design to evaluate the influence of random variations in design parameters on overall performance. It entails performing numerous simulations with randomly varied parameters to capture a wide range of possible outcomes, offering valuable insights into the design's behavior and robustness across different conditions [35]. In IC design, manufacturing imperfections often cause random variations in parameters such as transistor threshold voltage, channel length, and oxide thickness. Monte Carlo analysis models these variations through random sampling, allowing designers to predict system performance and reliability across diverse scenarios. Unlike corner analysis, which examines only the extreme best-case and worst-case conditions, Monte Carlo analysis provides a broader statistical view, revealing how the design performs across the full range of potential variations.

This approach is vital for IC design, helping designers understand the effects of manufacturing and environmental randomness on circuit performance. It enables the optimization of designs for improved yield, robustness, and reliability in real-world applications.

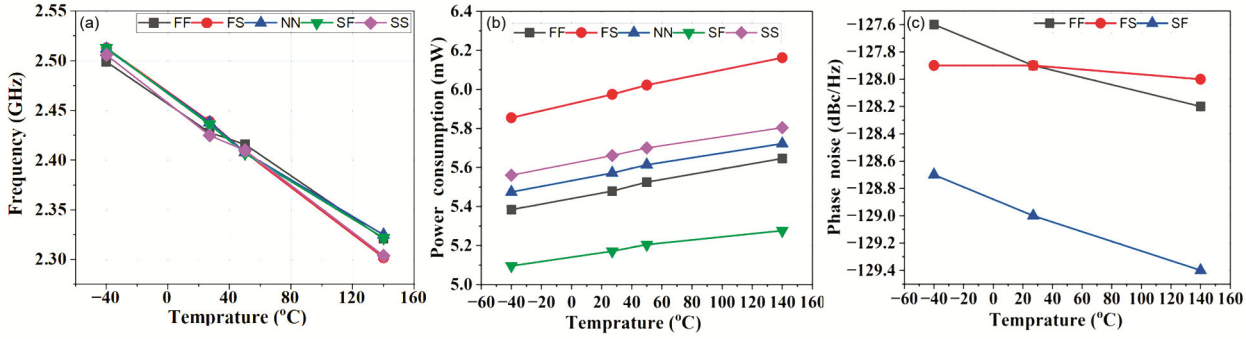

Fig. 12 — Variation in (a) frequency (b) power consumption, and (c) phase noise with tuning voltage of the LC-VCO for various temperatures

The proposed current-starved voltage-controlled oscillator (CSVCO) and LC-VCO underwent Monte Carlo analysis to evaluate the effects of process variation and mismatch. The analysis was performed at control voltages of 0.3 V, 0.6 V, 0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.1 V, 2.4 V, 2.7 V, and 3.0 V, with 200 samples used to evaluate oscillation frequency and power consumption.

Figure 13 (a - b) display the statistical distribution of Monte Carlo results for the CSVCO's oscillation frequency and power consumption. The average oscillation frequency is 1.718 GHz with a standard deviation of 126.050 MHz, while the average power consumption is 857.231 µW with a standard deviation of 52.926 µW.

Figure 14 (a - b) present the Monte Carlo simulation results for the LC-VCO, including oscillation frequency, and power consumption. The average oscillation frequency is 2.44396 GHz with a standard deviation of 118.234 MHz, and the average power consumption is 5.5842 mW with a standard deviation of 83.914 µW.

4.6 Tuning Range

The tuning range of a VCO defines the frequency span over which the VCO can be adjusted or tuned by varying its control voltage [36].

$$f_0 = f_{center} = \frac{f_{\max} + f_{\min}}{2} \quad \ldots (15)$$

$$FrequencyTunningRange(\%) = \frac{f_{\max} - f_{\min}}{f_{center}} \quad \ldots (16)$$

In Eqs (15) and (16) f_0 or f_{center} and FTR (%) are given, respectively. Where f_{max} is the maximum frequency and f_{min} is the minimum frequency of the VCO. In Fig. 8 (a), at a V_{DD} 2.4 V power supply, the frequency of current-starved VCO varies between 0.119 GHz to 2.905 GHz at different process corners by varying the control voltage from 0 V to 3.0 V. In Fig. 9 (a), at a V_{DD} 1.8 V power supply, the frequency of LC-VCO varies between 2.418 GHz to 2.439 GHz at different process corners by varying the control voltage from 0 V to 3 V. The Tuning frequency of current starved VCO and LC-VCO are 184.26 %, and 0.87 % respectively.

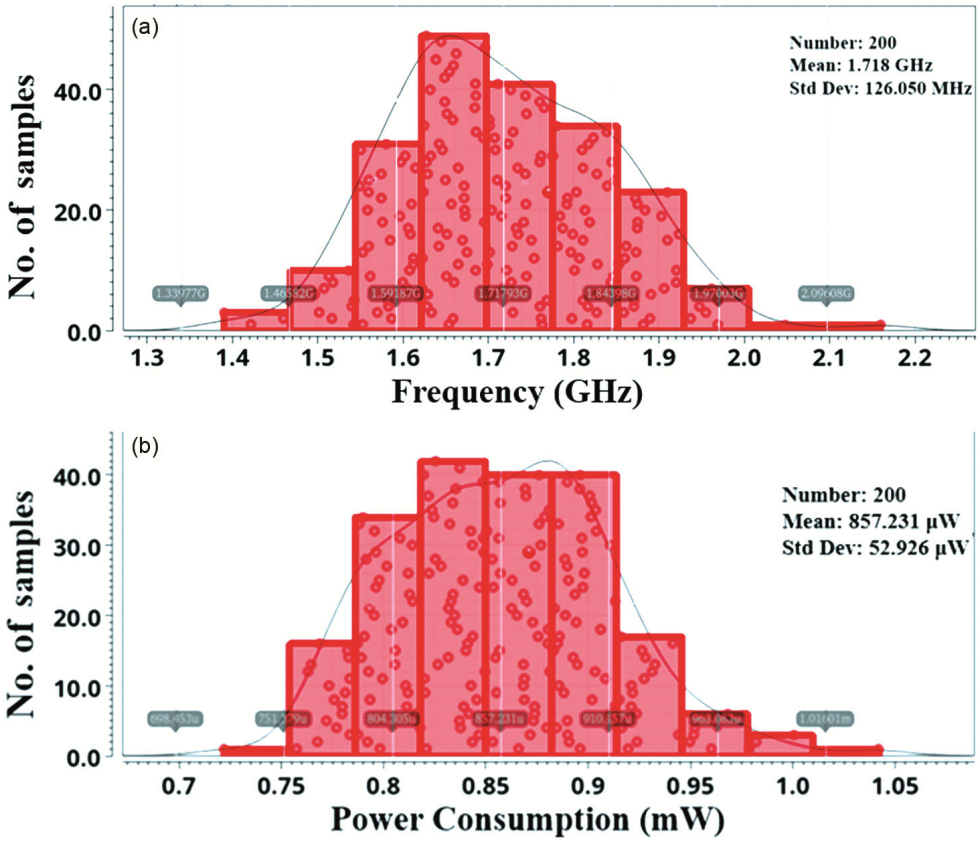

Fig. 13 — Statistical distribution of (a) oscillation frequency, and (b) power consumption for Current starved voltage-controlled oscillator

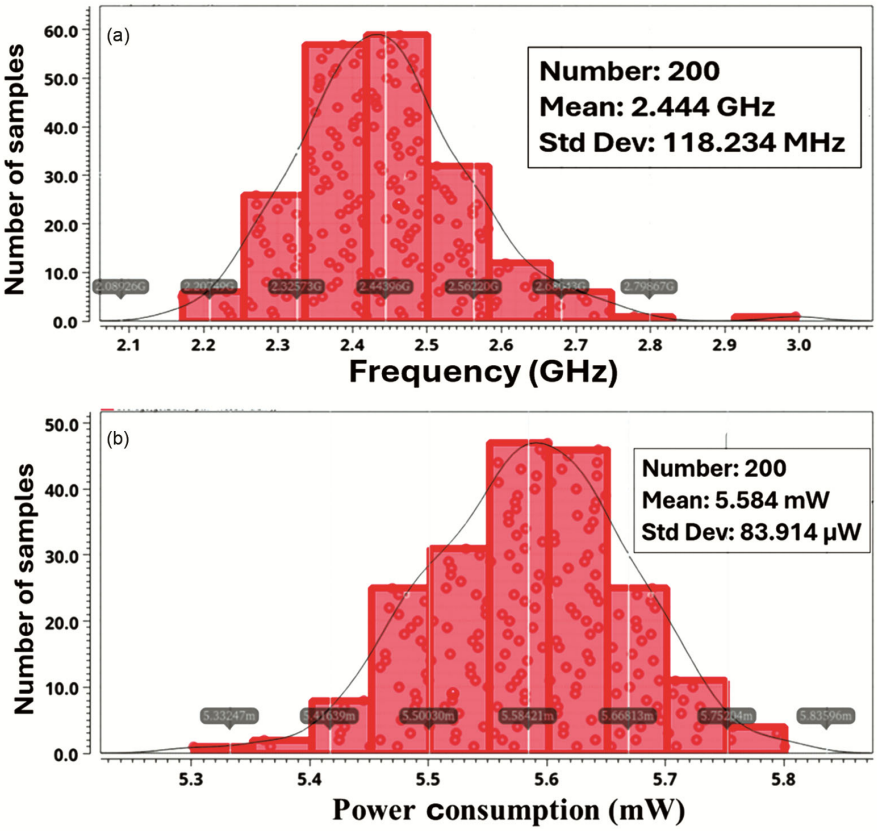

Fig. 14 — Statistical distribution of (a) oscillation frequency, and (b) power consumption of LC-VCO

Table 7 — Performance comparison with reported Current Starved Ring VCOs

	Simulated/ Measured	Technology (nm)	Supply Voltage (V)	Power Consumption (mW)	Tuning Range (GHz)	Tuning Range (%)	Phase Noise (dBc/Hz) @ 1MHz	FOM (dBc/Hz) @ 1MHz	FOM_T (dBc/Hz) @ 1MHz	Type
[41]	M	180	1.8	28	1.78 to 2.53	34.72	-92.68	-144.9	-155.71	4-stage Ring
[42]	S	180	0.9	26.41	0.1 to 0.13	26.09	-129.01	-156.01	-164.34	8-stage Ring
[43]	S	180	1.15	0.01	2.05 to 2.6	23.66	-67	-152.66	-160.14	5-stage Ring
[44]	M	180	1.8	4.89	2.25 to 2.52	11.32	-107	-167.66	-168.74	3-stage Ring
This Work	S	180	2.4	1.16	0.119 to 2.905	184.26	-91.80	-154.75	-180.05	5-stage Ring

The figure-of-merit (FoM) term assesses, compares, and consolidates various design metrics of the Voltage-Controlled Oscillator (VCO) into a single equation[37-40]. A lower FOM indicates a superior oscillator design. The universally accepted definition of the figure of merit (FoM) is as follows Eq (17):

$$FoM = L(\Delta f) - 20\log(\frac{f_0}{\Delta f}) + 10\log(\frac{P_{DC}}{1mw}) \quad \ldots (17)$$

In this case, f_0 denotes the center oscillation frequency, L (Δf) is the phase noise at the offset frequency Δf, and P_{DC} is the DC power used by the core oscillator. The FoM of the LC-VCO is -167.34 dBc/Hz, while the CSVCO's is -154.75 dBc/Hz.

The voltage-controlled oscillator's overall performance is represented by FoM_T as shown in Eq (18). More negative values improve the FoM_T [50-53].

$$FoM_T = FoM - 20\log(\frac{FTR(\%)}{10}) \quad \ldots (18)$$

Table 8 — Performance comparison with reported LC-VCOs

Ref.	Simulated/ Measured	Technology (nm)	Supply Voltage (V)	Power Consumption (mW)	Tuning Range (GHz)	Phase Noise (dBc/Hz) @ 1MHz	FOM (dBc/Hz) @ 1MHz	Type
[45]	S	180	1.8	28.17	3.75 to 3.95	-132.9	-190.11	LC
[46]	S	180	1.5	11.32	11.59 to 13.96	-110.1	-193.11	LC
[47]	M	180	2	7.5	17 to 17.9	-110.3	-186.39	LC
[48]	M	180	1.8	20.6	2.1 to 2.8	-129.3	-183.94	LC
[49]	M	180	1.8	14.4	19.93 to 29.52	-97.6	-173.88	LC
[23]	S	180	1.5	8.22	2.6 to 4.4	-125	-184.47	LC
[44]	S	180	1.1	12	20.8 to 26.8	-102.7	-178.8	LC
This Work	S	180	1.8	5.58	2.418 to 2.439	-128.37	-188.55	LC

Taking advantage of the wide TR, we calculated FoM with TR (FoM_T) for fair comparison[54-55]. Table 7 and 8 summarize this work and other state-of-the-art published voltage-controlled oscillators.

The proposed CS-VCO in Table 7, outperforms existing designs with an exceptional tuning range of 184.26%, far surpassing previous works. It achieves low power consumption (1.16 mW), significantly lower than[41] (28 mW) and[42] (26.41 mW). While its phase noise (-91.80 dBc/Hz) is slightly worse than[44] (-107 dBc/Hz), it compensates with the best FoM_T (-180.05 dBc/Hz).

The proposed LC-VCO stands out for its low power consumption (5.58 mW), significantly lower than most references like[45] (28.17mW) and [48] (20.6 mW). While its tuning range (2.418–2.439 GHz) is narrower than others, it maintains good phase noise (-128.37 dBc/Hz), comparable to[48] (-129.3 dBc/Hz). It's high F_OM (-188.55 dBc/Hz) surpasses designs like[49] (-173.88 dBc/Hz), proving its efficiency. Indicating superior overall efficiency. Compared to prior designs, this 5-stage ring VCO provides an excellent balance of wide tuning range, low power, and strong FoM_T performance, making it highly suitable for low-power, wideband applications.

5 Conclusion

In conclusion, this research demonstrates the design and performance analysis of two Voltage-Controlled to 2.91 GHz, while the LC-VCO covers a narrower range from 2.418 GHz to 2.439 GHz. Phase noise measurements at a 1 MHz offset are -91.80 dBc/Hz for the CSVCO and -128.37 dBc/Hz for the LC-VCO, with power consumption of 1.16 mW and 5.58 mW, respectively. The calculated Figure of Merit with Tuning (FoM_T) is -180.05 dBc/Hz for the CSVCO and -167.34 dBc/Hz for the LC-VCO. Both designs exhibit strong performance in terms of low power, low phase noise, and enhanced temperature resilience, positioning them as promising candidates for a range of UHF applications where these characteristics are crucial.

With its bandwidth-enhanced varactor circuit, it achieves superior low-phase noise performance, while the CSVCO leverages an I-MOS varactor for enhanced tuning capabilities. Through extensive simulations, including process, voltage, and temperature (PVT) variations, as well as temperature sweeps from -40°C to 140°C and Monte Carlo analysis with 200 samples, both designs were evaluated under extreme conditions. The CSVCO demonstrates a wide tuning range from 0.119 GHz to 2.91 GHz, while the LC-VCO covers a narrower range from 2.418 GHz to 2.439 GHz. Phase noise measurements at a 1 MHz offset are -91.80 dBc/Hz for the CSVCO and -128.37 dBc/Hz for the LC-VCO, with power consumption of 1.16 mW and 5.58 mW, respectively. The calculated Figure of Merit with Tuning (FoM_T) is -180.05 dBc/Hz for the CSVCO and -167.34 dBc/Hz for the LC-VCO. Both designs exhibit strong performance in terms of low power, low phase noise, and enhanced temperature resilience, positioning them as promising candidates for a range of UHF applications where these characteristics are crucial.

Oscillators (VCOs) optimized for Ultra High Frequency (UHF) applications: a current-starved VCO (CSVCO) and a cross-coupled LC-based VCO (LC-VCO), both implemented using a 180 nm CMOS process. The LC-VCO, with its bandwidth-enhanced varactor circuit, achieves superior low-phase noise performance, while the CSVCO leverages an I-MOS varactor for enhanced tuning capabilities. Through extensive simulations, including process, voltage, and temperature (PVT) variations, as well as temperature sweeps from -40°C to 140°C and Monte Carlo analysis with 200 samples, both designs were evaluated under

extreme conditions. The CSVCO demonstrates a wide tuning range from 0.119 GHz to 2.91 GHz, while the LC-VCO covers a narrower range from 2.418 GHz to 2.439 GHz. Phase noise measurements at a 1 MHz offset are -91.80 dBc/Hz for the CSVCO and -128.37 dBc/Hz for the LC-VCO, with power consumption of 1.16 mW and 5.58 mW, respectively. The calculated Figure of Merit with Tuning (FoM_T) is -180.05 dBc/Hz for the CSVCO and -167.34 dBc/Hz for the LC-VCO. Both designs exhibit strong performance in terms of low power, low phase noise, and enhanced temperature resilience, positioning them as promising candidates for a range of UHF applications where these characteristics are crucial.

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References

1 Yelleswarapu P, Jha A, Willis R, Makris Y & K K O, *IEEE Trans Microw Theory Tech*, 70 (6) (2022) 3244, https://doi.org/10.1109/TMTT.2022.3164949.

2 Sivaraaj N R & Majeed K K A, *IEEE Access,* 11 (2023) 127987, https://doi.org/10.1109/ACCESS.2023.3331308.

3 Kuo Y F, Wu Y P & Liu Y C, *IEEE Microw Wirel Compon Lett,* 31 (2) (2021) 181, https://doi.org/10.1109/LMWC.2020.3036127.

4 Fang M & Yoshimasu T, *IEEE Trans Microw Theory Tech,* 68(10) (2020) 4116, https://doi.org/10.1109/TMTT.2020.2990441.

5 Kandpal N, Singh A & Agarwal A, *Circuits Systems and Signal Processing*, 41 (2022) 4275, https://doi.org/10.1007/s00034-022-02001-x.

6 Liao R-Y, Chen H-H, Lin P-Y, Liang T-A, Su K-H, Lin I-C & Cheng C-H, *Mater,* 16 (2023) 3306, https://doi.org/10.3390/ma16093306.

7 Guo R, Qian K, Wei J, Chen T, Liu Y, Kong D, Wang J J, Wu Y, Hu S G, Yu Q I & Liu Y, *IEEE Access* 7 (2019) 60120, https://doi.org/10.1109/ACCESS.2019.2915335.

8 Xiang P, Fang Y, Zhang Q, Xie Z, Wang H & Wang Z, *IEEE Trans Circuits Syst II Express Briefs,* 70 (9) (2023) 3654, https://doi.org/10.1109/TCSII.2023.3279312.

9 Alzahrani S, Elabd S, Smith S, Naguib A, Tantawy R & Khalil W, *IEEE Trans Microw Theory Tech,* 70 (5) (2022) 2668, https://doi.org/10.1109/TMTT.2022.3151668.

10 Riccardi D, Franceschin A & Mazzanti A, *SSC-L*, 5 (2022) 182, https://doi.org/10.1109/LSSC.2022.3193236.

11 Bhat A, Nandwana R & Lakshmikumar K, *IEEE Trans Circuits Syst II Express Briefs*, 69 (3) (2022) 919, https://doi.org/10.1109/TCSII.2021.3134093.

12 Saha S, Krishnan S & Sweet A A, *IEEE J microw,* 2 (1) (2022) 185, https://doi.org/10.1109/JMW.2021.3122881.

13 Yoshio T, Kihara T & Yoshimura T, *APMC*, (2017) 946, https://doi.org/10.1109/APMC.2017.8251606.

14 Chen Y, Liu Y H, Zong Z, Dijkhuis J, Dolmans G, Staszewski R B & Babaie M, *JSSC*, 54 (1) (2019) 240, https://doi.org/10.1109/JSSC.2018.2871195.

15 Bhat A & Krishnapura N, *IEEE TCAS-I*, 65 (7) (2018) 2127, https://doi.org/10.1109/TCSI.2017.2782247.

16 Li H, Deng S, Xu Y, Zhong W, Luo D, Li G, Kwok H S & Chen R, *IEEE Trans Electron Devices* 69 (4) (2022) 1870, https://doi.org/10.1109/TED.2022.3152453.

17 Lee D, Park G, Han J & Choo M S, *IEEE Access*, 11 (2023) 7530, https://doi.org/10.1109/ACCESS.2022.3232960.

18 Anjum N, Yadav V K S & Nath V, *IJMIT,* 1 (2) (2023) 82, https://doi.org/10.5281/zenodo.8288193.

19 Schramme M, Van Brandt L, Flandre D & Bol D, *IEEE TCAS-I,* 69 (5) (2022) 1883, https://doi.org/10.1109/TCSI.2022.3144527.

20 Minati L, Frasca M, Yoshimura N, Ricci L, Oświecimka P, Koike Y, Masu K & Hiroyuki Ito H, *IEEE Access,* 7 (2019) 54638, https://doi.org/10.1109/ACCESS.2019.2912903.

21 Huq S M I, Baroi O L, Shihab S A & Biswas S N, *IEEE Trans Circuits Syst II Express Briefs,* 68 (4) (2021) 1098 , https://doi.org/10.1109/TCSII.2020.3027897.

22 Rudrapati S & Gupta S, *IEEE Trans Circuits Syst II Express Briefs,* 65 (12) (2018) 1914, https://doi.org/10.1109/TCSII.2018.2802930.

23 Yu F, Tang Q, Wang W & Wu H, *Wireless Personal Communications,* 86 (2015) 671, doi:10.1007/s11277-015-2951-8.

24 Fiorelli R, Peralias E J & Silveira F, *IEEE Trans Microw Theory Tech,* 59 (7) (2011) 1822, https://doi.org/10.1109/TMTT.2011.2132735.

25 Lu J, Wang N –Y & Chang M -C F, *IEEE J Solid-State Circuits,* 47 (5) (2012) 1131, https://doi.org/10.1109/JSSC.2012.2185573.

26 Jahan N, Barakat A & Pokharel R K, *IEEE Trans Circuits Syst II Express Briefs,* 68 (12) (2021) 3513, https://doi.org/10.1109/TCSII.2021.3079309.

27 Hsieh J Y & Lin K Y, *IEEE Trans Circuits Syst II Express Briefs,* 66 (8) (2019) 1307, https://doi.org/10.1109/TCSII.2018.2886171.

28 Hamidi S B & Dawn D, *IEEE Microw Wirel Compon Lett,* 32 (11) (2022) 1307, https://doi.org/10.1109/LMWC.2022.3182020.

29 Lee H S, Jang T H, Kim J H & Park C S, *IEEE T VLSI SYST,* 31 (10) (2023) 1629, https://doi.org/10.1109/TVLSI.2023.3294404.

30 Fiorelli R, Peralias E J & Silveira F, *IEEE Trans Microw Theory Tech,* 59 (7) (2011) 1822, https://doi.org/10.1109/TMTT.2011.2132735.

31 Saw S K & Nath V, *In 2015 International Conference on Industrial Instrumentation and Control (ICIC),* 1388, https://doi.org/10.1109/IIC.2015.7150965.

32 Maiti M, Saw S K, Nath V, *et al*., *Microsyst Technol*, 25 (2019) 4615, https://doi.org/10.1007/s00542-019-04458-4.

33 Verma S, Singh S, Pal B B, Kumar M, Devendra K, Verma S & Nath V, *Indian J Sci Technol,* 9 (44) (2016), https://doi.org/10.17485/ijst/2016/v9i44/125458.

34 Souri M & Ghaznavi M B, *Circuits Syst Signal Process,* 35 (2016) 1481, https://doi.org/10.1007/s00034-015-0127-0.

35 Ullah F, Liu Y, Li Z, Wang X, Sarfraz M M & Zhang H, *Electronics,* 7(8) (2018) 127, https://doi.org/10.3390/electronics7080127.

36 Rajalingam P, Jayakumar S & Routray S, *Silicon,* 13 (2021) 2715, https://doi.org/10.1007/s12633-020-00619-7.

37 Suhas D & Bharadwaj S, *Procedia Comput Sci,* 115 (2017) 756, https://doi.org/10.1016/j.procs.2017.09.170.

38 Saw S K & Nath V, *In 2015 International Conference on Computing, Communication & Automation,* 1252, https://doi.org/10.1109/CCAA.2015.7148611.

39 Saw S K, Maiti M, Nath V & Majumder A, *In 2020, Nath V, Mandal J (eds) Nanoelectronics, Circuits and Communication Systems NCCS 2018, Lecture Notes in Electrical Engineering, Springer,* 642, https://doi.org/10.1007/978-981-15-2854-5_33.

40 Cheng K W, Chang S K & Huang Y C, *IEEE Trans. Circuits Syst. II Express Briefs,* 66 (5) (2019) 733, https://doi.org/10.1109/TCSII.2019.2908423.

41 Gui X, Tang R, Zhang Y, Li D & Geng L, *IEEE Microw Wirel Compon Lett,* 30 (3) (2020) 288, https://doi.org/10.1109/LMWC.2020.2967391.

42 Aviña P R C, Cuautle E T & Fraga L G D L, *AIMS Math*, 7 (2022) 14826, http://dx.doi.org/%2010.3934/math.2022813.

43 Das K, Pradhan N, Kumar V & Jana S K, *ISDCS Howrah India*, (2020) 1, https://doi.org/10.1109/ISDCS49393.2020.9263006.

44 Lin J, Li J, Luo Z, & Yu M, *AEU - Int J Electron Comm,* 187 (2024) 155557, https://doi.org/10.1016/j.aeue.2024.155557.

45 Mazloum J & Sheikhaei S, *Microelectron J,* 107 (2021) 104944, https://doi.org/10.1016/j.mejo.2020.104944.

46 Nasri A & Yargholi M, *IETE J Res,* 68 (3) (2022) 2164, https://doi.org/10.1080/03772063.2019.1691063.

47 Mansour I, Mansour M, Aboualalaa M, Allam A, Rahman A B A, Pokharel R K & Zahhad M A, *IEEE Microw Wirel Compon Lett,* 32 (10) (2022) 1207, https://doi.org/10.1109/LMWC.2022.3167705.

48 Xi N, Lin F & Ye T, *IEEE Trans Circuits Syst II Express Briefs,* 67 (3) (2020) 450, https://doi.org/10.1109/TCSII.2019.2923235.

49 Chen Y D & Chin A, *IEEE Microw Wirel Compon Lett,* 31 (9) (2021) 1063, https://doi.org/10.1109/LMWC.2021.3096006.

50 Kuo Y F, Wu Y P & Liu Y C, *IEEE Microw Wirel Compon Lett,* 31 (2) (2021) 181, https://doi.org/10.1109/LMWC.2020.3036127.

51 Gui X, Tang B, Tang R, Li D & Geng L, *IEEE T VLSI Syst,* 28 (7) (2020) 1589, https://doi.org/10.1109/TVLSI.2020.2991765.

52 Yang T -S, Hsieh H –Y & Lu L –H, *IEEE TCAS-I,* 70 (9) (2023) 3545, https://doi.org/10.1109/TCSI.2023.3284294.

53 Chen B, Pokharel R K, Thapa S K, Jahan N & Barakat A, *IEEE Microw Wirel Compon Lett,* 32 (10) (2022) 1203, https://doi.org/10.1109/LMWC.2022.3171405.

54 Abdulazhanov S, Lederer M, Lehninger D, Mart C, Ali T, Wang D & Gerlach G, *IEEE Transactions on Electron Devices,* (2021) 1, https://doi.org/10.1109/TED.2021.3104532.

55 Urso A, Chen Y, Staszewski R B, Dijkhuis J F, Stanzione S, Liu Y H, Serdijn W A & Babaie M, *IEEE TCAS-I,* 67 (11) (2020) 3764, https://doi.org/10.1109/TCSI.2020.3012106.