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Design and Simulation of All-optical 2×2-Bit Reversible Multiplier Using RSOA-Based Switches

Diksha Ruhela* & Rajni Jindal
Delhi Technological University, Delhi 110 042, India

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This work presents the design and simulation of an all-optical 2×2-bit reversible multiplier utilizing switches based on Reflective Semiconductor Optical Amplifiers (RSOAs). The architecture exploits the inherent gain saturation and double-pass reflection characteristics of RSOAs to realize reversible logic operations, specifically XOR and AND gates. A comprehensive theoretical analysis is provided, along with numerical simulations assessing key performance indicators such as Extinction Ratio (ER), Quality Factor (Q), and Relative Eye Opening (REOP). Simulation results validate the functional correctness and efficiency of the proposed design, demonstrating its potential for high-speed, low-power optical computing systems.

Keywords: RSOA, Multiplier, Reversible logic, Cross gain modulation, Extinction ratio (ER), Quality factor (Q)

1 Introduction

The rapid advancement of digital technologies and the growing demand for high-speed, energy-efficient computation have catalyzed significant research into all-optical signal processing. In this context, reversible logic circuits have emerged as a promising approach due to their ability to minimize energy dissipation by preserving a bijective mapping between inputs and outputs. Unlike conventional irreversible logic gates, which inherently dissipate energy due to information loss—an effect explained by Landauer's principle—reversible gates circumvent this limitation, making them particularly suitable for low-power optical and quantum computing applications[1–4].

To implement such reversible gates, various optical devices have been explored, including semiconductor optical amplifiers (SOAs), Mach–Zehnder interferometers (MZIs), micro-ring resonators, Sagnac interferometers, and terahertz optical asymmetric demultiplexers (TOADs). These devices exploit the inherent properties of light to perform signal modulation, amplification, and interference-based logic operations, enabling fast and efficient optical computing.

Among these components, Reflective Semiconductor Optical Amplifiers (RSOAs) have attracted considerable interest due to their dual functionality as both amplifiers and switches. This dual role provides a key advantage over traditional optical devices that typically perform only one function. RSOAs enhance the signal-to-noise ratio by enabling direct signal amplification, thereby reducing the need for external amplification stages. Their key attributes—including high optical gain, fast switching speed, low power consumption, and bidirectional amplification—make them ideal candidates for constructing high-performance optical logic circuits. In particular, when operated under the cross-gain modulation (XGM) regime, RSOAs can implement fundamental logic functions such as AND, XOR, and NOT in a compact and power-efficient manner. The inherent compactness of RSOA-based logic gates further facilitates their integration into semiconductor-based photonic integrated circuits (PICs), which is critical for the scalability and miniaturization of future optical computing systems[5–12].

Multipliers are fundamental components of arithmetic logic units and play a pivotal role in numerous computational architectures. Designing a compact 2×2-bit reversible multiplier provides a suitable platform for evaluating the performance of optical logic circuits in terms of speed, energy efficiency, and signal integrity. While several optical multiplier architectures have been proposed—employing technologies such as micro-ring resonators, photonic crystals, plasmonic gates, and hybrid electro-optic platforms—many of these approaches face challenges related to scalability,

*Corresponding author: E-mail: diksharuhela_phd2k19@dtu.ac.in

polarization sensitivity, fabrication complexity, and compatibility with existing photonic integration techniques.

In this study, we propose a novel 2×2-bit all-optical reversible multiplier using RSOA-based Feynman and Peres logic gates. The proposed architecture leverages the advantages of RSOAs and utilizes XGM dynamics to enable high-speed reversible logic operations. The design incorporates multiple RSOA-based switches and optical beam splitters to realize the required logic functions, achieving improved performance in key optical metrics such as extinction ratio (ER), quality factor (Q), and relative eye opening (REOP). These parameters serve as critical indicators of signal fidelity, noise tolerance, and operational stability.

A simulation-based evaluation is presented to analyze the influence of control pulse energy and injection current on the circuit's optical behavior. The results confirm the feasibility of the proposed RSOA-based design for low-power, high-speed optical computing applications and suggest its potential scalability for more complex arithmetic systems. Additionally, a comparative analysis is performed against recent state-of-the-art all-optical multiplier architectures, benchmarking the proposed design based on ER, Q-factor, and REOP. This comparison underscores the proposed circuit's superiority in terms of signal integrity, energy efficiency, and integration potential, highlighting its suitability for future high-performance photonic computing platforms.

2 Background

2.1 Reversible Logic in Optical Computing

All-optical reversible logic gates are a class of optical logic gates designed to perform logical operations while ensuring the reversibility of the computation. This means that for every output produced, there exists a unique corresponding input, preventing any information loss during the operation. Since reversible circuit retain all the input information, signal degradation due to data loss is minimized. This helps reduce noise accumulation and improving the accuracy of optical computation. In optical circuits, where light intensity can be affected by scattering, absorption, and diffraction, reversible operation can help maintain signal coherence better[13].

Common examples of all-optical reversible logic gates include Feynman, Toffoli, and Peres gates, which are studied for their applications in optical computation and communication systems. These gates have the potential to support operations like addition and multiplication, making them promising for advanced computational tasks.

The important design constraints of reversible logic circuits are as follows:

(i) Reversible logic gates do not allow fan-outs.
(ii) Reversible logic circuits should possess minimum optical cost.
(iii) The design must be optimized enough to produce minimum number of garbage outputs.
(iv) The reversible logic circuits must be realized to use minimum number of constant inputs.
(v) The reversible logic circuits must use minimum logic depth or gate levels.

In order to efficiently incorporate the reversible circuits, it is essential to optimize the certain paradigm such as, number of constant inputs (CI), garbage outputs (GO), optical cost (GC), and optical delay (OD) which are defined as follows:

Constant inputs (CI): Inputs that are assigned fixed values (0 or 1) to facilitate the desired logical operation in a reversible circuit are known as constant inputs. These inputs help achieve the required functionality without affecting the circuit's reversibility.

Garbage outputs (GO): The additional, unused outputs introduced in a circuit to ensure reversibility are known as garbage outputs. These outputs do not contribute to the primary function but are necessary for maintaining the reversibility of the logic operation

Optical Cost (OC): It is determined by the total number of RSOA switches required for the implementation of the circuit.

Optical delay: It refers to the time taken for an optical signal to propagate through a medium, device, or system before reaching its destination. It is calculated as: Optical Delay=$\Delta \times N$
where:

- Δ (Unit Delay) represents the delay introduced by a single RSOA switch, typically dependent on carrier recovery time and signal processing speed.
- N is the number of RSOA switches present in the critical path of the circuit.

This study, for simplicity, we consider only the optical cost of RSOA switches. Both optical delay and optical cost are analysed as unity to maintain consistency in the evaluation.

2.2 RSOA-Based Optical Switch Using Cross-Gain Modulation

Reflective Semiconductor Optical Amplifiers (RSOAs) play a pivotal role in optical logic gate

implementations due to their ability to amplify signals while exhibiting nonlinear gain saturation, which can be exploited for all-optical signal processing. In this design, the cross-gain modulation (XGM) mechanism is utilized to implement logic operations.

XGM in RSOAs operates based on carrier density depletion and gain saturation. When a high-power control (pump) pulse is injected, it depletes the carrier population, reducing the gain available to a lower-power probe signal, thus modulating the probe's amplification. This mechanism enables inversion logic behaviour and other gate functionalities.

This study, Gaussian pulses are used for both control and probe signals to ensure smooth temporal profiles and reduced distortion. A Gaussian pulse is mathematically described as:

$$P(t) = P_o e^{\left(-\frac{(t-t_O)^2}{2\sigma^2}\right)} \quad \ldots (1)$$

where P_o is the peak power, t_o is the pulse centre, and σ is the standard deviation, related to full-width at half-maximum (FWHM) as:

$$\sigma = \frac{\tau_{FWHM}}{2\sqrt{2\ln 2}} \quad \ldots (2)$$

The small-signal gain G_0 of the RSOA is dependent on the carrier density N:

$$G_0 = \Gamma * \alpha N(N - N_t) \quad \ldots (3)$$

where Γ is the confinement factor, αN is the differential gain, and N_t is the carrier density at transparency.

The dynamic carrier density is governed by:

$$\frac{dN(t)}{dt} = \frac{I}{qV} - \frac{N(t)}{\tau_c} - \frac{g(N(t))|E(t)|^2}{\hbar\omega} \quad \ldots (4)$$

where N(t) is the carrier density, I is the bias current, ħω is the photon energy, q is the elementary charge, $V = w \times d \times L$ is the active volume, τ_c is the carrier lifetime, g(N) is the gain coefficient, and $|E(t)|^2$is the optical field intensity.

Under the influence of a strong control signal Pc, the gain compression is expressed as:

$$G = \frac{G_O}{1+\frac{P_c}{P_{sat}}} \quad \ldots (5)$$

where P_{sat} is the saturation power.

As a result, the probe signal experiences lower gain when the control is present, producing a logic-level inversion. When only the probe is present, it receives unsaturated gain, yielding high output. The output probe power is given by:

$$P_{out} = P_p e^{(G-\alpha_D)L} \quad \ldots (6)$$

where α_D is the internal loss and L is the active length.

In practical implementations, the total output power also includes Amplified Spontaneous Emission (ASE), a noise component introduced during gain amplification. ASE power is given by:

$$P_{ASE} = 2n_{sp} * h\nu(G-1)\Delta f \quad \ldots (7)$$

where n_{sp} is the spontaneous emission factor, hν is the photon energy, and Δf is the optical bandwidth. ASE is incorporated into the output power as it arises from spontaneous emission during the gain process and is modelled using the standard ASE power equation.

This functionality underpins the construction of basic logic gates such as XOR and AND in our 2×2 optical multiplier design.

The RSOA-XGM switch provides ultra-fast response, energy efficiency, and wavelength transparency, which are crucial for high-speed, scalable optical computing systems. The architecture of the RSOA-based optical switch is illustrated in Fig. 1(a), while Fig. 1(b) presents the simulated output waveform corresponding to different control and probe signal combinations. As seen, the device exhibits inverted logic behaviour when both signals are present, a characteristic feature of cross-gain modulation[14-16].

3 Circuit Implementation

This work presents the design of a 2×2 reversible optical multiplier utilizing RSOA-based reversible logic gates. Specifically, the circuit is implemented using two types of reversible gates: the Feynman Gate (FG) and the Peres Gate (PG), both adapted to operate in the optical domain via cross-gain modulation (XGM) in RSOA switches.

3.1 Feynman Gate (FG)

The Feynman Gate (FG) is a two-input, two-output reversible logic gate capable of performing fundamental optical logic operations. It has been implemented here using RSOA-based switching architecture optimized for all-optical XOR functionality. The gate provides two output functions: P = A (pass-through of input A) and Q = A ⊕ B (exclusive-OR of inputs A and B).

The RSOA-based implementation of the FG gate employs two RSOA switches and three beam splitters. A schematic representation of the optical FG gate is shown in Fig. 2.

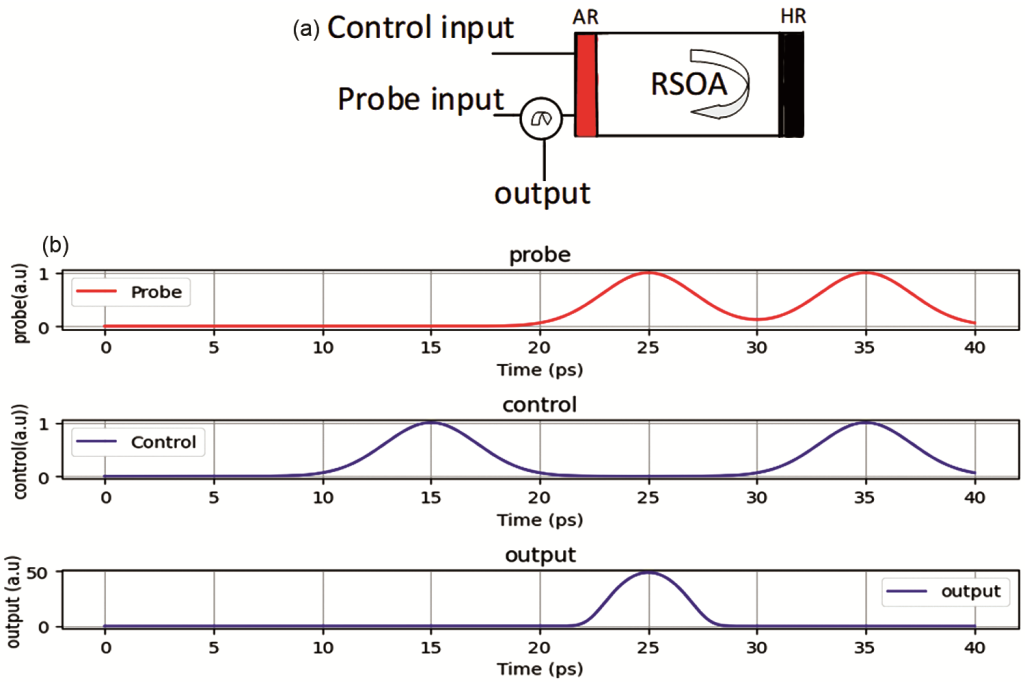

Fig. 1 — (a) Schematic diagram of the Reflective Semiconductor Optical Amplifier (RSOA) used in the switching configuration, and (b) Simulated waveform showing logic levels based on control and probe signal inputs using cross-gain modulation (XGM). The logic behaviour is as follows: Control = 1, Probe = 1 → Output = 0; Control = 0, Probe = 1 → Output = 1

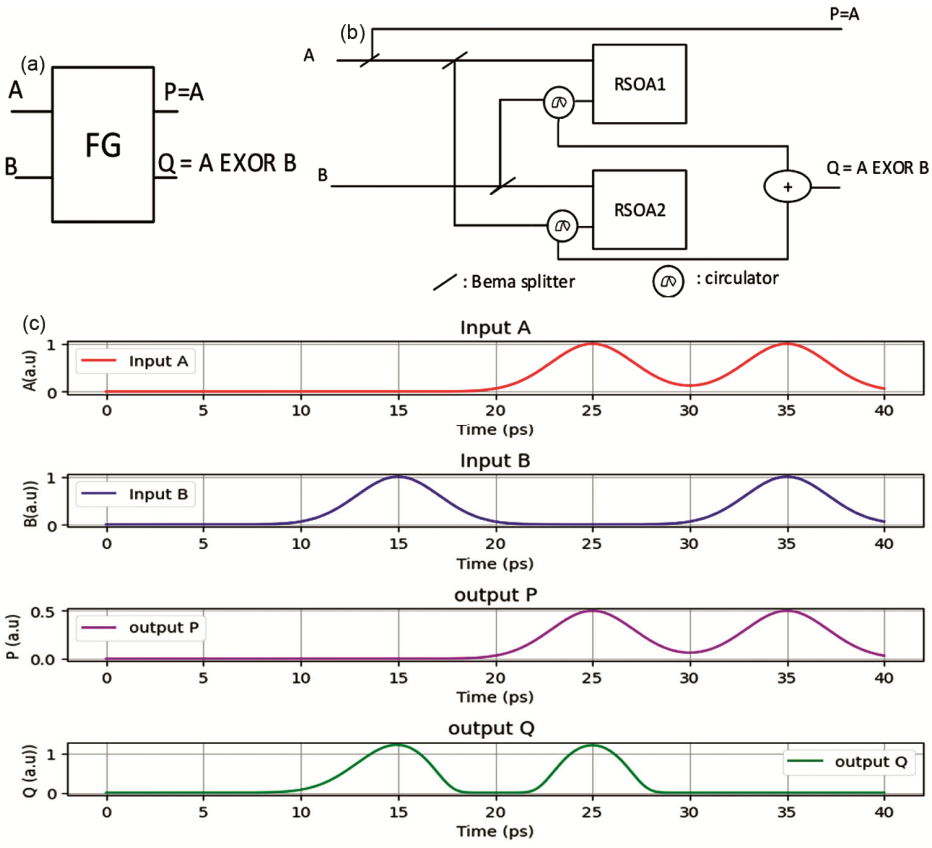

Fig. 2 — (a) Block diagram of FG gate, (b) RSOA implementation of FG gate, and (c) Simulation waveform of FG gate[17]

The functional behaviour of the FG gate is summarized in Table 1. Key performance parameters for the optical FG gate are as follows:

- Optical Cost (OC): 2 (based on the number of RSOA switches used),
- Optical Delay (OD): 1Δ (assuming unit delay per RSOA switch in the critical path).

The truth table of FG gate is given in Table 2. The FG gate also facilitates signal copying, which is crucial in reversible circuit design where fan-out is prohibited. Its simplicity and low resource footprint make it suitable for constructing larger reversible circuits such as multipliers.

3.2 Peres Gate (PG)

The Peres Gate (PG) is a 3×3 reversible optical logic gate implemented using RSOA-based optical switches. It accepts three input signals (A, B, and C) and generates three outputs based on the following transformations: P = A (pass-through), Q = A ⊕ B (XOR operation), and R = AB ⊕ C (AND-XOR combination).

Due to its compact structure and ability to simultaneously implement basic logical operations, the PG gate is highly effective for constructing arithmetic circuits such as adders, multipliers, and encoders. As such, it is considered a fundamental component in the design of all-optical computing architectures for next-generation photonic processors.

The optical implementation of the PG gate consists of six RSOA switches and seven beam splitters, as shown in Fig. 3.

When the third input (**C**) is fixed at logical '0', the PG gate effectively behaves as a half adder, demonstrating its functional versatility. The simulated output waveform for this configuration is presented in Fig. 4, confirming the correct operation of the gate under typical input conditions. A detailed operation of RSOA switches in PG gate logic is provided in Table 3.

The performance metrics of the PG gate are as follows:

- Optical Cost (OC): 6 (number of RSOA switches),
- Optical Delay (OD): 3Δ (assuming a unit delay Δ per RSOA in the critical path). The truth table of PG gate is illustrated in Table 4.

Table 1 — RSOA based Logic Operation of FG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	'$\bar{A}B$'
RSOA2	'A'	'B'	'$\bar{B}A$'

P = A

Q = Output RSOA1 + Output RSOA2 = A ⊕ B

Table 2 — Truth table of FG gate

INPUTS		OUTPUTS	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

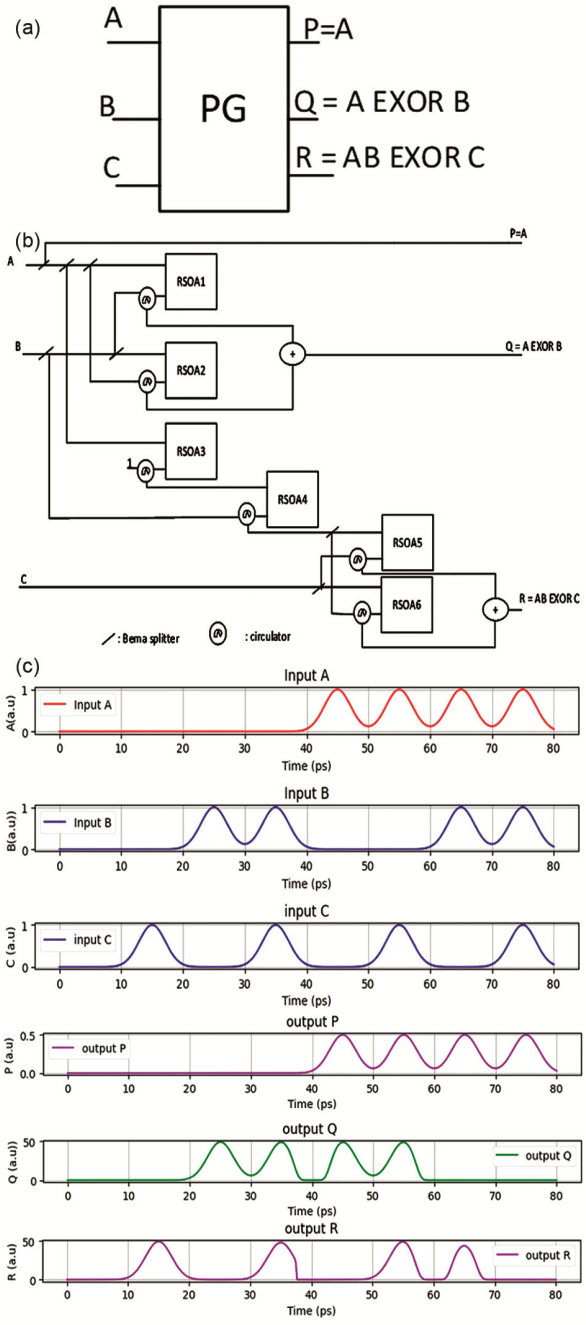

Fig. 3 — (a) Block diagram of PG gate, (b) RSOA implementation of PG gate, and (c) Simulation waveform of PG gate

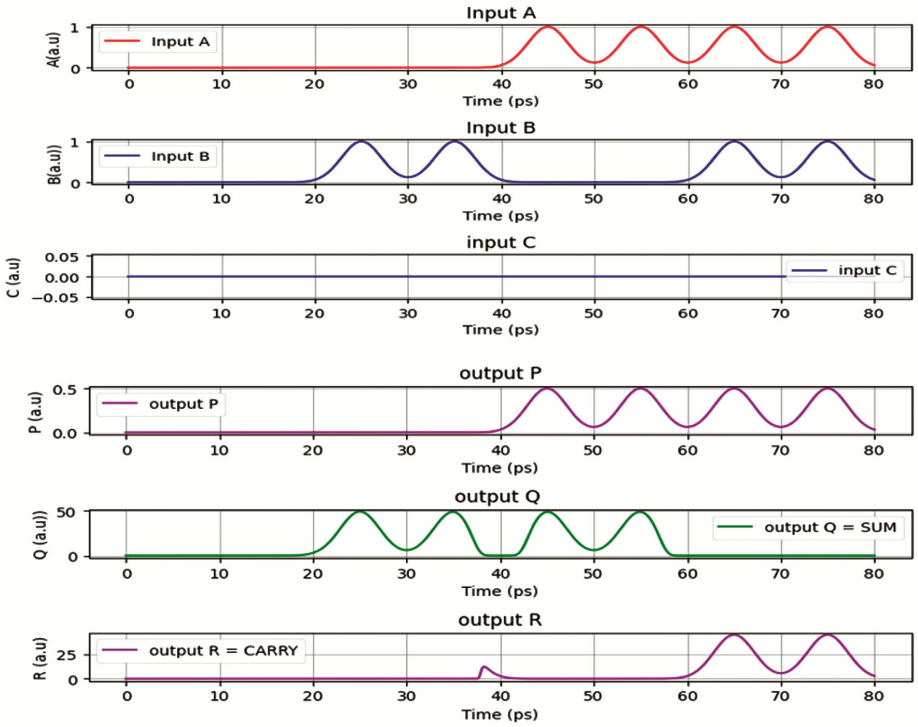

Fig. 4 — PG gate as a half adder

Table 3 — RSOA-Based Logic Operations of PG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	'$\bar{A}B$'
RSOA2	'A'	'B'	'$\bar{B}A$'
RSOA3	High state	'A'	'$\bar{A}$'
RSOA4	'B'	'$\bar{A}$'	'$\bar{\bar{A}}$B'
RSOA5	'C'	'AB'	'$\overline{AB}C$'
RSOA6	'AB'	'C'	'$\bar{C}AB$'

P = A
Q = RSOA1 + RSOA2 = A ⊕ B
R = RSOA5 + RSOA6 = AB ⊕ C

Table 4 — Truth table of PG gate

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

3.3 All-Optical 2×2-Bit Reversible Multiplier

The proposed all-optical 2×2-bit reversible multiplier utilizes a combination of FG and PG gates implemented with RSOA-based switches (Fig. 5). The design is structured into three main functional blocks: fan-out generation, partial product computation, and addition of partial products, followed by final product generation.

3.3.1 Fan-Out Generation

As reversible logic does not permit direct fan-out, four FG gates are employed to generate copies of the input signals A_1, A_0, B_1 and B_0. This ensures signal duplication without violating reversibility. As shown in Fig. 6, an auxiliary input B = 0 is applied to prevent alteration of the original signal values.

3.3.2 Partial Product Generation

Four PG gates are used to compute the partial products of the binary inputs as follows: $P_3 = A1B1$, $P2 = A1B0$, $P1 = A0B1$, $P0 = A0B0$

Each PG gate exploits the AND-XOR logic to produce the required products in an all-optical domain using the XGM effect in RSOAs.

3.3.3 Addition of Partial Products

The partial products are summed using additional PG gates functioning as half adders. These PG gates handle the carry-forward and sum operations required to compute the intermediate values.

3.3.4 Final Product Generation

The final 4-bit product (Pout) is computed using the weighted sum of the partial products:

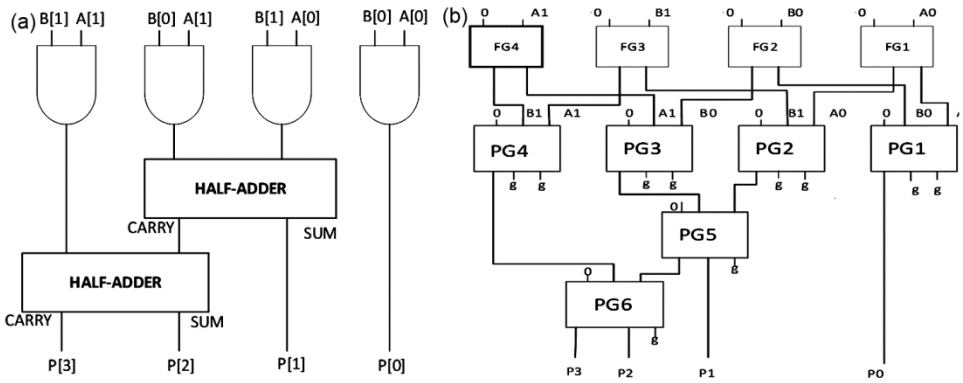

Fig. 5 — (a) Block diagram of 2x2-bit multiplier, (b) Implementation of 2x2-bit multiplier using RSOA-FG and RSOA-PG logic gates.

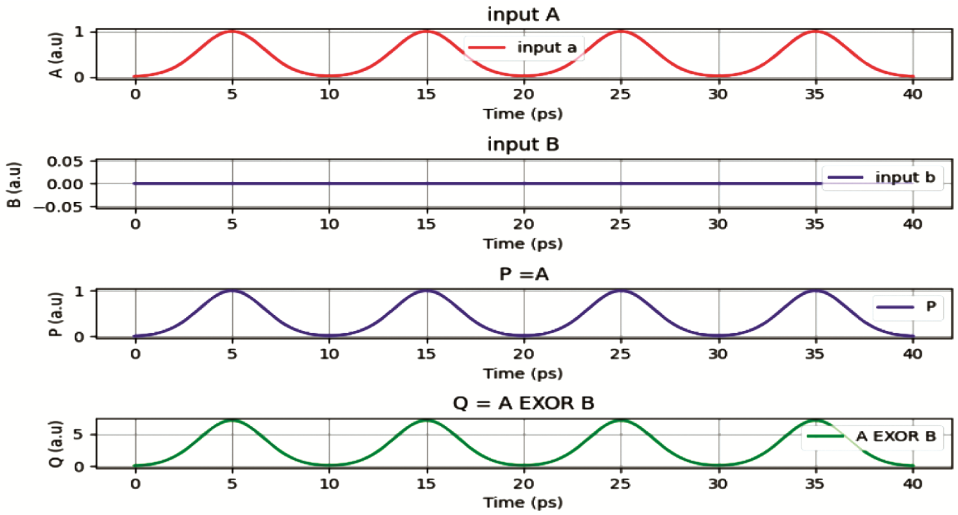

Fig. 6 — FG gate with inputs A = [1,1,1,1], B = [0,0,0,0] and outputs P = A [1,1,1,1], Q = A [1,1,1,1], generate copy of A.

$$\text{Pout} = [P_3 \ll 2 + (P_2 + P_1) \ll 1 + P_0],$$

where "≪" denotes a binary left shift operation to correctly align the partial products based on their significance.

The block diagram of the proposed 2×2-bit optical multiplier is illustrated in figure 5. The circuit is designed to be reversible with 10 constant inputs and 10 garbage outputs, ensuring no loss of information and maintaining reversibility throughout the computation process. The optical cost of the circuit is 44, while the optical delay is 10Δ.This approach is particularly suitable for high-speed optical computing, where the multiplication of binary inputs enabling efficient binary multiplication with minimal optical delay.

4 Simulation and Results

The simulation of the proposed 2×2-bit all-optical reversible multiplier was conducted using Python in a Jupyter Notebook environment. Figure 7 presents the simulated input-output waveform, illustrating the dynamic behavior of the optical logic circuit. The results demonstrate the correct generation of multiplication outputs for all possible input combinations, thereby validating the functional accuracy and feasibility of the design for high-speed optical computation. Moreover, the simulated outputs were systematically mapped to the expected results defined in the 2×2 multiplier truth table, as shown in Table 5, further confirming the logical correctness of the implementation. Notably, this all-optical design eliminates the need for intermediate electrical conversions, leading to improved energy efficiency and reduced latency in signal processing.

In optical communication systems, key performance metrics such as Extinction Ratio (ER), Q-factor and Relative Eye Opening are used to evaluate signal quality and system efficiency. Extinction Ratio (ER) measures the ratio of the optical power in the logic '1' state to the logic '0' state, indicating the effectiveness of signal transmission. A

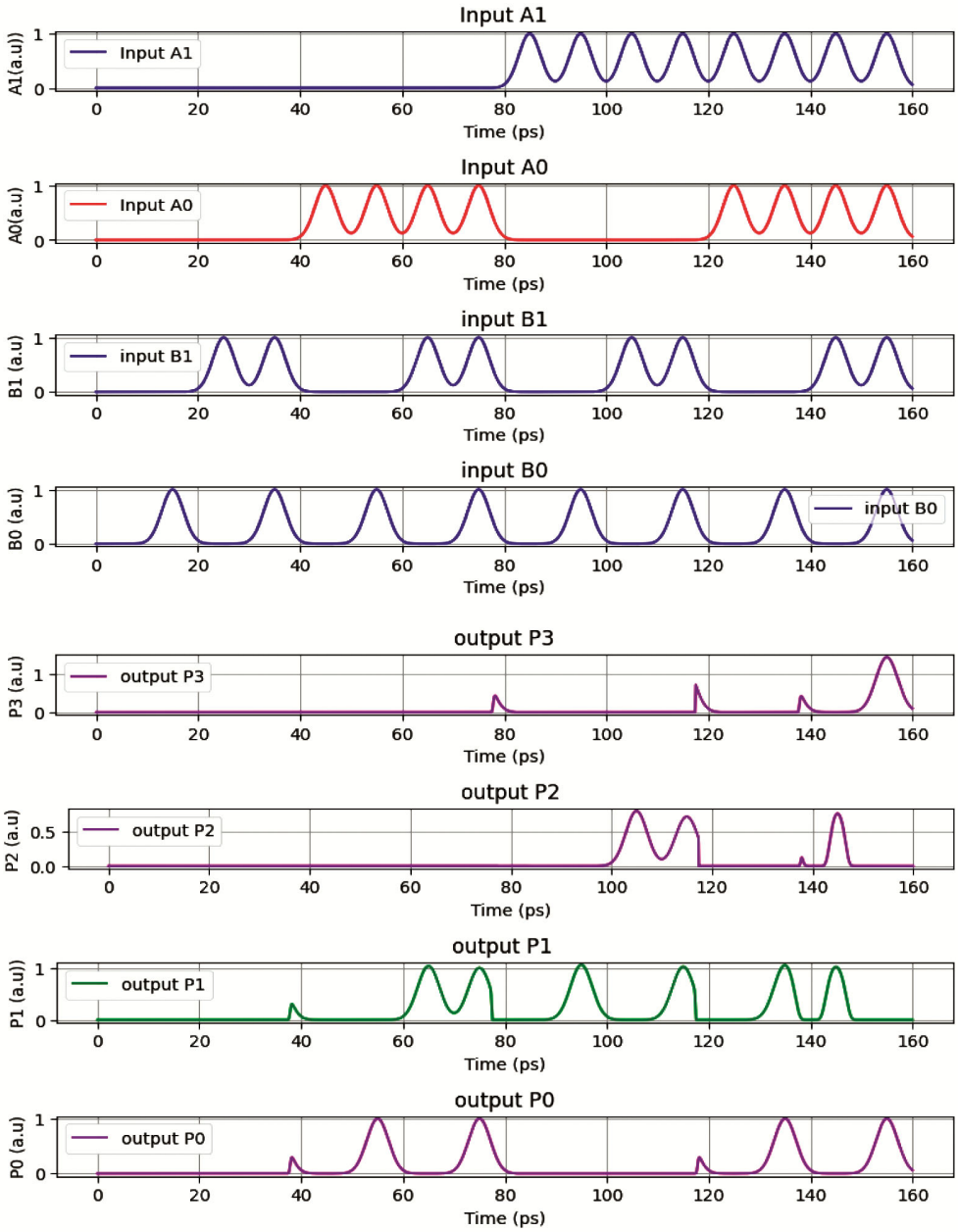

Fig. 7 — Simulation waveform of the 2x2-bit multiplier

higher ER ensures better signal differentiation, reducing bit errors. The Q-factor is a statistical measure derived from signal noise characteristics and is defined as the ratio of the difference between mean power levels of '1' and '0' states to the sum of their standard deviations. A higher Q-factor represents improved signal integrity and lower bit error rates (BER). Relative Eye Opening (REO) is a normalized measure of the vertical eye opening in an eye diagram, used to assess the quality of an optical signal. It indicates how much margin is available for signal detection and helps in evaluating the robustness of the transmission system. A wider eye opening indicates less inter-symbol interference (ISI) and a robust signal with minimal noise. These parameters collectively define the performance of an optical circuit, ensuring high-speed and low-error data transmission in photonic computing and optical communication applications.

To assess the impact of varying input conditions, the extinction ratio (ER), Q-factor, and relative eye opening (REOP) were evaluated for three different

Table 5 — Truth Table of 2x2- Multiplier

INPUTS				OUTPUTS			
A1	A0	B1	B0	P3	P2	P1	P0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

injection currents: 180 mA, 190 mA, and 200 mA. These values correspond to practical operating regimes of RSOA devices and provide insight into the circuit's performance under varying power conditions. Figure 8 shows the variation of ER as a function of control energy for different injection currents. Figure 9 illustrates the corresponding Q-factor behaviour under similar conditions. Figure 10 presents the REOP trends, indicating how signal clarity evolves with increased control energy.

Across all metrics, the results demonstrate improved performance with higher injection current, highlighting the potential of tuning RSOA operating parameters for optimal gate performance.

The performance of the proposed 2×2-bit optical multiplier was evaluated at data rate of 100Gbps. At an injection current I = 200 mA and control energy Ec = 20fJ, The parameters used in the calculations are given in Table 6.

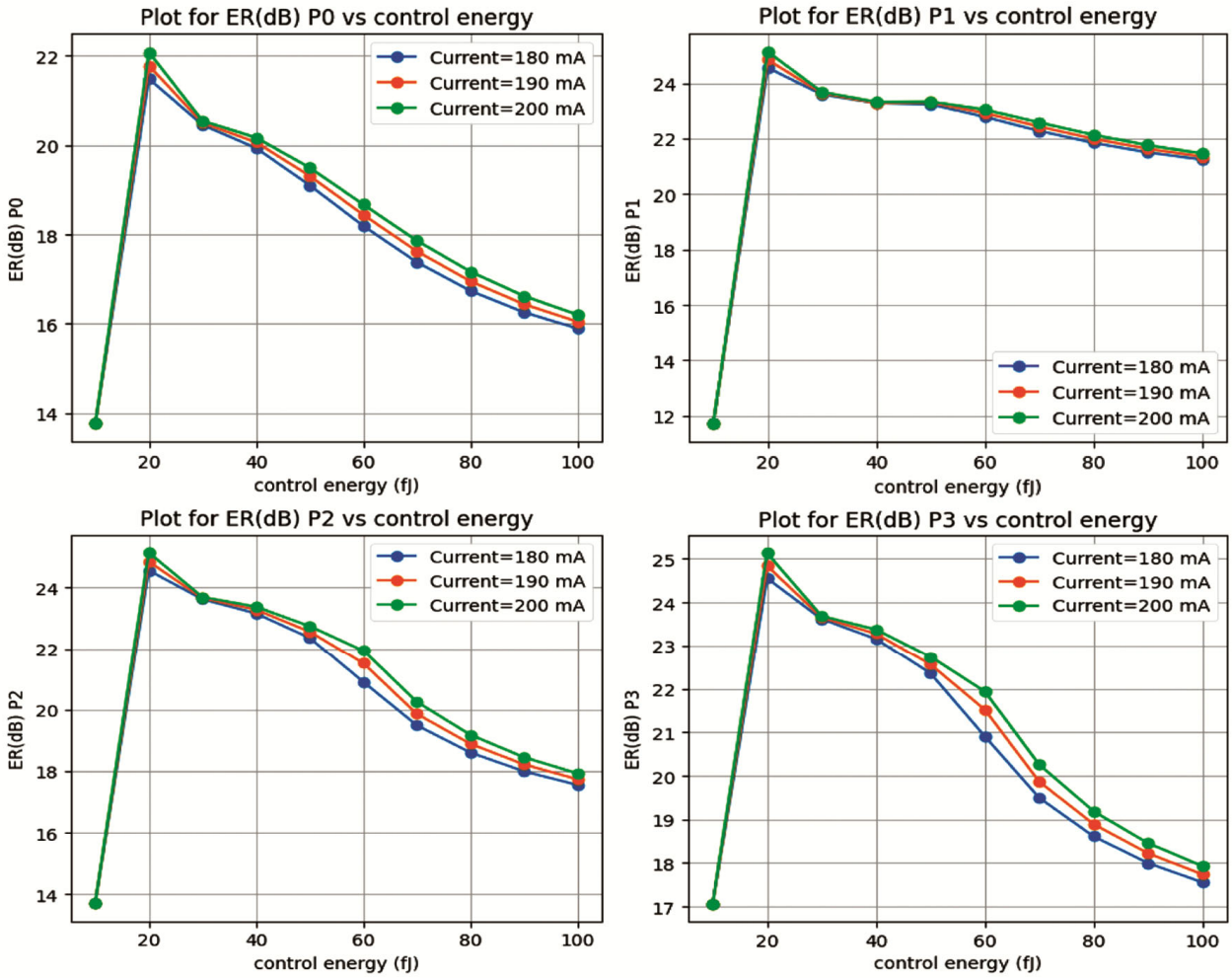

Fig. 8 — Plot of Extinction Ratio (ER) vs. Control Energy (Ec) for outputs P0, P1, P2, and P3

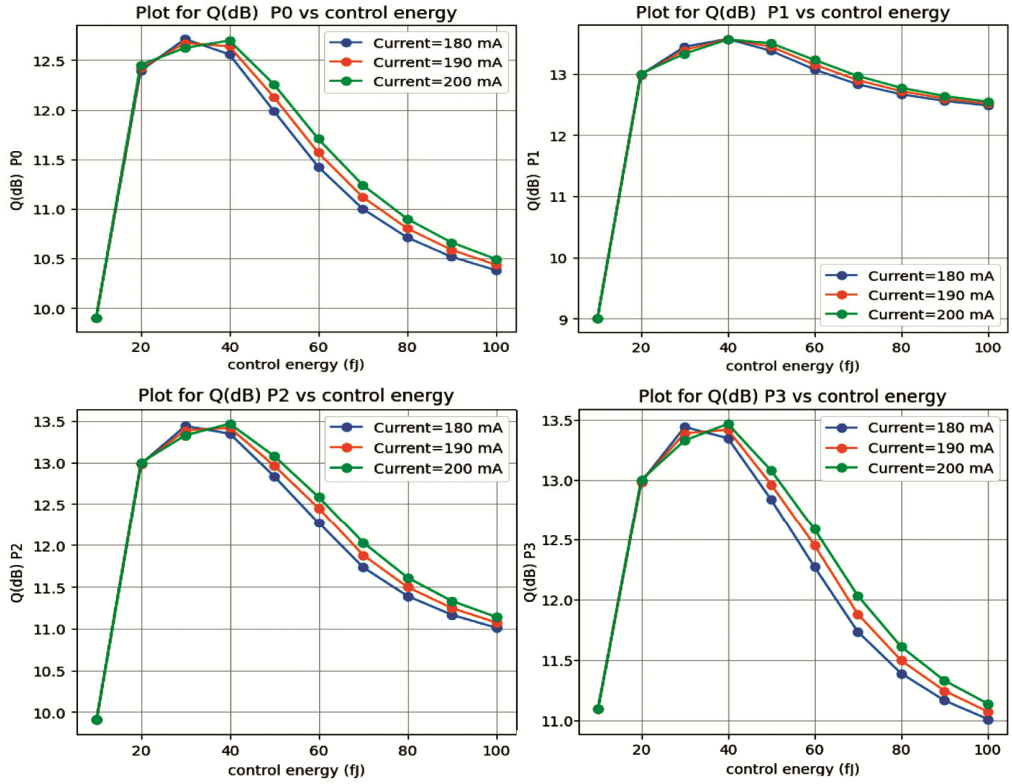

Fig. 9 — Plot of Q-factor (Q) vs. Control Energy (Ec) for outputs P0, P1, P2, and P3

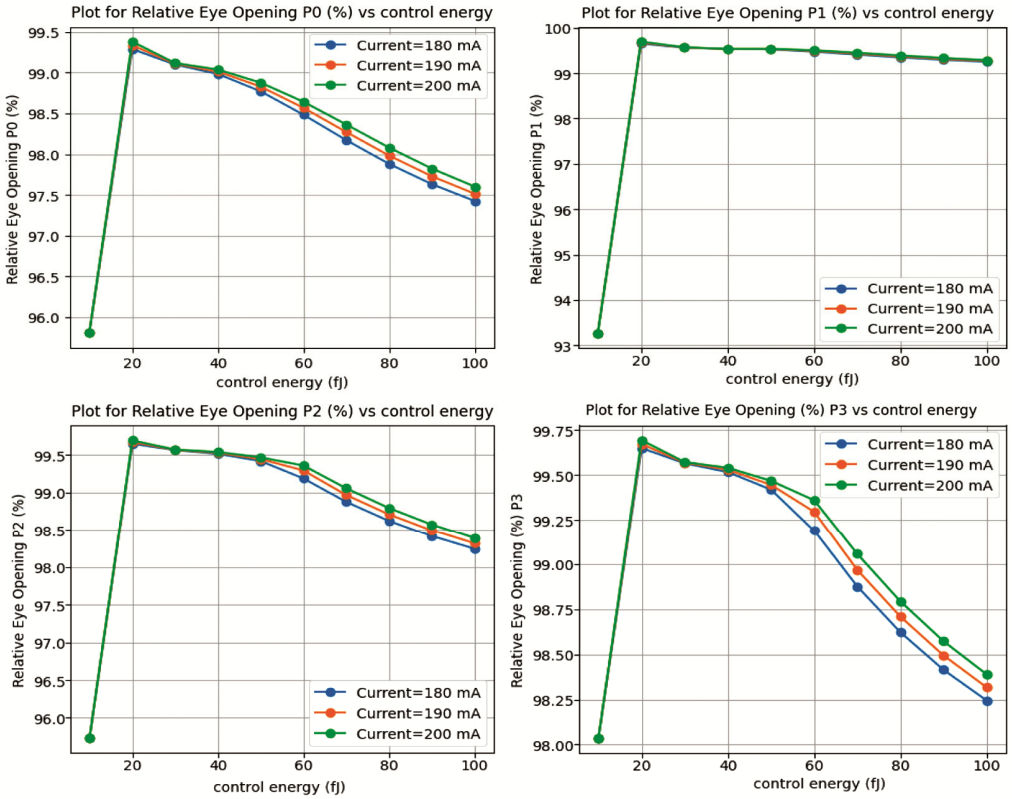

Fig. 10 — Plot of Relative Eye Opening (REOP) vs. Control Energy (Ec) for outputs P0, P1, P2, and P3

P_0: ER = 22.48 dB, Q = 12.4, REOP = 99.46%

P_1: ER = 25.45 dB, Q = 13.0, REOP = 99.76%

P_2: ER = 25.75 dB, Q = 13.1, REOP = 99.74%

P_3: ER = 25.18 dB, Q = 13.0, REOP = 99.65%

The obtained results provide critical insights into the circuit's signal integrity and optical switching efficiency. The high ER values indicate a strong contrast between logical '0' and '1', ensuring efficient optical signal modulation. The Q-Factor suggests low bit error rates (BER), which is crucial for maintaining the reliability of optical computation. Additionally, the high REOP percentages (above 99%) demonstrate minimal distortion and inter-symbol interference, thereby confirming the circuit's ability to sustain signal clarity and transmission accuracy. The formula of ER, Q-factor, Eye Opening is given in Table 7.

As shown in the figure, these performance metrics gradually decline with increasing control energy. This degradation is primarily due to the gain saturation effect in the RSOA, where higher control energy reduces amplification efficiency, thereby impacting signal quality. Additionally, ER, Q, and REOP values may vary slightly across different input bit sequences since each input combination generates different output power levels due to the nonlinear effects in RSOA circuits. Certain logic states may experience higher losses, leading to a lower ER and Q, highlighting the circuit's sensitivity to the input data pattern. Table 8 presents a comparison between the proposed work and existing approaches reported in the literature.

Overall, the results confirm that the proposed all-optical 2×2-bit reversible multiplier maintains high performance and signal fidelity while exhibiting sensitivity to control energy, injection current and input variations. These findings highlight its potential for high-speed optical computing applications, where efficient signal processing with minimal distortion is essential.

Table 6 — Parameter used in simulation

Symbol	Parameter	Value
Γ	Confinement factor	0.48
c	Velocity of light	3×10^8m/s
I	Injection current	200 mA
αN	Differential gain	$3.3 \times 10^{-20}\ m^2$
N_t	Carrier density at transparency	$1 \times 10^{24} m^{-3}$
w	Width of the active region	1.5 μm
d	Depth of the active region	250 nm
L	Active length	150 μm
α_D	Internal loss of the waveguide	2700 m^{-1}
λ	Wavelength of light	1550 nm
E_c	Control pulse energy	20fJ
τ_{FWHM}	Full-width at half-maximum	5 ps
n_2	Nonlinear coefficient	$2.6 \times 10^{-20}\ m^2/w$
D	Dispersion constant	1 ps/(nm km)
A_{eff}	Fiber effective area	$5 \times 10^{-13}\ m^2$
Es	Saturation energy	25fJ
b0	Optical bandwidth	3 nm
n_{sp}	ASE factor	2
B	data rate	100 Gbps

Table 7 — Formula of ER, Q-factor, Eye Opening

Parameters	Formula
Extinction Ratio (ER)	$\mathrm{ER} = 10 \log_{10}\left(\frac{P_1}{P_0}\right)$
Q-Factor (Q)	$Q = \frac{\mu_1 - \mu_0}{\sigma_1 - \sigma_0}$
Relative Eye Opening (REOP)	$REOP(\%) = \left(\frac{P_{max} - P_{min}}{P_{max}}\right) \times 100$

Table 8 — Comparison of proposed design with existing optical multiplier architectures

Reference	Technology Used	ER (dB)	REOP (%)	Q(dB)	reversible
[18]	Semiconductor Optical Amplifier—assisted Sagnac Switch	25.16	Not calculated	Not calculated	no
[19]	Polarization Switch	Not calculated	Not calculated	Not calculated	no
[20]	Micro-ring resonator	12.9	Not calculated	Not calculated	no
[21]	Photonic Crystal Structure.	8.82	Not calculated	Not calculated	no
[22]	MIM Waveguides	Not calculated	Not calculated	31.31	no
[23]	SPP technology	Not calculated	Not calculated	Not calculated	no
Our work	Reflective Semiconductor Optical Amplifier	25.89	99 (approx.)	13.46	yes

5 Conclusion

The analysis of the all-optical 2×2-bit reversible multiplier based on RSOA-based logic gates demonstrates its effectiveness in optical signal processing. The results confirm that the circuit achieves high ER, Q, and REOP values, indicating strong optical contrast, low bit error rates, and minimal signal distortion. However, the performance is sensitive to control energy variations due to gain saturation in the RSOA, leading to a decrease in ER, Q, and REOP with higher control energy. Moreover, different input combinations may slightly affect the optical measuring parameters, highlighting the influence of input bit sequences on the multiplier's performance.

Despite these variations, the circuit maintains high performance, making it suitable for high-speed, low-power optical computing applications. The design is modular and readily scalable to higher-bit multipliers with minimal architectural changes, supporting its integration into more complex optical arithmetic units. Future work can explore optimized gain management techniques and improved energy efficiency strategies to further enhance the robustness and scalability of the proposed design.

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