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Numerical Simulation and Optimization of a Novel Dopingless Vertical Nanowire TFET for Low Power Memory Applications

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The use of portable devices has significantly increased in today's life, due to this the performance parameters of low power application devices are the key feature to notice. Dopingless devices are the new attracting techniques for low power applications and high I_{ON} / I_{OFF} factor. The nanowire devices utilize the gate control over the channel to reduce OFF current in the device and vertical structure of device helps to enhance the tunnelling mechanism in tunnel FETs. In this work a dopingless vertical nanowire tunnel FET is designed and simulated. The simulation results are showing charge plasma dopingless VNWTFET in both P-type and N-type, performance characteristics like drain current (I_D), transconductance (g_m), gate to drain capacitance (C_{GD}), gate to source capacitance (C_{GS}), total gate capacitance (C_{GG}), cut off frequency (f_T), energy, potential, electron and hole concentration, electric field, electron band to band tunnelling. Then the 6T CP-VNWTFET based SRAM circuit is demonstrated. The analysis of circuit shows that circuit of SRAM designed by 6T CP-VNWTFET gives preferably superior signal to noise margin like RSNM of 376.43mV and WSNM of 433.35mV at V_{DD} = 1.0V; also, a reduced read delay as 4.1ns and write delay as 0.18ns when compared with conventional 6T TFET and 7T TFET device-based SRAMs. The leakage power of proposed device-based SRAM circuit is also showing better performance at all the voltage range.

Keywords: Charge plasma, SRAM, Noise margin, Standby power, CP-VNWTFET, Butterfly curve

1 Introduction

In the past few years, the technologies are narrowing at very fast rate, so the silicon devices are moving towards nanoscale regime[1-4]. As a result, the required supply voltage is also reduced prominently, as a lot of devices are employed on a solitary chip. As the scaling of the devices goes beyond 32nm technology[5-8], the circuit designing is facing certain problems, like static power consumption and stability of the system. A large number of devices like MOSFETs[9-11], TFETs[12-20], and JLFETs[21] are investigated and some of the problems were found while analysing. The scaling down in conventional MOSFETs creates the problems like higher subthreshold swing (SS) and higher off current. Also, some short-channel effects (SCE)[22-27] arise like a situation of threshold voltage roll off[28-30] and drain-induced-barrier-loss (DIBL)[31-32]. As a replacement TFETs came into the market, but the off current was high due to only one gate in conventional TFETs and double gate TFETs DG-TFETs [33], so the gate is formed all around the channel to get better control over the device and reduce the leakage current as well as leakage power. In conventional nanowire TFETs the tunnelling is lesser; to increase the tunnelling the architecture of the device is changed to vertical architecture. Now the tunnelling in device and the drain current is enhanced significantly in vertical NWTFETs. At the time of doping in the devices the problems like random-dopant-fluctuation (RDF) and expensive-thermal-budgeting (ETB) occurs. To avoid these problems, dopingless devices are approached and the doping is achieved by charge plasma[34-35] or electrostatic[36-38] technique. Fabrication of dopingless vertical nanowire structures involves few challenges such as achieving uniform material properties, precise gate control, low contact resistance, and effective surface passivation. Additionally, techniques for consistent nanowire growth and precise etching at small scales are crucial for successful fabrication.

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Static Random-access Memory, commonly known as SRAM, which is mostly employed in electronic components, microprocessor, and other general computing applications[39-41]. While SRAM circuit is not requiring the dynamic refreshment and it is volatile memory, means if the power is switched off, the data will not be retained, and it will be vanished. The dynamic RAM circuit needs continuous refreshment, while SRAM does not require refreshment; it is a major advantageous feature of the SRAM circuit. Additionally, SRAM circuits are bigger than DRAM circuits in size, so the SRAM circuit is less expensive than DRAM[42]. In nanoscale technology, the stand-by power consumption is a significant problem. In the cache memory, a high amount of chip area, almost more than half is covered by SRAM. Few published research shows that a large amount of power (almost 40%-50%) consumed in any electronic circuitry is consumed by the memory only[43-45] nanoscale semiconductor devices (like NWTFETs) to design memory cell.

In this paper the N-type CP-VNWTFET[46] and P-type CP-VNWTFET are designed and analysed. Later the designing of SRAM circuit is performed. The designing of SRAM circuit using CP-VNWTFET is explored and analysed by utilizing the steeper sub-threshold slope for low power application. This paper also investigates the read and write stability as well as reliability of SRAM circuits based on 6T CP-VNWTFET, 6T TFET[47] and 7T TFET[48]. It also analyses the standby leakage power dissipation of the devices.

2 Device Structure and Simulation Parametrs

A cross-section view of N-type and P-type charge plasma based vertical nanowire tunnel FET is show in Fig. 1(a-b), respectively. The N-type CP-VNWTFET consists of P^+ region as source, intrinsic (i) as channel and N^+ region as drain, while P-type CP-VNWTFET consists of N^+ region as source, intrinsic (i) as channel and P^+ region as drain. The 3D structure of CP-VNWTFET is shown inFig. 1 (c). The gate work (ϕ_G) for N-type CP-VNWTFET is 4.2eV, whereas it is changed suitable to 5.2eV to design P-type CP-VNWTFET. In N-type CP-VNWTFET platinum was used as source-metal with a work function (ϕ_S) of 5.93eV and hafnium as drain having work function (ϕ_D) of 3.9eV. In the P-type CP-VNWTFET the work functions of drain and source-metals are interchanged, so that the drain can become P^+ doped and source will be N^+ doped. The channel length (L_C) for N- channel and P- channel CP-VNWTFET is taken as 20nm, while the drain length (L_D) and source length (L_S) is 10nm. The radius of intrinsic substrate (R) is 7.5nm. Initially the substrate was intrinsic or had a doping concentration (N_D) of 1×10^{15} cm^{-3}. The gate oxide is SiO_2 with a thickness (t_{OX}) of 2nm for both N- channel and P- channel CP-VNWTFET, as mentioned in Table 1.

Design and simulations of the devices are performed using Silvaco ATLAS TCAD simulator. At the time of device simulation, the nonlocal BTBT model is invoked to accelerate the tunneling spatially

Table 1 — Parameters and Specifications of N-type CP-VNWTFET and P-type CP-VNWTFET

Parameters	N-type CP-VNWTFET	P-type CP-VNWTFET
Channel Length (L_C)	20nm	20nm
Drain Length (L_D)	10nm	10nm
Source Length (L_S)	10nm	10nm
Radius of intrinsic substrate (R)	7.5nm	7.5nm
Doping Concentration (N_D)	Intrinsic	Intrinsic
Gate Work Function (ϕ_G)	4.2eV	5.2eV
Source Work Function (ϕ_S)	5.93eV	3.9eV
Drain Work Function (ϕ_D)	3.9eV	5.93eV
Gate Oxide Material	SiO_2	SiO_2
Gate Oxide Thickness (t_{OX})	2 nm	2 nm

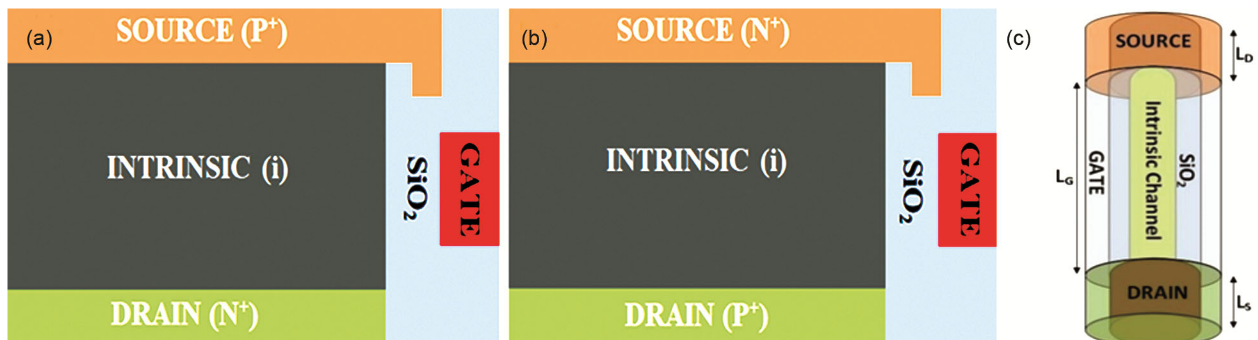

Fig. 1 — Cross-sectional view of (a) N-type CP-VNWTFET and (b) P-type CP-VNWTFET, and (c) 3D view of CP-VNWTFET

with the help of Wentzel Kramers Brillouin WKB approximation. A model to get narrower bang-gap, SRH recombination is also introduced to get the source and drain highly doped. In this simulation the leakage of the channel region is considered as zero. The calibration is done for vertical gate-all-around in TFET, which helps to acquire a better range of electric field in the tunneling area. On the other side, the bending of energy bands on source channel interface is raised; therefore, the barrier on tunneling is reduced. Due to these factors, the on current in device is increased as well as the subthreshold slope (SS) is decreased significantly. Here a Fermi Dirac Statical model is applied to get a reduced carrier concentration in heavily doped region.

On performing the simulation electron and hole concentration contour plot of for N-type and P-type CP-VNWTFET are represented in Fig. 2 (a-d) respectively. From these figures, it is easily understandable the achievement of N-type CP-VNWTFET and P-type CP-VNWTFET. Here the doping is dependent of metal used for source and drain. As mentioned in Table 1, for N-type CP-VNWTFET platinum was used as source-metal with a WF (ϕ_S) of 5.93eV and hafnium as drain-metal with a WF (ϕ_D) of 3.9eV. Its effect is visible in Fig. 2(a-b), that an electron cloud (an spatial region with a high density of electrons) is formed near drain-metal and holes are collected near source-metal with uniformity. On the other hand, when the metals are interchanged; platinum is used as drain-metal and hafnium is used as source-metal to design P-type CP-VNWTFET, the position of electron and hole clouds are also interchanged.

3 Device Simulation Results and Discussion

Here, the N-type CP-VNWTFET and P-type CP-VNWTFET are analyzed, and performance characteristics (analog parameters and structural parameters) are plotted. In N-type device the V_{GS} is applied from 0V to 1V, while in P-type device applied V_{GS} is 0V to -1V. In all the characteristics the left side with negative gates to source voltage the performance parameters are for P-type CP-VNWTFET (in Pink, Cyan and Blue Color) and in right side with positive gate to source voltage the performance parameters are for N-type CP-VNWTFET (in Green, Red and Black Color). The characteristics are drawn at different values of positive V_{DS} (0.1V, 0.5V & 1V) for N-type device and negative V_{DS} (-0.1V, -0.5V & -1V) for P-type device. The drain current with respect to V_{GS} is shown on Fig. 3(a). For P-type device the drain current flow in opposite direction from source to drain, and for N-type it flows from drain to source.

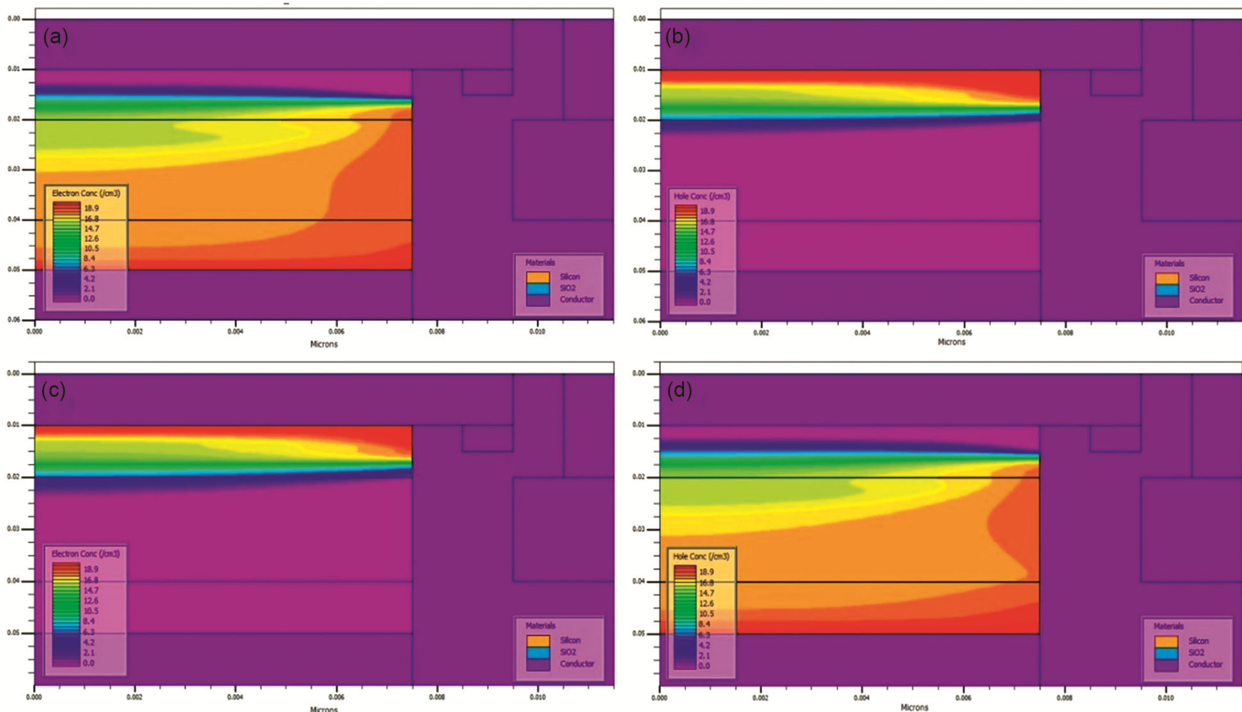

Fig. 2 — (a) Electron and (b) hole concentration for N-type CP-VNWTFET, (c) Electron and (d) hole concentration for P-type CP-VNWTFET

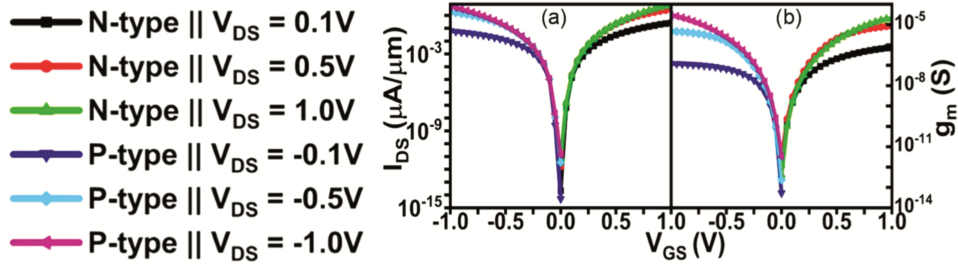

Fig. 3 — (a) Drain current, and (b) transconductance for N-type CP-VNWTFET and P-type CP-VNWTFET

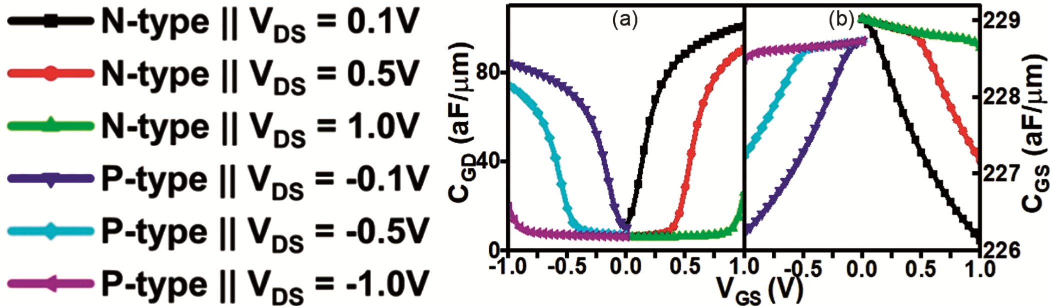

Fig. 4 — (a) C_{GD}, and (b) C_{GS} for N-type CP-VNWTFET and P-type CP-VNWTFET

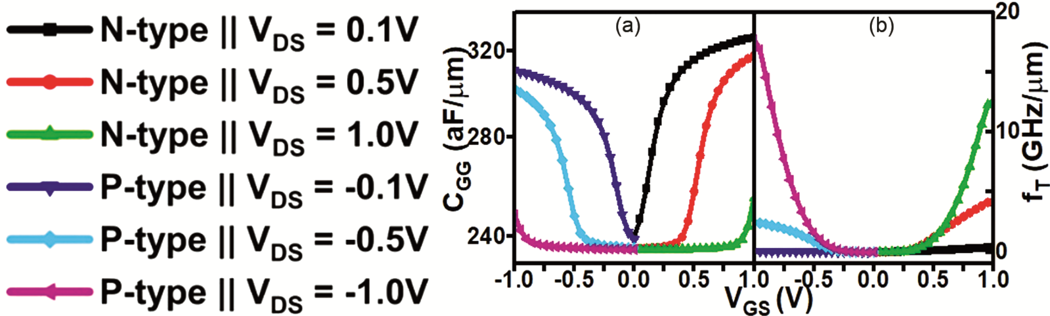

Fig. 5 — (a) C_{GG}, and (b) f_T for N-type CP-VNWTFET and P-type CP-VNWTFET

The ON current for device is 0.27μA, 2.99 μA and 6.78 μA for N-type device at 0.1V, 0.5V and 1.0V drain voltage. On the other hand, for P-type device the ON current is 0.06μA, 1.83μA and 4.92μA at -0.1V, -0.5V and -1.0V drain voltage. Figure 3(b) shows the transconductance for both the devices. Similar to drain current it is maximum for -1V in case of P-type device and +1V for N-type device.

C_{GD} is also known with the name of feedback-capacitance and reverse-transfer-capacitance. It is observed that if the value of C_{GD} is higher, the drain current can face a delay in rise after applying gate voltage. Also, the fall in drain current is delayed after removing the gate voltage. It can also be stated that C_{GD} acts as very important factor in switching speed of the device, so this parameter should be as low as possible. In Fig. 4(a) it can be observed that as V_{DS} increases from 0.1 to 1.0V for N-type device, C_{GD} is degrading. Similarly, if V_{DS} is changed from -0.1 to -1.0V for P-type device, C_{GD} is again reducing. Its effect is visible in Fig. 3(a), where ON current is max when C_{GD} is min. An electric field used to occur between the positive charge carrier's ant gate and negative charge carriers at channel. Due to this electric field a capacitor shows its existence between gate and channel. The capacitance of this capacitor is known as gate to source capacitance or gate to channel capacitance. Figure 4(b) is showing the C_{GS} at distinguish values of V_{DS} for the devices. It is exhibiting the max C_{GS} at V_{DS} = +1.0V for N-type device and min C_{GS} at V_{DS} = -1.0V for N-type device. C_{GG} is calculated by adding the C_{GD} and C_{GS}, as it is the total gate capacitance of the device. Figure 5(a) is displaying the analysis of C_{GG} of both the devices. Figure 5(b) shows f_T in GHz for both the devices with respect to V_{GS} at various range of V_{DS}. This parameter

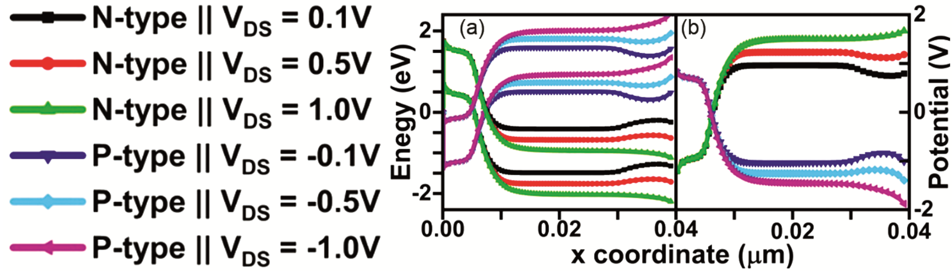

Fig. 6 — (a) Energy, and (b) Potential for N-type CP-VNWTFET and P-type CP-VNWTFET

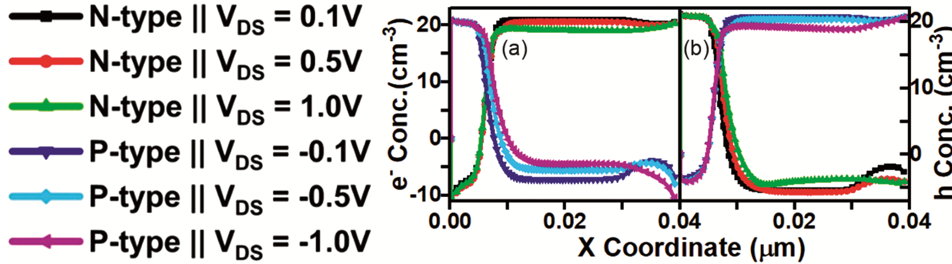

Fig. 7 — Carrier concentration of (a) electron, and (b) hole for N-type CP-VNWTFET and P-type CP-VNWTFET

is calculated by the formula - gm /2π C_{GG}. It reduces as C_{GG} goes high, as f_T is inversely related to C_{GG}; but it is found that gm is max at +1.0V for N-type device and at -1.0V for P-type device; so, the values of f_T is also max for the same inputs.

The charge carriers use to start their tunneling in only one condition when conduction band (CB) at source side gets in the alignment of valence band (VB) at channel. In the device CP-VNWTFET (with vertical architecture) the tunneling is happening vertically. So, the area exposed or responsible for tunneling is larger as compared to lateral devices. The tunneling distance or gap is shortest at the source channel interface, and this shortest distance has played a key role in getting a reasonable amount of tunneling current for the devices. V_{GS} also affects the tunneling phenomenon significantly as observed in Fig. 6(a). When V_{GS} is low, the bending of CB and VB is very small. So, the drain current is also significantly high; the reason is that the alignment is not achieved between CB at source side and VB of channel. Bending of energy bands in the semiconductor devices is also evaluated as term of surface potential of the TFET devices. The potential is inversely proportional to the banding of energy bands, which is clear from Fig. 6(b). In the channel, the potential varies with a factor of unit band gap energy per elementary charge (Eg/q). In this paper a dopingless VNWTFET is doped by using charge-plasma technique to escape the problem raised while doping like RDF (random dopant fluctuations) and expensive thermal budgeting etc. The electron concentration for N-type device is lowest near the source-metal, as a cloud of electron is formed near drain-metal due to low WF metal at drain side. The electron concentration uses to rise after source channel interface as shown in Fig. 7(a). On the other hand, the electron concentration for N-type device is highest near source-metal and it rises after source channel interface because the metals for source and drain are interchanged. Figure 7 (b) displays the hole concentration is opposite to the electron concentration for both the devices. But it is very clear from the graph that there is no fluctuation in doping in the whole device.

In the TFETs, the flow of the charge carriers (electron in the case of N-type and holes for P-type) is changed by the produced electrical field by a V_{GS}. Figure 8(a) shows the electric field of the N-type and P-type devices by varying the device length from source to drain side. For both the devices the electric field is min near source-metal and then starts increasing. The value of electric field is max at source-channel interface; while after the interface it reduces. The electric field is majorly affected by V_{DS}, as at V_{DS} = +0.1V (for N-type device) and -0.1V (for P-type device) it is highest in channel region; at V_{DS} = +0.5V (for N-type device) and -0.5V (for P-type device) it is reduced and it is having a min value at V_{DS} = +1.0V (for N-type device) and -1.0V (for

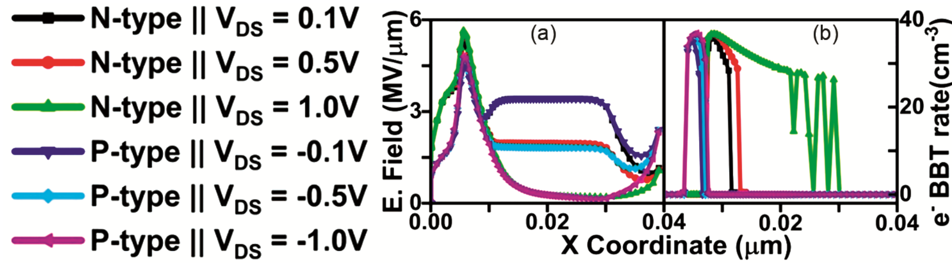

Fig. 8 — (a) Electric field, and (b) electron BBT for N-type CP-VNWTFET and P-type CP-VNWTFET

P-type device). TFETs are the device with region of p-i-n like diode, but it works like a transistor because of tunneling of charge carriers over the barrier. This phenomenon is known as band to band tunneling (BTBT). In the TFET device V_{GS} is applied for accumulation of electrons for N-type TFET and accumulation of holes for P-type TFET. When a sufficient amount of V_{GS} is applied, CB of intrinsic region gets aligned with VB of P region and BTBT occurs. Figure 8 (b) is showing the rate of electron transition rate or band to band tunneling rate of electron with respect to the device length in µm.

4 Result Analysis

4.1 6T CP-VNWTFET Based SRAM Design

Figure 9 shows the 6T-SRAM circuit based on CP-VNWTFET, this circuit is implemented by four N-type CP-VNWTFETs and two P-type CP-VNWTFETs. The designing of 6T-SRAM circuit is performed by programming in Smart-Spice tool. First of P-type and N-type devices were designed shown in Fig. 1(b&c); then the .tbl files (look up tables) were created for I_D, C_{GS} and C_{GD} for both the devices. Thereafter, the Verilog-A model with extension of .va is used to analyze the circuit behaviour and finally the .sp file is used to design the circuit of 6T-SRAM. The circuit is having two inverters connected in back-to-back arrangement (means the output of inverter1 is connected as input of inverter2 and vice versa); these inverters are made by two N-type CP-VNWTFETs (labeled as T1 & T2) and two P-type CP-VNWTFETs (labeled as T3 & T4). These two inverters are connected to bit-line (BL) and bit-line-bar (BLB) via the access transistors T6 and T5 respectively. The word-line (WL) is used to turn on the access transistor T5 and T6 to perform the read and write operation. In the read operation node Q and Q-bar (Q' or QB) are used as output node.

Basically, SRAM can perform 3 operations- hold, write and read operations. When WL is connected to ground, the access transistors T5 and T6 becomes in OFF state. Then BL and BLB also come to OFF state, and the memory cell reach to the hold state. In the hold condition, data is latched between both the inverters. If Q is at '0', it will remain at '0' and QB will remain at '1'. To perform any other operation like read and write operation; WL is kept high, so that access transistors become in ON state.

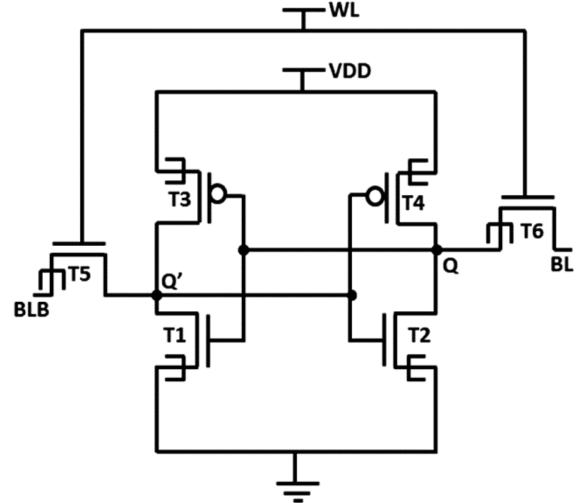

Fig. 9 — Proposed SRAM circuit design using 6T charge plasma based vertical nanowire TFET

4.2 Read Operation

In the read operation, the memory cell should retain some value; so, let's assume that Q is at 1 and QB is at 0. Now change the state of WL from 0 to 1, for read operation. Here BL and BLB will work as the output nodes, and these are initially pre-charged due to a connection of voltage VDD at BL and BLB. As assumed earlier, Q is at 1; so, there is no discharge in the circuit between BL and Q node. But QB is at 0 and BLB is 1, so there is a voltage difference between both the nodes QB and BLB, therefore voltage at BLB will decrease. Due to this reason, there is a discharge in the circuit and the current will start flowing. Here BL and BLB nodes are connected to sense amplifier, which will act as a comparator; so,

when BLB is low the output is 1. Hence it can be stated that input the input at node Q was 1 and the output we got on node BL is also 1. Similarly, if we consider Q at 0 and QB at 1 in the SRAM circuit, also BL and BLB are connected to VDD i.e. 1. This time the discharge will occur between Q and BL, as there is a voltage difference. Now BL will decrease and the output at node BL will be 0, in the condition when applied input at Q is 0. Therefore, the read operation is verified in both the cases when input at Q is 0 or 1.

4.3 Write Operation

For the write operation, let's assume that the SRAM has Q at 0 and QB at 1. In starting, WL is kept at 1 to perform the write operation successfully. For the write operation the nodes BL and BLB are considered as input nodes, as we can control these nodes. Initially the BLB node is connected to ground to generate a voltage difference between QB and BLB. To write logic 1 in SRAM, T2 should be stronger than T4, it can only get by varying the aspect ratio of the TFETs. So, Q will become at 1. As it is found that in before write operation, Q was at 0 and after the operation, it became 1. Therefore, we can state that the write operation is performed successfully.

4.4 Butterfly Curve for SRAM Circuit

The SRAM circuit is considered an excellent circuitry to analyze the interaction of device and circuit. For this analysis the proper realization of SRAM memory element is necessary. To achieve it, stability must be realized by static noise margin (SNM). The SNM is nothing but the maximum noise voltage that the circuit can bear without degrading its performance[49-50]. The SNM was calculated using the standard butterfly curve method, which is based on plotting the voltage transfer characteristics (VTCs) of the cross-coupled inverters. First, the VTC is plotted by sweeping the voltage at node Q and measuring the response at node QB, placing Q on the x-axis and QB on the y-axis. Then, the curve is mirrored by swapping axes-plotting QB on the x-axis and Q on the y-axis. This creates the characteristic butterfly shape. The largest possible square that can fit between the two lobes of the butterfly curve and is tangent to the unity gain (45°) line is constructed[51-53]. The side length of this square represents the static noise margin. The diagonal of this square is measured and used to quantify the SNM in millivolts (mV) as shown in Fig. 10 (a-b). This process is repeated under read and write conditions to extract the Read SNM (RSNM) and Write SNM (WSNM), respectively. The procedure ensures a consistent and comparative evaluation of SRAM stability under different operations. Figure 10 (a–b) is showing the butterfly curve (SNM) for read and write operations for SRAM circuit by 6T CP-VNWTFET.

4.5 Stability of SRAM Circuit

Stability for both read and write operations is the most preferable factor to encounter a victorious realization of SRAM circuit. The RSNM and WSNM is the most recommended component to estimate the stability of SRAM circuit. RSNM for proposed SRAM circuit is analyzed at the supply voltage V_{DD} = 1.0V and compared with other SRAM circuits published previously like SRAM based on 6T TFET [47] and 7T TFET [48], where the 6T and 7T SRAM cells are designed using tunnel FET structure. The comparison of RSNM (in mV) for all three SRAMs is displayed Fig. 11 (a). Here it can be observed that RSNM for proposed SRAM circuit is highest in comparison of other devices-based SRAM. Similarly, WSNM for proposed SRAM and others at V_{DD} =1.0V is shown in Fig.11 (b). WSNM for proposed device-based SRAM is higher than that of 6T TFET [47] and 7T TFET[48] both. So finally, it is concluded that the proposed device is showing the best stability as compared to 6T TFET and 7T TFET.

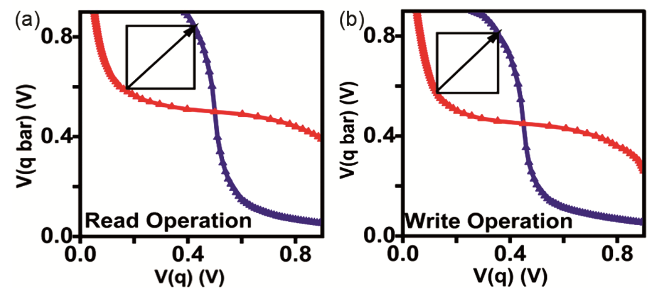

Fig. 10 — Butterfly curve for (a) read, and (b) write operations

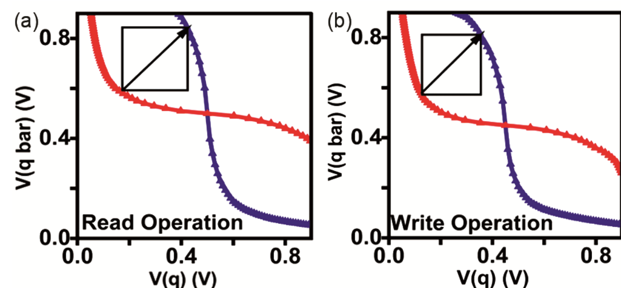

Fig. 11 — (a) RSNM, and (b) WSNM for different SRAM circuit at V_{DD} = 1.0V[47-4]].

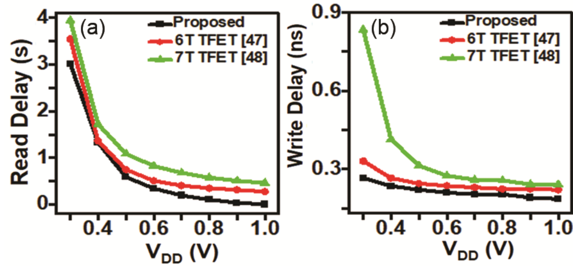

Fig. 12 — (a) Read Delay and (b) Write Delay for different SRAM circuit[47-48]

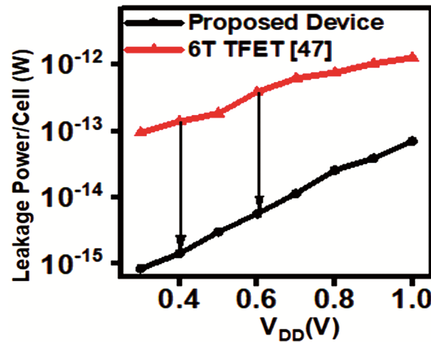

Fig. 13 — Leakage Power in SRAM circuit based on 6T CP-VNWTFET and 6T TFET[47]

4.6 Performance of SRAM Circuit

Delay in any circuit is very important component to measure the performance of any circuit, it is basically the difference of time when input is applied, and the output is achieved. In SRAM circuit, there are two different kinds of time delays to analyse, read delay and write delay. In the TFET based SRAM circuits, read delay is the time between 50% of WL activating till 10% of pre-charged voltage difference in BL. In Fig. 12 (a) the read delays for different SRAM designs are shown and it is observed that at low voltages like 0.3V to 0.7V, the proposed SRAM design is having lesser delay as compared to SRAM circuit based on 6T TFET and 7T TFET at all the ranges of VDD. The write delay for SRAM circuit is considered as the time gap between 50% activation of WL to the time when value of Q is flipped to 90% of its previous value. Figure 12 (b) is showing the write delay for all four devices. And it found that SRAM circuit by 6T CP-VNWTFET is retaining the best delay as compared to other SRAM structure.

4.7 Power Consumption of SRAM Circuit

The static power consumption in the circuits occurs in the case when the device is on standby mode and in read operation in SRAM. Write operations, which contribute to dynamic power, occur infrequently and last for only 1 to 2ms. As a result, static power dominates the overall power profile of the system. Therefore, the static power is calculated and compared. The consumed power is calculated by multiplication of consumed current and applied voltage.

Figure 13 shows the power consumption of SRAM circuit based on 6T CP-VNWTFET and 6T TFET. From Figure it is observed that at SRAM circuit based on 6T CP-VNWTFET is having 98 times and 68 times better power dissipation at V_{DD} 0.4V and 0.6V, respectively. Therefore, it can be concluded that 6T CP-VNWTFET SRAM circuit should be used at 0.4V or 0.6V V_{DD} to gain low power consumption application.

5 Conclusion

Low power applications are increasing in demand nowadays. To achieve this requirement some factors are very important like low voltage and smaller chip size. In this paper 20nm technology is used to design proposed N-type and P-type CP-VNWTFET to reduce the chip size and to deploy a large number of transistors on a single chip. The analysis for performance parameters of these two devices is also performed. This device has an advantage to avoid the problems like RDF and ETB occurred during doping. This paper also demonstrates designing of a low power 6T SRAM based on proposed CP-VNWTFET. Then the analysis of the performance parameters like signal to noise margin for read and write operations, read delay, write delay and power dissipation is done. A comparison of these parameters is also conducted with previously published SRAM designs based on 6T TFET and 7T TFET. After comparison it is found that RSNM for the proposed SRAM circuit have 46% and 33% improvement as compared with 6T TFET and 7T TFET based SRAM circuit respectively. Similarly, WSNM for proposed SRAM circuit have 57% improvement as compared with 7T TFET at V_{DD} =1.0V. The CP-VNWTFET based SRAM also proved to have 80% and 23% better read delay and write delay than TFET 7T based SRAM. The superior SNM and reduced delay as well as power dissipation proves the proposed SRAM design better to replace the previous devices-based application also with reduced chip area.

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