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Exploring the Active Realization of Analog Multi-Level Memristors for Neuromorphic Applications

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This article presents a novel method for identifying analog memristor functions that enable multiple resistance levels with tailored switching parameters. These multi-level memristors hold potential applications in multi-bit memory systems, chaotic oscillators, and multi-level logic design. The proposed approach is based on constructing a Parameter vs. State Map (PSM), which can be designed to contain a specific number of stationary points along its curvature. The regions surrounding these stationary points serve as discrete resistance levels. Using this method, analog multi-level memristors can be realized with predefined switching characteristics, such as resistance margins and switching thresholds. Unlike conventional memristor emulators, which typically rely on monotonic memristance/conductance functions, the proposed approach enables precise control over resistance states. As a result, memristors developed through this method can replace complex, discrete-valued memristors in various applications. To validate the proposed concept, an OTA (Operational Transconductance Amplifier)-based emulator circuit has been designed and verified through PSPICE simulations, demonstrating the feasibility of the approach.

Keywords: Memristor, Analogue memristor, Multi-level memristors, Stationary points

1 Introduction

The memristor has been considered a prime contender for resistive- switching applications over the past decade[1–3]. The effective use of a memristor in these applications requires that it provide discrete resistance levels. This implies that the static characteristic (charge versus flux) of the memristor must be piecewise-linear**.** To achieve these characteristics, several complex architectures using digital techniques have been proposed to date[4–5].

However, many memristor architectures based on both circuits and materials exhibit a continuous type of memristive behavior**.** Nevertheless, the possibility of using analog memristors in memory and logic applications as an alternative to discrete-valued memristors has often been ignored. Consequently, most previously reported continuous memristors (whether solid-state architectures or circuit-emulated) are designed without considering the suitability of their realized conductance for switching applications. These architectures are based on conventional conductance (or memristance) functions[6–7]. Such functions are found to be monotonically increasing (or decreasing) with flux and exhibit small or large non-linearity. Due to this consistent monotonic nature, these functions lack stationary regions in which conductance exhibits minimal variation. If these unsystematically designed memristors are used for resistance switching, they will be highly sensitive to parameter variations and external noise, and may thus shift from the stored resistance level leading to volatility, i.e., erroneous switching.

To overcome the limitations of conventional conductance functions, this article proposes a method by which a conductance function G_m with desired switching properties and multiple conductance levels can be derived. The proposed method can be used to extract the conductance expression from given switching parameters: the Conductance Margin (G_{mar}, representing the difference between lowest and highest conductance levels) and switching thresholds $\varphi_1, \varphi_2, \varphi_3, \ldots, \varphi_m$.

Finally, the use of a realized three-level analog memristor emulator is demonstrated in an Amoeba-Learning neuromorphic circuit.

1.1 Proposed Algorithm to Find Out Desired Conductance Function

Let us consider a Conductance expression $G_M(\varphi)$ of nth order as follows;

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$$G_M = a_0 + a_1\phi + a_2\phi^2 + a_3\phi^3 + \dots\dots\dots \dots a_n\phi^n \quad \dots (1)$$

The $\varphi_1, \varphi_2\ \varphi_3 \dots\dots\dots\ \varphi_m$ are given as the switching thresholds, then as per the basis of proposed algorithm, at every given φ flux point, $G_M(\varphi)$ must have a stationary point. (Stationary points may be maxima, minima or saddle points). A small range of Conductance values, at these *m* stationary points and in the neighbourhood, can be considered as discrete resistance levels (as per the mathematical property of stationary points).

Now, for stationary points to occur, the given flux points $\varphi_1, \varphi_2\ \varphi_3 \dots\dots\dots\ \varphi_m$ must be the roots of following equation;

$$\frac{dG_M}{d\phi} = 0 \quad \dots (2)$$

From (1) and (2), we can write;

$$\begin{bmatrix} na_n\varphi^{n-1} + (n-1)a_n\varphi^{n-2} + \dots\dots\dots\dots \\ +3a_3\varphi^2 + 2a_2\varphi + a_1 \end{bmatrix} = 0 \quad \dots (3)$$

From (3), it can be easily understood that number of stationary points will be m=(n-1) present at φ_1, φ_2 $\varphi_3 \dots\dots\ \varphi_{n-1}$. Therefore, Conductance of nth order, can exhibit maximum (n-1) number of resistance levels. It has also been depicted through Fig. 1.

Finally, for the given parameters (switching thresholds) the values of unknown coefficients of Eq. (1) can be found through the following steps;

1. First, construct the Eq. (2 or 3) for given values of flux points, $\varphi_1, \varphi_2, \varphi_3 \dots\dots\ \varphi_{n-1}$, as follows;

$$\frac{dG_M}{d\phi} = \begin{bmatrix} \phi^{n-1} - (\phi_1 + \phi_2 + \phi_3 \dots\dots\dots \dots + \phi_{n-1})\phi^{n-2} \\ + (\phi_1\phi_2 + \dots\dots\phi_1\phi_{n-1} + \phi_2\phi_3 + \dots\dots) - (\phi_1\phi_2\phi_3 + \\ \dots\dots\phi_1\phi_{n-2}\phi_{n-1} + \phi_2\phi_3\phi_4 + \dots\dots) + \dots\dots\dots\dots \dots\dots\phi_2\phi_3\phi_4 \end{bmatrix} = 0 \quad \dots (4)$$

2. Find the coefficient values a_1, a_2, a_3....and a_{n-1} in terms of $\varphi_1, \varphi_2\ \varphi_3 \dots\dots$ and φ_{n-1}, after comparing Eq 4 with Eq 3.

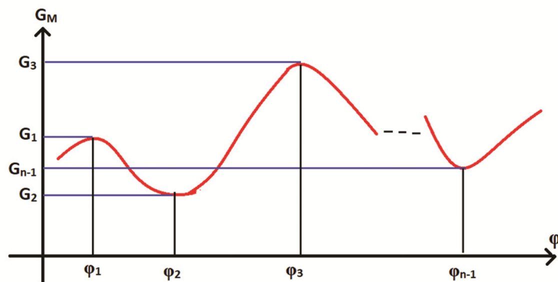

Fig. 1 — G_M versus φ response having multiple stationary points serving as distinct Conductance levels at given flux points

3. Put these coefficient values in (1) and find a_0 by assuming a Conductance value G_{Mm} for any switching threshold φ_m.

This way we can find the Eq 1, which exhibit the stationary points at the desired switching threshold values. The Eq 1 can be used to realize a corresponding memristor emulator to exhibit the PSM characteristics with stationary points at selected flux points.

However following points need to be addressed for the effective implementation of this method;

1.1.1 Conductance Margin G_{mar}

It is the difference between the two consecutive Conductance values i.e. $G_{mar} = |G(\varphi_m) - G(\varphi_{m-1})|$). It may change between every pair of the switching thresholds (two consecutive levels), but we are focusing upon the minimum value of G_{mmin}.

Now, it is always required that minimum values of the G_{mar} must be such that it should not be affected by the external noise, which may result in an undesired switching. But higher value of G_{mmin} creates another problem, which is, instability of the resistance levels. It can be understood from the following example. Below are the Conductance functions for different values of Conductance margin as; G_{mar}= 5 Mhos, 7 Mhos 10 Mhos and 12 Mhos, can be computed as given in Eq 5, 6 7 and 8, respectively;

$$G_{M3} = 5 + 11.25\phi - 7.5\phi^2 + 1.25\phi^3 \quad \dots (5)$$

$$G_{M3} = 5 + 15.75\phi - 10.5\phi^2 + 1.75\phi^3 \quad \dots (6)$$

$$G_{M3} = 5 + 15.75\phi - 15\phi^2 + 2.5\phi^3 \quad \dots (7)$$

$$G_{M3} = 5 - 27\phi - 18\phi^2 + 3\phi^3 \quad \dots (8)$$

These Conductance functions obtained for different values of Conductance margins given in Eqs (5)-(8) have been plotted in Fig. 2, which verifies the presence of two stationary points at given flux points. From these plots, it can be noticed that reduction in the value of G_{Mar} can result in more stable (corresponding to less variation) resistance states over wide ranges of flux values. Therefore, a trade-off can be observed between Conductance margin and constancy of Conductance levels. Now, for proper selection of switching thresholds and resistance margin, this type of response can be very useful in binary memories, logic design and other digital applications.

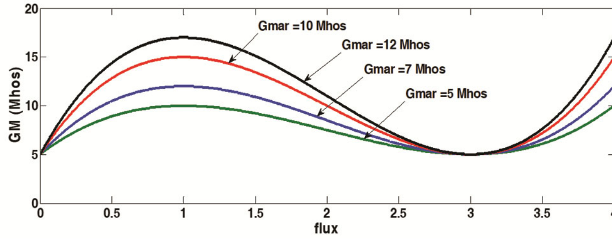

Fig. 2 — MATLAB generated responses for Eq. 5-8 plotted for different values of G_{Mar}

The discussion highlights the need for following considerations, while realizing a third-order memductance simulator.

Switching Thresholds: In implementing multi-level memristors, the switching thresholds should be chosen carefully so that the conductance margin (G_{mar}) maintains an optimal value that does not impair the performance of memristive resistance-switching applications.

Non-negative Conductance: It must be ensured that the realized conductance remains non-negative; otherwise, negative values may introduce undesirable effects in the application circuit.

Circuit-based Emulation: Emulating multi-level memristors in hardware is a major challenge, as they rely on highly nonlinear conductance functions. The above method primarily requires selecting appropriate conductance coefficients to meet the predetermined switching thresholds.

2 Transient *V-I* Behaviour Of Multi-Level Memristor For Sinusoidal Excitation

It is clear that the corresponding v-i (voltage-current) behavior of a multi-level memristor cannot be the same as a conventional monotonic memristor function**.** This is because the direction of the v-i contour rotation depends on the increases and decreases of the memristor state within the operating region.

Consequently, the *v-i* loop of monotonic functions always encloses of single lobe in a quadrant, representing the resistance change in only one direction. But, in case of a multi-level memristor, this behaviour will depend upon both input sinusoidal voltage and Conductance response i.e. number of stationary points lying in operating region. It has been explained below through Fig. 3.

In Fig. 3(a), a dual-level Conductance response has been depicted, having two stationary points φ_1 and φ_2. If a sinusoidal voltage $v(t)=V_m sin\omega t$ is applied across this memristor then the operating region on the G_M- φ curve is decided by the supplied flux during a half-cycle, φ_S, which is given by;

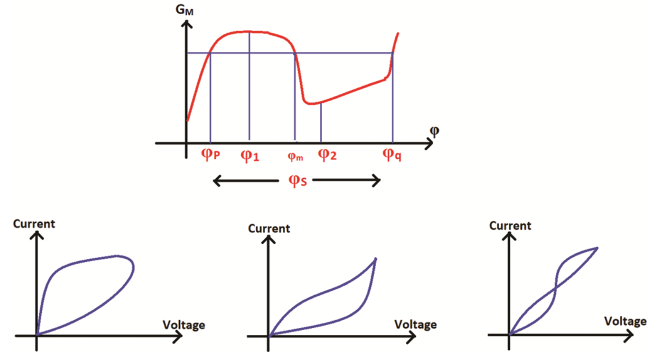

Fig. 3 — Different type of transient *v-i* behaviours for different conditions of operating region covered by φ_S (a) G_M- φ response having two stationary points (b) VI plot when φ_S covers only single stationary point (c) When both points are covered, and (d) When two symmetrical points are covered by φ_S

$$\phi_S = \int_0^{T/2} V_m Sin\omega t dt = \frac{2V_m}{\omega} \quad \ldots (9)$$

(It must be noted that that φ_S is always added to the initial flux state, which plays a major role in deciding the operating region)

In Fig. 3(b), the transient *v-i* loop is shown, which is generated when φ_S covers only single stationary point on the G_M- φ curve. This behaviour is observed as similar to conventional one due to monotonic variation of Conductance in this region. The effect of the stationary points on the transient behaviour is observed, when both points lie in the operating region. In this case *v-i* loop is formed with an irregular shape due to change in the direction of Conductance variation as shown in Fig. 3(c)

Furthermore, in a particular condition, the second case shown in Fig. 3(c) can also exhibit an extra pinch-off point besides the cross-over found at origin as shown in Fig. 3(d). It happens when operating region on the G_M-φ curve finds two symmetrical points, φ_p and φ_q, lying outside the region consisting of φ_1 and φ_2. These two points φ_p and φ_q lie at equal distances from point φ_m, where φ_m is the flux transferred during the quarter cycle of sinusoidal input voltage. And at these two symmetrical points, same value of Conductance is exhibited as shown in Fig. 3(a).

i.e.,

$$G_M(\phi_P) = G_M(\phi_m + \phi_P) \quad \ldots (10)$$

where,

$$\varphi_m = \frac{V_m}{\omega} \quad \ldots (11)$$

Now, on applying mathematics and the condition given in Eq. 10, the parametric condition for occurrence of symmetrical pinch-off points is found as;

$$\frac{a_1\omega^2 + 2a_2\omega V_m + 4a_3V_m^2}{a_3V_m^2} < V_m^2 \quad \ldots (12)$$

It can be also verified for the G_M- φ response evaluated in Eq 5 (plotted in Fig. 2) for selecting suitable value of applied sinusoidal voltage (satisfying the condition given in Eq 12). The corresponding MATLAB generated *v-i* plot has been shown in Fig. 4.

3 Memristor Emulator to Realize the Three Pinch-Off Characteristics

The Memristor emulator to realize the Conductance function given in Eq. 1 is shown in Fig. 5. The presented circuit is based on four OTAs and three grounded passive elements. Previously some other multi-pinch-off memristor emulators have also been designed but using only fractional order models[8-12].

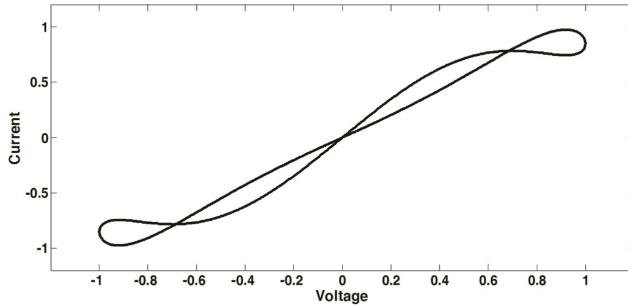

Fig. 4 — PHL (Pinched Hysteresis Loop) having two non-zero symmetrical pinch-off points for the Conductance represented by Eq. 5.

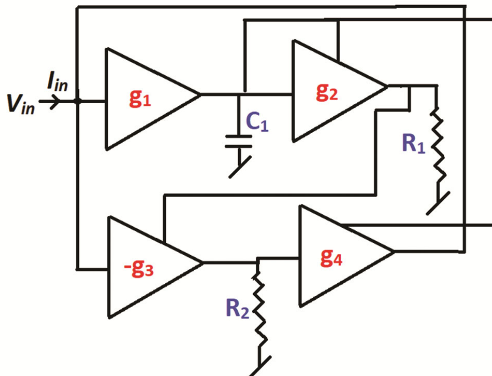

Fig. 5 — Designed emulation configuration of Three-cross-over memristor using OTA

On applying the KVL-KCL analysis, the Input current I_{in} of the above circuit can be calculated as,

$$I_{in} = k_3k_4\left(\frac{g_{m1}\phi_{in}}{C_1} + (-V_{SS} - V_{th})\right)\begin{pmatrix} k_2R_1\left(\frac{g_{m1}\phi_{in}}{C_1}\right)^2 \\ + k_2(-V_{SS} - V_{th})\left(\frac{g_{m1}\phi_{in}}{C_1}\right)R_1 + (-V_{SS} - V_{th}) \end{pmatrix} V_{in}R_2 \quad \ldots (13)$$

where g_{m1}, g_{m2}, g_{m3} and g_{m4} are transconductance ratios of the employed OTAs respectively and k is the transconductance parameter with V_{SS} and V_{th} are supply voltage and threshold voltage respectively.

On Expanding Eq. 13, the Conductance G_{M3} of the realized three-pinch off memristor can be found as,

$$G_{M3} = \frac{I_{in}}{V_{in}} = k_2k_3k_4R_1R_2\left[\frac{g_{m1}\phi_{in}}{C_1}\right]^3 + 2k_2k_3k_4R_1R_2(-V_{SS} - V_{th})\left[\frac{g_{m1}\phi_{in}}{C_1}\right]^2 +$$
$$(k_3k_4R_2(-V_{SS} - V_{th}) + k_2k_4k_3R_1R_2(-V_{SS} - V_{th})^2)\left[\frac{g_{m1}\phi_{in}}{C_1}\right] + k_3k_4R_2(-V_{SS} - V_{th})^2 \quad \ldots (14)$$

Now, to verify the three pinch-off characteristics of this circuit, we have used the PSPICE simulation software at 0.18µm CMOS technology. The standard OTA CMOS implementation given in [13] has been employed. For the simulation purpose, the passive component values are selected as; C_1=.54nf, R_1=45k and R_2=10k with power supply as $V_{SS,DD}$=±0.9V. Also, the sinusoidal signal with peak value V_P=0.64V is applied at the input. In Fig. 6 and 7 the transient *v-i* contours for two different operating frequencies have been plotted, which consists of three pinch-off points.

4 Application of the Proposed Memristor Emulator in Modelling Amoeba's Behaviour

A neuromorphic circuit using a has memristor been reported in[14]. This circuit is essentially an RLC network but with the incorporation of a memory element instead of a passive component. It was designed to validate the synaptic nature of the memristor in modelling the behaviour of an Amoeba. The Amoeba adapts its locomotive speed in response to changes in environmental temperature. Initially, the Amoeba reduces its movement after repeated temperature drops. However, after some time, it quickly adjusts its speed even after a single

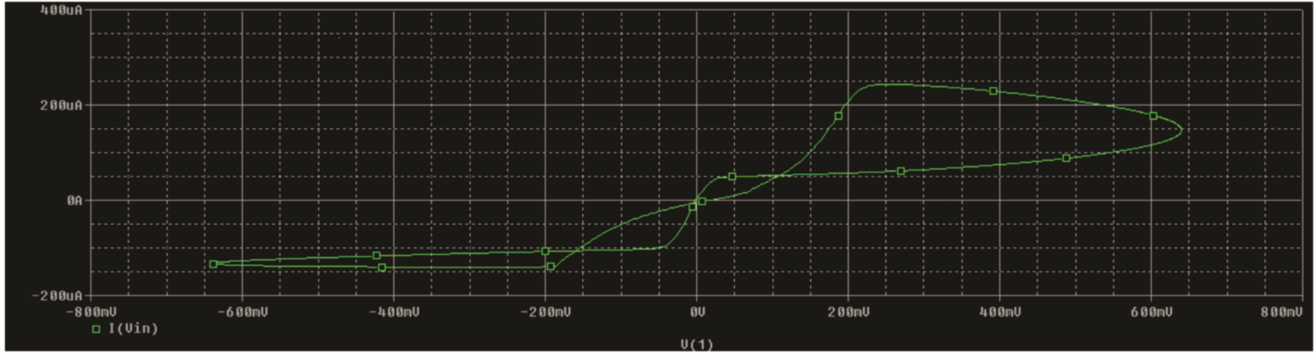

Fig. 6 — Three Pinch-off point *v-i* contour generated by the emulator given in Fig. 5 at 800 kHz

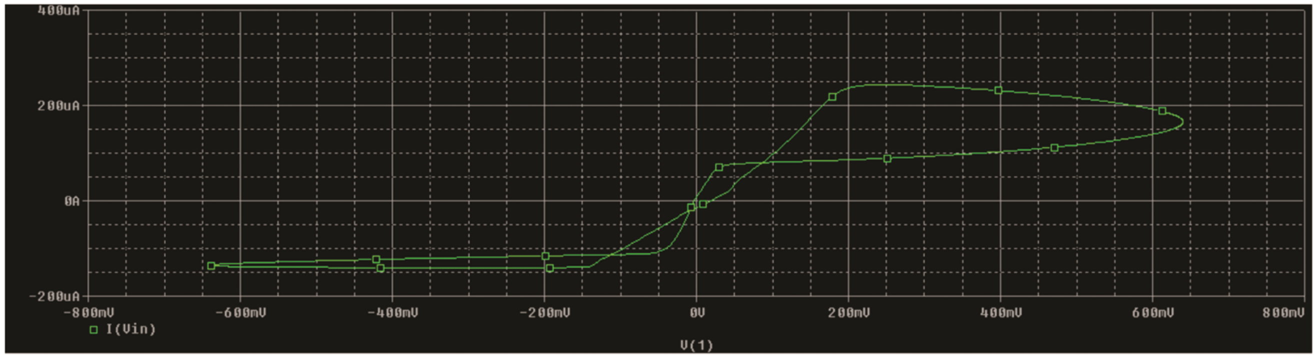

Fig. 7 — Three Pinch-off point *v-i* contour generated by the emulator given in Fig. 5 at 1 MHz

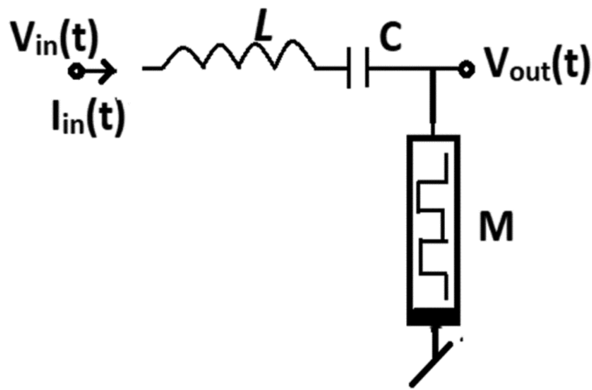

Fig. 8 — Proposed memristor M realised by the proposed multi-level model used in amoeba-learning's modelling with passive elements selected as R_1 = 2 kΩ, C_1 = 0.1 nf, R_2 =1 kΩ and C = 0.04 nF, R=10kΩ

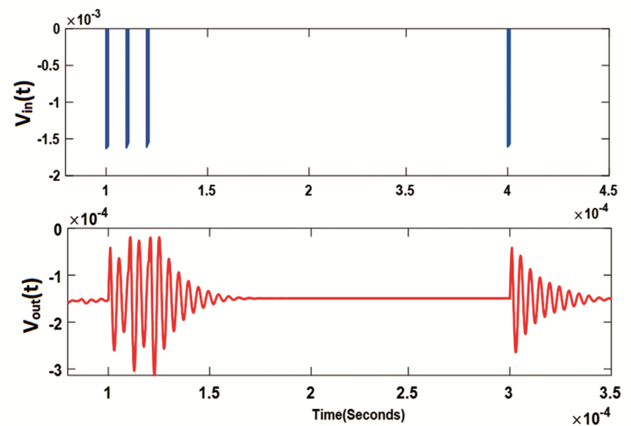

Fig. 9 — Output voltage V_{OUT} demonstrating gradual drop with the occurrence of input pulses (V_M parameters with peak value as V_m = 0.3 mV and pulse width as T_W = 0.01 μs)

temperature drop, demonstrating how it learns from past experiences. The circuit is illustrated in Fig. 8. In Fig. 8, the developed circuit, the input $V_M(t)$ represents temperature variations in the surrounding environment, while $V_{OUT}(t)$ reflects the changes in the Amoeba's locomotive speed. The simulation results for $V_{OUT}(t)$ are shown in the lower plot of Fig. 9, with the input voltage $V_{in}(t)$ applied as a pulse signal (illustrated in the upper plot of Fig. 9). The output shows that during multiple pulse events, the oscillations gradually decrease. However, the output slows down immediately when a single pulse occurs after a delay. This behaviour confirms that the circuit accurately models the Amoeba's response. The Amoeba anticipates further temperature drops based on past occurrences, which leads to a faster reduction in movement, a behaviour mirrored in the circuit's output.

Table 1 — Comparison of previously reported multi-level memristor emulators with the proposed one

Ref.	No. of Active Elements	Order of Realizing Expression	No. of Capacitors(F/G*)	No. of Resistors (F/G)	No. of Crossing points
[8]	2 CCII, 1 AD633	II (Fractional)	12G	1F/8G	2
[9]	1 AD844, 1 AD633	II(Fractional)	1G	4F/3G	2
[10]	2 CCII, 3 AD633	III (Fractional)	1G	5F/9G	3
[11]	3 CCIIs, 2 Adders, 1 devider and multiplier, 1 AD633	III (Fractional)	Undefined (Large number of passive elements due to fractional capacitors)		3
[12]	2 CCII& Blocks of adder, differentiator and multiplier, 1 AD633	III(Fractional)	Undefined (Large number of passive elements due to fractional capacitors)		3
Proposed	4OTAs,	III	1G	2G	3

*F=Floating, G=Grounded

5 Conclusion

The method presented in this paper can be considered a novel approach to the systematic emulation of memristor functions with a desired response. Using the presented method, we can design multivalued memristors based on predefined switching thresholds on the flux axis. With the help of these flux points, the critical values of pulse excitation voltages can be determined to switch the memristor between different resistance states. Finally, the computed conductance expression can be realized through corresponding circuit emulators, which are applicable to memristive applications. It is also shown that by choosing appropriate values of resistance margin we can achieve less-sensitive behavior by reducing variation in resistance states.

Moreover, we have discussed the effect of multiple peaks (resistance states) in the conductance response on the transient v-i behavior for sinusoidal inputs. When compared with previously reported memristors based on higher-order conductance expressions, the proposed design offers several design-related advantages in terms of size and component usage, as shown in Table 1.

The response is a three-pinch-off v-i characteristic, whose generation is also demonstrated through an OTA-based emulator. The operation of the proposed memristor emulator was also validate**d** using a neuromorphic application circuit modeling Amoeba behavior.

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