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Reversed C-shape Pocket Double Gate TFET with dual-κ Spacers

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The study delves into the evaluation of the Double Gate Tunnel Field-effect Transistors (DGTFET) structures, Reversed C-shape Pocket TFET (RCSP-TFET), and RCSP-TFET with dual-k spacers. The TFET supports current generation through band-to-band tunneling among source/drain and channel regions. By strategically placing the three n+ pockets nearby the source-channel region, the tunneling barrier width is lowered and the current is increased in the ON-state. Subsequent to the calibration of the DGTFET utilizingdiverse tunneling models, a comprehensive evaluation of the performanceof the RCSP-TFET is undertaken. This assessment is executed through the meticulous optimization of the thickness and length of the n+ pocket, thereby ensuring precise and dependable outcomes.Furthermore, the spacer walls comprised of an amalgamation of high-k and low-k dielectrics is intended to augment the performance of the device. This approach seeks to optimize efficacy and improve operational capabilities. The optimized structure reveals a higherON-state current (I_{ON})= 7.0 x 10^{-5} (A/μm), the ON-OFF current ratio (I_{ON}/I_{OFF}) 1.12×10^{11}, Ambipolar Current (I_{Amb})= 2.1x 10^{-13} (A/μm), reduced subthreshold swing (SS)=11.09 mV/decade) in the RCSP-TFET structure with dual-k spacers. The resultsimply the potential feasibility of the RCSP-TFET with dual-k spacers as a compelling choice for next-generation semiconductor technology.

Keywords: Band-to-band tunneling (BTBT), DGTFET, RCSP-TFET, Dual-k spacer, Subthreshold swing (SS)

1 Introduction

In the contemporary era, an increasing number of individuals and businesses are leveraging electronic devices for communication and various functionalities. The growing popularity of these devices can be attributed to their cost-effectiveness and user-friendly attributes. Furthermore, the continuous transistor-level CMOS scaling is consistently leading to a reduction in the size of these devices. Numerous challenges are associated with downsizing conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Some of these characteristics include a smaller ON/OFF current ratio, a larger OFF current, more power dissipation, and shorter channel effects accompanied by a larger subthreshold swing[1-4]. For metal-oxide field-effect transistors (MOSFETs), the limitations imposed by Boltzmann statistics make it very difficult to achieve a subthreshold swing (SS) below 60 mV/decade at 300 K.Tunneling field-effect transistors (TFETs), a practical and effective substitute, have been created to overcome these intrinsic constraints[5]. A gated p-i-n diode makes up a TFET, which functions via gate-controlled band-to-band tunneling (BTBT)[6]. The operational principle of a TFET is fundamentally based on quantum BTBT of charge carriers[7-8]. TFETs often displays lesser ON current compared to MOSFETs due to its reverse biased design[9-10]. However, TFET's ambipolar conduction poses a disadvantage, potentially causing power loss when the transistor is switched off[11-13]. Unfortunately, the utilization of TFETs for higher-frequency applications is constrained due to their inadequate current driving capabilities[14]. Several strategies have been explored to address this challenge and enhance the on-current while reducing the subthreshold swing (SS). These approaches encompass the utilization of narrow band gap materials[15,16], extension of source doping[6], gate engineering[17,18], work function engineering[19], and implementation of pocket-doped layers[20-21]. Nonetheless, the development of additional innovative methods remains imperative to enhance ON-state current and mitigate smaller subthres hold swingfor a reduced channel length.The adoption of the source-pocket tunneling field-effect transistor structure is indeed a promising strategy aimed ataugmenting the ON-state current in silicon-based TFETs. This approach leveragesadvantages aimed at localized doping to create an optimal band alignment, which facilitates improved tunneling probability at the source-channel junction[22]. This architectural design incorporates a heavily doped pocket (n-type)within the

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source region to further increase the device performance in comparison to conventional TFET designs. Numerous materials and structures for the pocket in TFETs have been rigorously examined, encompassing the implementation of a vertical pocket strategically placed across the source and the channel[23-24] to advance the tunneling current.

Achieving effective tunneling barrier modulation and maintaining a low SS while optimizing other parameters is difficult. High doping levels, required for enhanced tunneling, can lead to increased junction capacitance and reduced mobility. Additionally, TFETs often rely on advanced materials, such as strained silicon or III-V compounds, which pose fabrication and integration challenges. Not with standing these advancements, there remains a critical need for further refinement of silicon-based TFETs to attain optimal I_{ON} and SS with metrics at diminished channel lengths, particularly for applications necessitating ultra-low power design.

The proposed silicon-based ReverseC-shaped pocket TFET (RCSP-TFET) with dual-k spacers is a double-gate pnpn-TFET comprisingthree pockets i.e. two horizontal pockets, and one vertical pocket. Its purpose is to enhanceON-state current and subthreshold swing with reduced ambi-polarity with lower channel length. A comprehensive analysis of the physical dimensions of the structure and variation in gate work functionis carried out.

2 Device Architecture and Simulation Methodology

Figure 1 illustrates three variations of silicon-based double gate TFET (DG-TFET). In Fig. 1(a), the conventional DG-TFET with multi-layer gate oxide is presented, while Fig. 1(b) showcases the Reversed C-shape Pocket DG-TEFT with stacked gate dielectric, denoted as RCSP-TFET and Fig. 1(c) shows the RCSP-TFET with spacers. In the latter configuration, a reversed C-shape is established between the source and channel regions, achieved through utilization of three heavily n-type doped pockets, namely pocket 1, pocket 2, and pocket 3 oxide comprises of high-k and low-k spacers. The structures exhibit a uniform doping profile, characterized by a constant doping concentration of the source (p-type), intrinsic channel, and drain (n-type)are$1 \times 10^{20} cm^{-3}, 1 \times 10^{17} cm^{-3} and\ 5 \times 10^{18} cm^{-3}$, respectively. To reduce the ambi-polarity in TFETs, the doping concentration of the source has been intentionally engineered to exceed that of the drain.Doping concentration of all pockets are taken $1 \times 10^{20} cm^{-3}$ (n-type)[21]. Throughout the scope of this study, the EOT is taken as 1 nm, while the thickness of

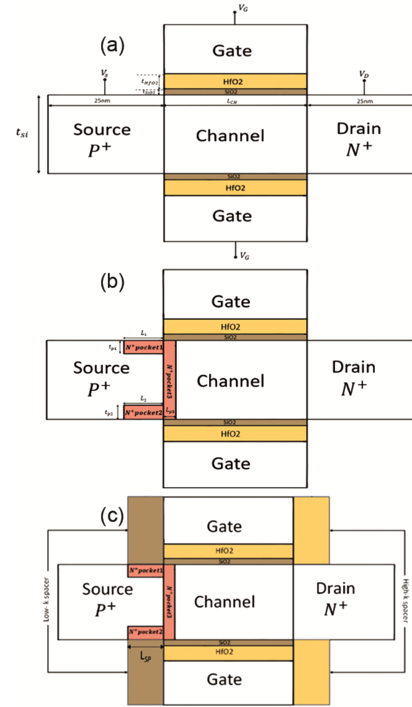

Fig. 1 — Schematics of (a) Double Gate TFET with Multi-layer gate Dielectric (DGTFET), (b) Reversed C-shape Pocket DGTFET (RCSP-TFET), and (c) RCSP-TFET with dual-k spacer

HfO_2 is taken as 2nm. The channel length (L_{Ch}) serves as a variable for DGTFET in the simulation parameter.

Subsequently, in the simulation for RCSP-TFET, the channel length is standardized at 25nm. The Silicon thickness (t_{Si}) is 10 nm.The length of pocket 1 (L_{p1}) and pocket 2 (L_{p2}) is 7nm, with the thicknesses of pocket 1 (t_{p1}) and pocket 2 (t_{p2}) being subject to variation within the range of 2nm to 2.5nm. The length of pocket 3 (L_{p3}) is also modulated as a variable, encompassing values from 1nm to 2nm. Figure1(c) demonstrates the use of HfO_2 and SiO_2as dual-κ spacers with respective dielectric constantvalues of 23 and 3.9. The initial length of the spacer wall (L_s) is set at 7 nm, aligned parallel to the lengths of pocket 1 and pocket 2. Subsequently, the optimization of the spacer length implicates a variation of L_{sp} within the range of 7 nm to 10 nm.

The proposed RCSP-TFET with a dual-k spacer structure presents a challenge in terms of requiring aggressive process capabilities. To comprehensively address this challenge, it is advisable to formulate a conceptual process flow for the proposed device, informed by the findings delineated in reports[7,21-23,31], for the effective realization of the pockets. The procedure encompasses the vertical growth of distinct doped layers via epitaxy, succeeded by selective etching at both

extremities to facilitate the formation of pocket windows and subsequent deposition of a thin pocket film using the chemical vapor deposition (CVD) technique. The spacers are formed by selective deposition on both sides of the source and drain. For the gate formation selective etching and metallization processes are carried out to serve the fabrication of the proposed RCSP-TFET structure.However, the process steps involved are complex. The research presented[21] has successfully demonstrated the growth of thin silicon pockets within a line Tunnel Field-Effect Transistor (TFET) structure. Furthermore, the creation of narrow silicon films has been realized through the selective epitaxial growth process, as detailed in[22,] as well as by employing electron cyclotron resonance plasma chemical vapor deposition (CVD). The proposed structure holds significant promise for future fabrication.

For the simulation process, Synopsys Sentaurus TCAD tool is utilized[24]. It incorporates a nonlocal BTBT model, that facilitates the examination of differences in electric field distributions and tunneling generation rates along the device's tunneling length. The nonlocal method takes into consideration the density of states and occupancy levels. High doping concentration, and reverse bias tunneling junctions are well-suited for this design. Considering the substantial doping of the source and drain regions, the bandgap narrowing model, in conjunction with the Fermi–Dirac model, is utilized for comprehensive analysis. A variety of models are employed to optimize performance, including the Shockley–Read–Hall (SRH) recombination model, the drift-diffusion carrier model, as well as the Auger and doping-dependent models. Moreover, quantum tunneling mechanisms are meticulously considered at the source/Drain-channel junctions to further enhance operational efficacy.To meticulously establish the specific parameters pertinent to the BTBT model, reference[21] was duly consulted. The nonlocal BTBT model employed within the framework of this research has been calibrated in alignment with the scholarly contributions of Boucart and Ionescu[25]. Figure 2 illustrates the calibration of transfer characteristics. Using modelling and calibration techniques, the Synopsys TCAD tools allow for effective model analysis and simulation.

3 Results and Discussion

This segment discusses several key parameters that can improve the device performance, including channel length (L_{Ch}), pocket thickness(t_P), and spacer length(L_S). The ON-state current (I_{ON}), OFF-state current (I_{OFF}), ambipolar current (I_{AMB}), and subthreshold swing (SS) are noteworthy measures of DC performance.

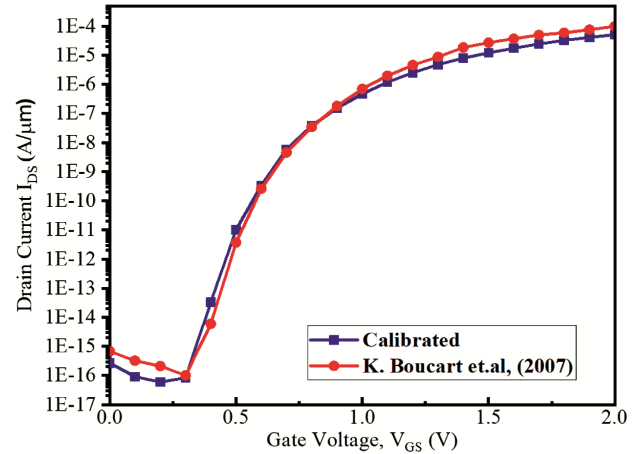

Fig. 2 — The I_{DS} vs V_{GS}were calibrated using the TCAD models[24]

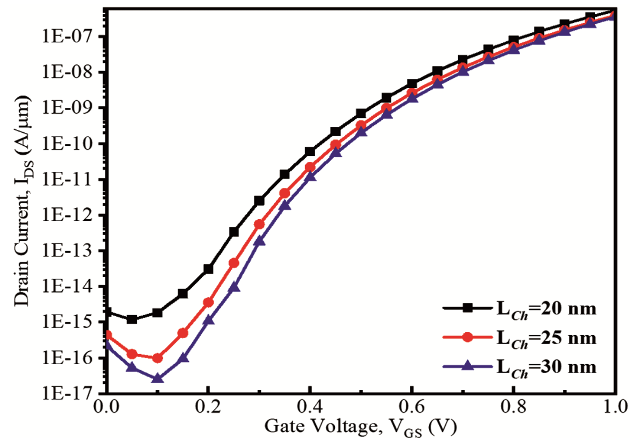

Fig. 3 — Transfer characteristics of DG-TFET when channel length (L_{Ch}) is varied from 20nm to 30nm

3.1 Effect of Varying the Channel Length (L_{Ch})of Device

Figure 3 shows how changes in the channel length affect the transfer characteristics. For DGTFETs, the channel length (L_{Ch}) is adjusted between 20 and 30 nm. While the gate voltage is swept from 0V to 1V for the analysis, the drain voltage is assumed to be 1V. Analysis of data reveals minimal variation in the ON state current.

A low subthreshold swing (SS) is observed for channel lengths of 20 and 25 nm. A higher I_{ON} is observed for L_{Ch}= 20 nm while forL_{Ch} = 25 nm and 30 nm comprise lower (I_{OFF}).The phenomenon occurs because a shorter channel length results in a narrower tunneling barrier. This is attributed to the higher electric field present at the source-channel junction,

which consequently leads to an increase in leakage current[31].It is important to note that the ON-OFF current ratio is significantly higher when the channel length (L_{Ch}) is set to 25 nm. Furthermore, a reduced SS of 54.15 mV/dec is observed for L_{Ch}= 25 nm. Consequently, in the continued analysis of the RCSP-TFET structure, a channel length of 25 nm is being considered.

3.2 Impact of Pockets between Source and Channel

It examines the effects of applying the pockets amid the source and the channel region.The transfer characteristics of the RCSP-TFET provide valuable insights, emphasizing a comparison between the structure without any pocket and the implementations of horizontal and vertical pockets. This analysis is illustrated in Fig. 4. The structure with no pockets shows a higher leakage current compared to the structure with pockets.To begin with, two horizontal pockets are incorporated (L_{P1} and L_{P2}), followed by the single vertical pocket(L_{P3}) into the previously established no-pocket design. Introducing pockets providesa large tunneling area leading to higher tunneling efficiency and hence high I_{ON}. Figure 4 reveals that a lower ON state current is observed either by implementing horizontal pockets or a vertical pocket only. However, a combination of all three pockets gives improvement in the I_{ON},I_{OFF} and a low subthreshold swing. At first, the thickness and length of the pockets are considered as mentioned in Section II. Pockets 1 and 2 established a vertical tunneling path, while Pocket 3 facilitated lateral tunneling between the source-channel regions. Proposed configuration effectively reduces the width of the tunneling barrier, ultimately resulting in enhanced functioning of the Tunnel Field Effect Transistor (TFET).

3.3 Impact of Variationt_{p1}, t_{p2} and L_{p3} on RCSP-TFET

This section addresses the optimizations of the thickness and length of pocketsintheproposedstructure. The thickness of pocket 1 (t_{p1}),and pocket 2 (t_{p2}) is varied from 2nm to 2.5nm while the length of the pockets (L_{p1} and L_{p2}) is fixed at 7 nm. The length of pocket 3(L_{p3}) is varied from 1nm to 2nm with fixed thickness (t_{p3}) of 10 nm. For RCSP-TFET, a higherON-state current (I_{ON}) is observed, considering t_{p1}, t_{p2}= 2nm and , L_{p3}= 2nm.However, with such dimensions, the deteriorated performance of the device has been seen. The optimized dimensions aret_{p1}, t_{p2}=2nm and L_{P3}=1nm, which provides enhanced device performance. Figure 5 shows the transfer characteristics

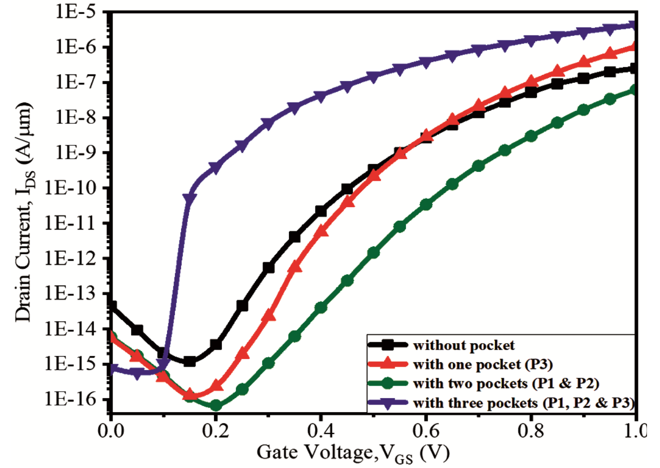

Fig. 4 — Transfer characteristics of RCSP-TFET by applying different pockets

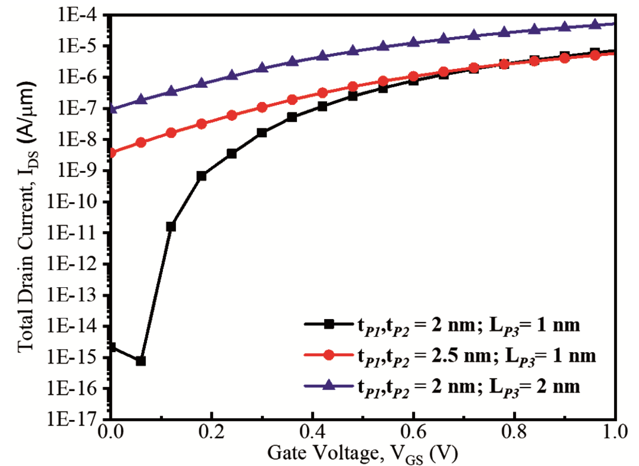

Fig. 5 — Transfer characteristics of RCSP-TFET with varying thickness of pocket 1 (t_{p1}),pocket (t_{p2}) and length of pocket 3 (L_{p3})

with varying thickness and length of the pockets. For further simulation the t_{p1}, t_{p2}= 2 nm, andL_{p3} = 1 nm are considered for RCSP-TFET.

3.4 EffectofVaryingthe Work-Function of Gate

The significance of altering the work-function of gate on the transfer characteristic is effectively demonstrated in Fig. 6. An increase in the work function reduces band bending between the source and channel regions. As a result, a device with a 4.5 eV work function requires a higher gate voltage (0.2V) to initiate tunneling current compared to lower work function devices. However, the 4.5 eV work function device exhibits slightly higher leakage current across the source-channel junctions compared to other devices with lower work function.The device with a 4.2 eV work function is selected for further analysis,

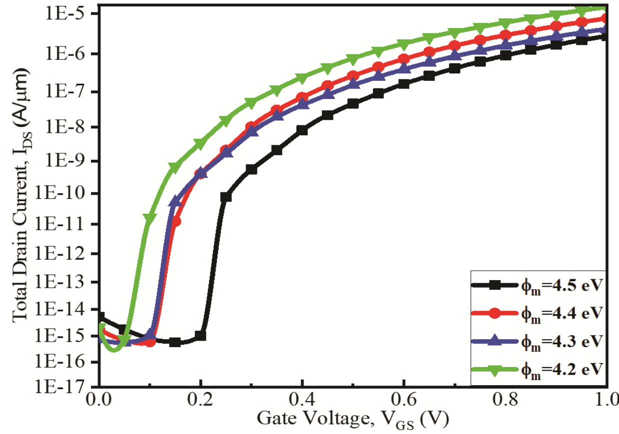

Fig. 6 — Transfer characteristics of RCSP-TFET with varyinggate work functions at V_{GS}=V_{DS}=1V

as it enhances the on-off current ratio while maintaining a moderately good subthreshold swing. To minimize leakage, the work function can only be adjusted within a limited range. To further improve the subthreshold swing (SS) and I_{ON}, dual-κ spacer walls are implemented.

3.5 Effect of Applying Dual-k Spacer Walls

The analysis of spacer engineering is carried out in this section. A low-k spacer is represented by SiO_2 and a high-k spacer by HfO_2 as shown in Fig. 1. Initially, individual analysis of SiO_2 and $HfO_2$is carried out[26,33]. The observation indicates a higher order of ON-state current as well as reduced subthreshold swing (SS) associated alongside the HfO_2 spacer wall. Upon implementing the dual-k spacers, a low SS and an increase in the figure of merit is observed.Furthermore, the RCSP-TFET with HfO_2 on the right and SiO_2 on the left demonstrated a low SS (~11 mV/decade) in comparison to the RCSP-TFET with SiO_2 on the right side and HfO_2 on the left side as shown in Fig.7. Consequently, the optimized structure is indicated by the RCSP-TFET with HfO_2 on the right side and SiO_2 on the left side.

3.6 Effect of Varying Spacer Length (L_s) on the Device Performance

The length of spacer (L_s) is varied from 7 nm (i.e. aligned with the length of pocket 1 (L_{p1})and pocket 2 (L_{p2})) to 10nm as indicated in Fig.1(c). It is perceived that on increasing the length of spacer(L_s) beyond 7nm, the I_{ON} and SSdeteriorates as shown in Fig. 8. Hence 7 nm is considered an optimized spacer Length (L_s).

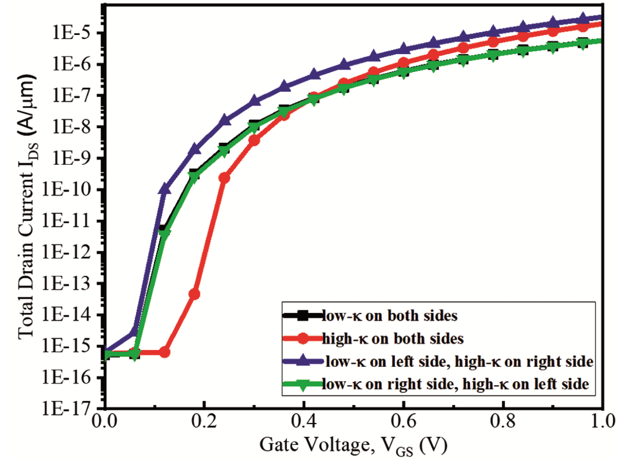

Fig. 7 — Transfer characteristics of RCSP-TFET with spacers

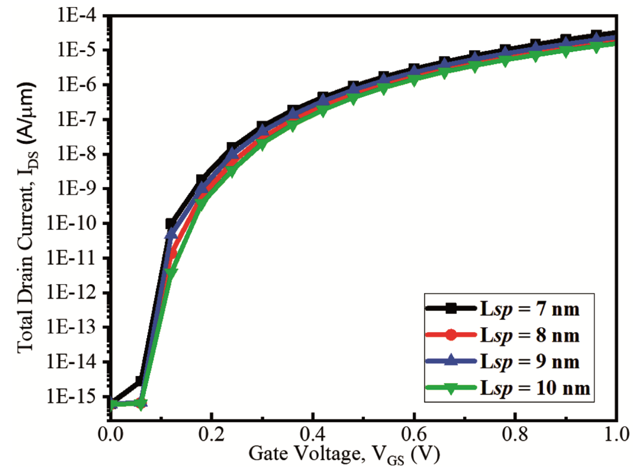

Fig. 8 — Transfer characteristics ofRCSP-TFET spacer length (L_{SP}) variations

3.7 Impact of Sidewall Spacers on Band-to-Band Generation

In Fig. 9, the effect of employing high-k and low-k spacers on the carrier generation rate ($cm^{-3}s^{-1}$) is demonstrated. The study reveals that the optimized RCSP-TFET structure, featuring HfO_2 on the right and SiO_2 on the left, shows the most prevalent carrier generation rate proximate to these semi conductor surfaces in comparison to alternative structures. This arrangement generates an elevated electric field nearby source-channel intersection as exhibited in Fig. 10, yielding a notable ON current.

3.8 Optimized Results of Proposed Device

Figure 11 compares the I_{DS}-V_{GS} of DGTFET, RCSP-TFET, and the RCSP-TFET including dual-k spacers. It is observed that the optimized structure of RCSP-TFET with dual-k spacers has low I_{Amb} current and very low SS as compared to the DGTFET and RCSP-TFET. The energy band diagram presented in

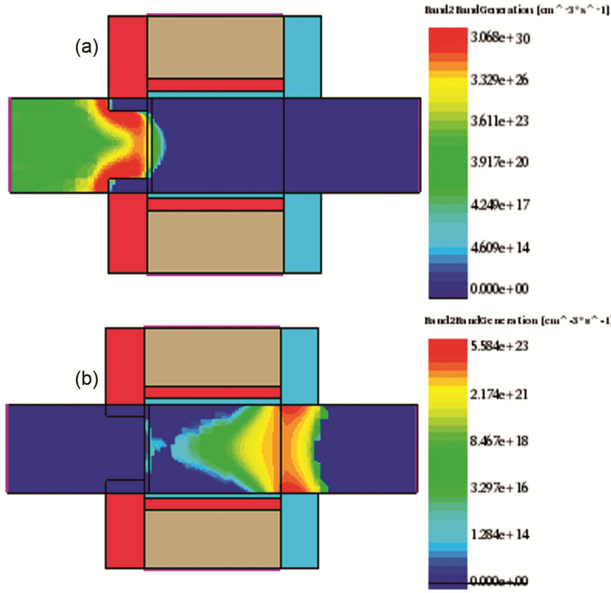

Fig. 9 — Carrier generation rates (a) ON-state (V_{GS}=V_{DS}=1V), and (b) Ambipolar state (V_{DS}=1V, V_{GS}=-1 V)

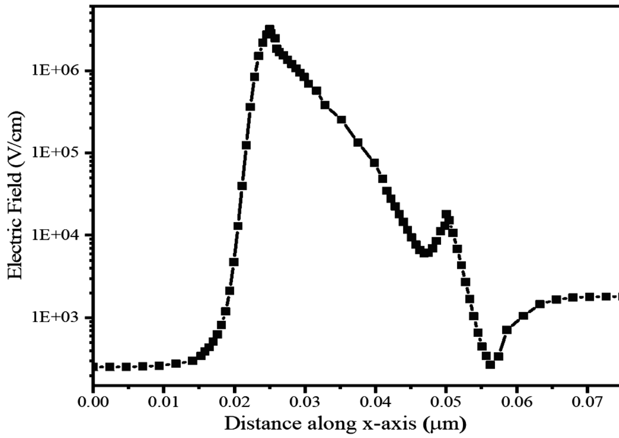

Fig. 10 — Electric Field in the proposed device's ON state (V_{DS}=V_{GS}=1V) along the cut line 5 nm below the oxide layer

Fig. 12 provides a detailed representation of the behavior of the proposed device in both the ON state and the ambi-polar state. The tunneling barrier width at the source-channel junction reduces when applying V_{GS} = +1V (ON-state). The observed phenomenon is attributed to the reverse C pockets, which effectively enhance the electric field due to the higher charge density as shown in Fig. 9. This significantly increases the band-to-BTBT between the source–channel regions, resulting in an improved I_{ON} for the device. Notably, the pocket region features doping opposite to the source region. This further contributes to enhancing the electric field and optimizing device performance. Consequently, this mechanism leads to an increased BTBT generation rate between the

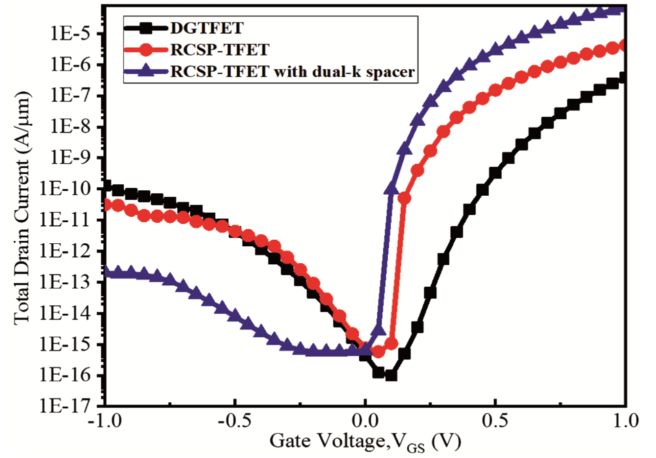

Fig. 11 — I_{DS}-V_{GS}curve of DGTFET, RCSP-TFET and RCSP-TFETwith dual-k spacers

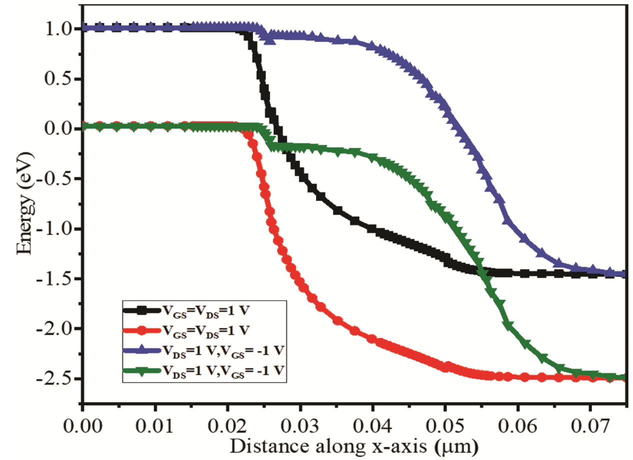

Fig. 12 — Energy Band diagram of the proposed device in ON state and Ambipolar state at 5 nm below the oxide layer

Table 1 — Tunneling barrier width when V_{GS} is ±1V is applied for the three devices

	Tunneling Barrier Widths		
Structure	DGTFET	RCSP-TFET	Proposed Structure
ON-state	4.6nm	4.2nm	3.7nm
Amb-state	5.3nm	5.5nm	6.1nm

source and channel regions. Table 1compares the tunneling barrier widths of DGTFET and proposed device. Additionally, the dual-k spacershelp to raise the electric field intensity near the tunneling junction[31], which improves subthreshold swing (SS) and increases current of device.The comparative results of all three structures are shown in Table 2.

Table 3 recapitulates the comparison of RCSP-TFET with dual-k spacer with the different TFET structures mentioned in the literature. The proposed structure provides better results compared to other structure with channel length of 25 nm.

Table 2 — Comparison between the DGTFET (convention with dual gate dielectric), RCSP-TFET, RCSP-TFET with the dual-k spacer wall

Parameters	DGTFET	RCSP-TFET	RCSP-TFET with dual-k spacer
$I_{ON}(A/\mu m)$	1.33×10^{-7}	4.23×10^{-6}	7×10^{-5}
$I_{OFF}(A/\mu m)$	3.6×10^{-15}	7.65×10^{-16}	6.23×10^{-16}
I_{ON}/I_{OFF}	3.6×10^{7}	5.5×10^{9}	1.12×10^{11}
$I_{Amb}(A/\mu m)$	1.9×10^{-10}	3.12×10^{-11}	2.1×10^{-13}
$SS(\frac{mV}{Dec})$	55.3	13.51	11.09

Table 3 — Comparison of RCSP-TFET with the dual-k spacer with different structures mentioned in the literature

Parameters	$I_{ON}(A/\mu m)$	$I_{OFF}(A/\mu m)$	I_{ON}/I_{OFF}	$I_{Amb}(A/\mu m)$	SS (mV/dec.)
[27]	4.26×10^{-6}	4.87×10^{-17}	8.65×10^{10}	3.20×10^{-12}	41.9
[28]	0.3×10^{-6}	-	-	-	26
[7]	1.29×10^{-6}	2.56×10^{-18}	5.05×10^{11}	-	15.94
[29]	1.6×10^{-7}	10^{-15}	10^{8}	-	12
[30]	$1.04\text{ x }10^{-3}$	$2.7\text{ x }10^{-13}$	$3.8\text{ x }10^{9}$	$7.4\text{ x }10^{-14}$	32
Proposed TFET	7×10^{-5}	6.23×10^{-16}	1.12×10^{11}	2.1×10^{-13}	11.09

4 Conclusion

Areverse C-shape pocket DGTEFT with multi-layer gate dielectric (RCSP-TFET)with dual-k spacer walls is examined and analysed with channel length taken as 25 nm. Three pockets are positioned thoughtfully throughout the source and channel region to improve the device's performance as compared to conventional TFETs. Although, the spacer walls are used to reduce ambipolarity and OFF current.The study included the optimizing the various parameters of the device such as L_{Ch}, t_P, $L_{P.}$ ϕ_m, $L_S$and spacer selection. It is stated and examined how changing these variables affects the device performance metrics, including I_{ON}, I_{OFF}, SS_{avg}, I_{ON}/I_{OFF}. The results shows that optimum performance is when L_{Ch}= 25 nm, t_{P1}=t_{P2}=2 nm,t_{P3}= 10 nm, L_{P1}=L_{P2}= 7 nm, L_{P3}= 1 nm, ϕ_m=4.2 eV and L_{sp}= 7 nm.The optimized value ofI_{ON},I_{OFF} and I_{ON}/I_{OFF} is found to be $7\times 10^{-5}(A/\mu m)$ and $6.23\times 10^{-16}(A/\mu m)$ and 1.12×10^{11}, and subthreshold swing (SS) is reduced to 11.09(mV/decade) for optimized RCSP-TFET with dual-k spacer. The a fore mentioned discussion leads to the conclusion that the proposed device might be a viable option for future low-power uses.

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