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Optimizing Gallium Nitride (GaN) Based SOI-TF-FinFETs for Enhanced Linearity and Low Distortion in High-Frequency Applications

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Gallium Nitride (GaN) based Fin Field-Effect Transistors (FinFETs) represent a breakthrough in semiconductor technology, especially for applications requiring high power, high frequency, and high efficiency. GaN is a wide bandgap semiconductor material known for its excellent electrical properties, including high electron mobility, breakdown voltage, and thermal stability. These characteristics make GaN an ideal candidate for next-generation electronic devices, particularly in RF and microwave communication, power amplification, and high-speed digital circuits. This paper investigates the GaN-SOI truncated FinFET (GaN-SOI-TF-FinFET) designed for high-performance linearity and low distortion, focusing on key metrics such as second-order and third-order transconductances (g_{m2} and g_{m3}) values, third-order intercept points (IIP3), second and third harmonic distortions (HD2 and HD3), third-order intermodulation distortion (IMD3), and the 1-dB compression point (P1dB). By leveraging the high electron mobility and wide bandgap of GaN, we have optimized the fin dimensions and gate structures to enhance device performance. Our results indicate that the GaN-SOI-TF-FinFET shows significant improvements compared to conventional Silicon FinFETs. The g_{m2}, g_{m3}, HD2, HD3, and IMD3 values are reduced by 42.86%, 62.50%, 112.50%, 56.12%, and 56.25% respectively, while IIP3 and P1dB values are increased by 300% and 100% respectively. These parameter improvements indicate better power handling capacity and robustness of the proposed device, highlighting the potential of GaN-SOI-TF-FinFET for advanced RF and communication applications requiring high linearity and low distortion.

Keywords— TF-FinFET; C-FinFET; SOI; GaN; Linearity, Distortion Reliability and Harmonics

1 Introduction

Planar MOSFETs are the traditional and most widely used transistor structures. In this design, the channel through which current flows is horizontal and parallel to the substrate[1-3]. As the channel length decreases, the short channel effect weakens the gate's control over the channel, increasing leakage currents when the device is off, which leads to higher power consumption, mobility degradation, and parasitic capacitances that affect speed and performance. To address these issues, strained silicon is used to improve carrier mobility and drive current, while silicon dioxide is combined with high-k materials to reduce gate leakage and improve capacitance[4-7].

Fin Field-Effect Transistors (FinFETs) represent a significant advancement over traditional planar MOSFETs, especially as semiconductor technology continues to scale down[8-12]. In FinFETs, the gate wraps around the fin, providing better control over the channel and reducing short-channel effects. This structure offers enhanced electrostatic control, lower leakage currents, improved power efficiency, higher drive current, better scalability, reduced threshold voltage variation, improved parasitic capacitance, and better thermal performance. Truncated FinFETs, which have shorter fin widths, are also critical as they impact the device's electrical properties and performance[13,14]. The fin width in truncated FinFETs is carefully optimized to balance drive current, leakage, and overall device scalability. Narrower fins can reduce short-channel effects, improve electrostatic control, lower leakage currents, enhancesubthreshold swing, and reduce parasitic capacitances, thereby enhancing switching performance and energy efficiency.

Silicon-on-insulator (SOI)FinFETs combine the benefits of SOI technology with the advanced design of FinFETs[15-19]. In this structure, a thin silicon layer sits on top of an insulating layer (usually silicon dioxide), which electrically isolates the active silicon layer from the bulk substrate. The insulating BOX layer reduces parasitic capacitance between the device and the substrate, improving switching speed, reducing power consumptionand leakage currents,

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and enhancing power efficiency, thereby improving scalability.

Gallium Nitride (GaN) has become a preferred semiconductor material in modern technology due to its remarkable properties, which distinguish it from traditional materials like silicon (Si). One of GaN's most significant advantages is its wide bandgap, which is approximately 3.4 eV, compared to 1.1 eV for silicon. This large bandgap enables GaN-based devices to operate at higher voltages and temperatures without breaking down, making them particularly well-suited for high-power applications. As a result, GaN can withstand greater electrical stresses, enhancing the reliability and efficiency of power electronics. GaN also exhibits high electron mobility, which contributes to faster switching speeds and supports higher frequency operation[16, 19-23]. These features make GaN ideal for radio frequency (RF) applications, where speed and efficiency are crucial. Devices that incorporate GaN technology are capable of operating at higher frequencies, offering significant improvements over traditional silicon-based devices.One specific example of how GaN is applied to enhance device performance is the GaN-SOI-TF-FinFET design. This innovative approach integrates GaN with a SOI substrate and utilizes a thin-film truncated FinFET structure. By combining these technologies, the design achieves superior efficiency, power density, and thermal management. These improvements make the GaN-based devices highly effective for a variety of demanding applications, such as high-performance power electronics and high-frequency RF systems, where both reliability and energy efficiency are essential.

2 Simulation Description and Methodology

The doping concentration for all the simulated n-type devices was kept constant at 1.0×10^{20} cm for both the source and drain and 1.0×10^{15} cm^{-3} for the substrate. Additional parameters used in the analysis of the device structure, as shown in Fig. 1, are provided in Table 1. Several physical simulation models were employed to predict and analyze the electrical behavior of the devices. The Bohm Quantum Potential (BQP) model was used to evaluate the effects of quantum confinement on electron and hole concentrations. This model investigates the position-dependent quantum potential, ultimately determining the charge carrier potential energy in the region of interest. The Fermi statistical model addresses bandgap shrinkage that occurs at high impurity concentrations, considering the doping-induced shifts in the conduction band minimum and valence band maximum, which can significantly influence device behavior. To address the distortion of simulated device properties caused by the interaction of electrons and ionized atoms at the drain-channel interface, where a sufficiently large electric field develops, the doping-dependent SRH recombination model was employed. Additionally, Crowell and Sze's impact ionization model was used to describe the relationship between electric field generation and ionization rate[24].

3 Calibartion & Validation

Figure 2 illustrates the calibration of our simulated results with those from previously published experimental research[25]. In the figure, the labels "Simulated" and "Reference" represent our results and the previously published results, respectively. Minor

Table 1 — The Device Parameters of GaN-SOI-TF-FinFET

Serial No.	Device Dimension	
	Parameter of Device	Dimension (nm)
1	Thickness of Gate Oxide (t_{ox})	1.5
2	Length of Channel (L_x)	7
3	Width of Lower Fin (F_l)	3
4	Width of Upper fin (F_u)	8
5	Height of Fin	8
6	Width of Spacer (T_{rc})	1
7	Length of Source and Drain	9

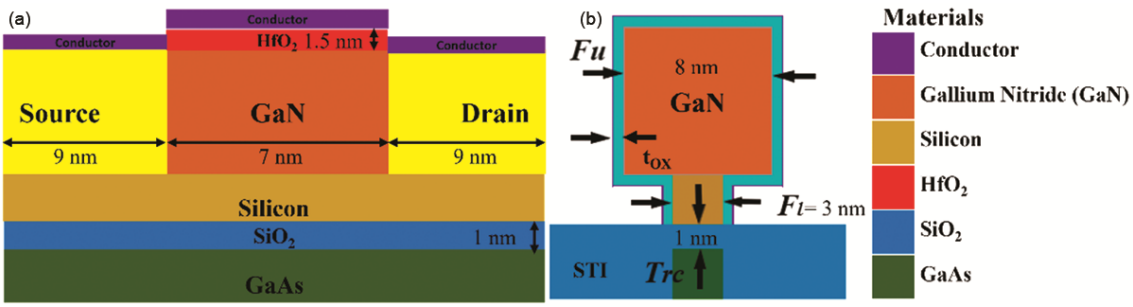

Fig. 1 — (a) Three-dimensional structure of GaN-SOI-TF-FinFET, (b) Lateral cross-sectional view of GaN-SOI-TF-FinFET at 7 nm Gate length

deviations are observed in the comparison. By using the previously published research as a benchmark, our simulated results have been calibrated to be approximately consistent.

4 Discussion on Results

Figure 3(a) shows the variation in drain current (I_{DS}) with gate-source voltage (V_{GS}) for various existing FinFETs (C-FinFET, TF-FinFET, and SOI-TF-FinFET) and the proposed GaN-SOI-TF-FinFET. The analysis reveals that the TF-FinFET exhibits a 6.67% improvement in drain current compared to the C-FinFET, the SOI-TF-FinFET shows a 20.00% improvement, and the GaN-SOI-TF-FinFET demonstrates a 60.00% improvement. Thus, the GaN-SOI-TF-FinFET exhibits superior performance in terms of drain current relative to the C-FinFET, TF-FinFET, and SOI-TF-FinFET. Fig. 3(b) illustrates the variation in transconductance (g_m) concerning gate-source voltage (V_{GS}) for the various FinFETs and the proposed GaN-SOI-TF-FinFET. Transconductance is defined as the rate of change of the drain current (I_{DS}) with changes in gate-source voltage (V_{GS}) while keeping the drain-source voltage (V_{DS}) constant. Mathematically, it is expressedin equation (1)[12] as follows:

$$g_{m=}\frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=Constanat} \quad \ldots(1)$$

Figure 3(b) shows the following improvements in transconductance compared to the C-FinFET, TF-FinFET: 11.33%, SOI-TF-FinFET: 33.33%, and GaN-SOI-TF-FinFET: 66.66%. These results demonstrate that the proposed GaN-SOI-TF-FinFET achieves a significantly better transconductance value than all other existing FinFETs. Therefore, the GaN-SOI-TF-FinFET offers superior analog performance relative to the other FinFETs.

The higher-order derivatives of transconductance are measured to assess the linearity and distortion performance of FinFETs. The nth-order derivative of the transconductance is represented by the mathematical expression (2)[12]:

$$g_{mn}=\frac{1}{n!}\frac{\delta^n I_{DS}}{\delta V_{GS}^n}, where\ n = 1,2,3 \quad \ldots(2)$$

For better linearity and reduced distortion, the values of these higher-order derivatives should be as low as possible. Figs. 4(a & b) show that the values of g_{m2} and g_{m3} for the GaN-SOI-TF-FinFET are lower compared to the existing C-FinFET, TF-FinFET, and SOI-TF-FinFET. This indicates that the GaN-SOI-TF-FinFET offers superior linearity and lower distortion performance than the other FinFETs.

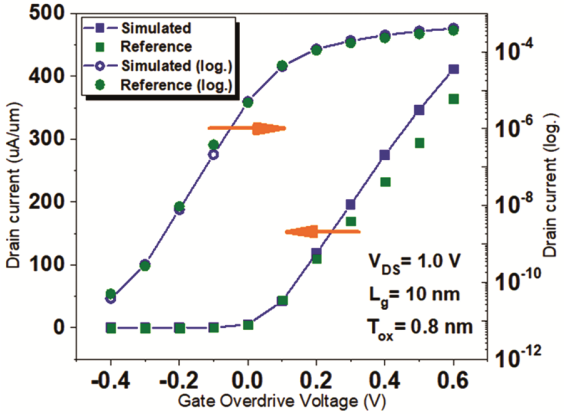

Fig. 2 — Results calibrations of the experimental work against our simulated work at a gate length of 10 nm

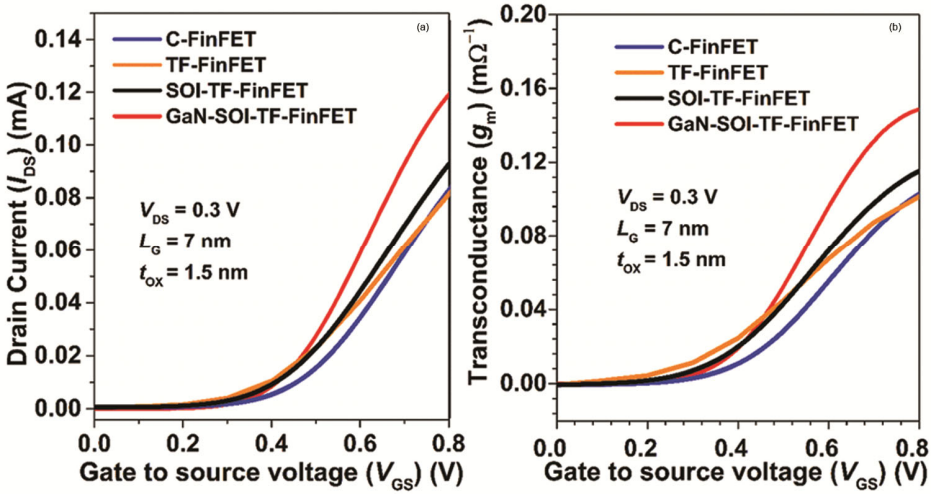

Fig. 3 — (a) Transfer characteristics of the various FinFETs. (b) Transconductance behavior of various FinFETs at different input V_{GS} values

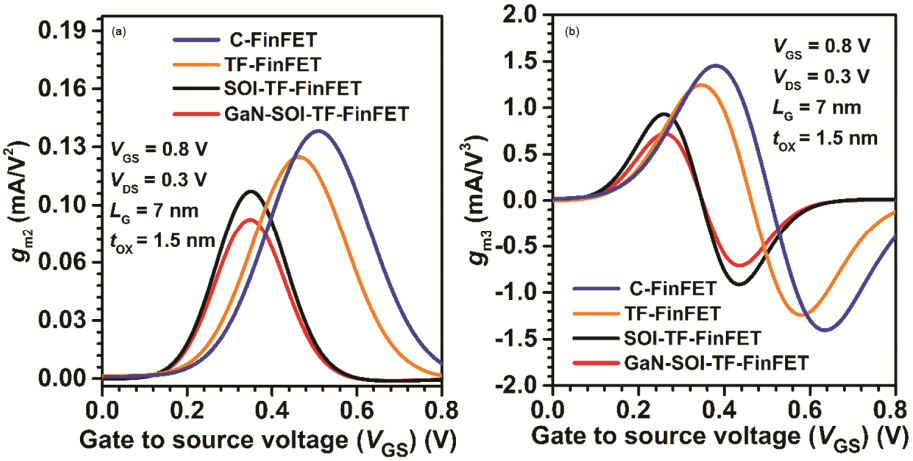

Fig. 4 — (a) g_{m2} for various FinFETs. (b) g_{m3} behaviour of various FinFETs with the variation of V_{GS}

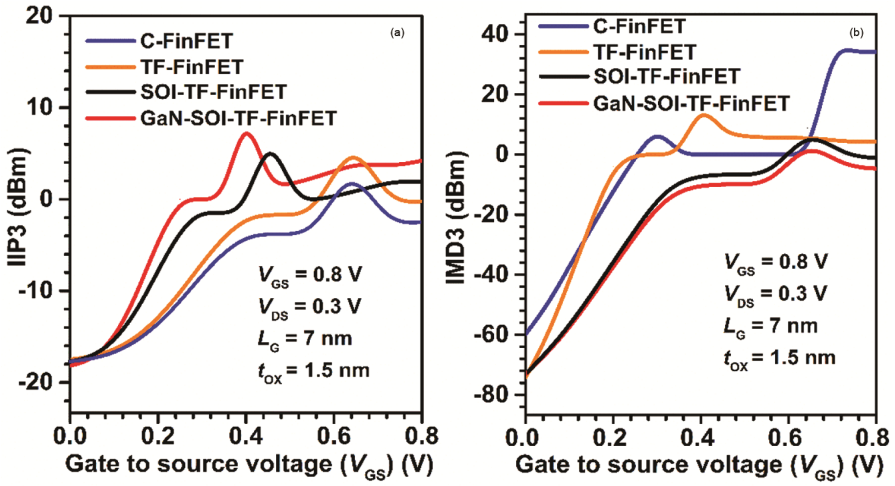

Fig. 5 — (a) IIP3 value for various FinFETs. (b) IMD3 behavior of various FinFETs a the different V_{GS}

The high-frequency performance of a system in communication design is measured in terms of its linearity and distortion behavior. Due to the nonlinear characteristics of these systems, two types of signals are produced in addition to the primary signals: intermodulation signals and harmonic signals. Intermodulation signals typically fall within the bandwidth of the designed system, causing nonlinear and distorted outputs. The nonlinearity and distortion behavior of the system due to intermodulation signals is quantified by parameters such as the IIP3, IMD3, and the 1-dB compression point (P1dB). The HD2 and HD3 parameters measure the nonlinearity and distortion due to harmonic signals. For optimal linearity and minimal distortion, the values of IIP3 and the 1-dB compression point should be high, while the values of IMD3, HD2, and HD3 should be low.

Figure 5(a) shows the variation of IIP3 concerning the V_{GS}. IIP3 is defined as the input power at which the output power of the fundamental signal and the third-order intermodulation signal are equal. A larger IIP3 value indicates better linearity and less distortion in the system. Fig. 5(a) demonstrates that the IIP3 value is larger for the GaN-SOI-TF-FinFET compared to the C-FinFET, TF-FinFET, and SOI-TF-FinFET. This indicates that the proposed GaN-SOI-TF-FinFET offers superior linearity and reduced distortion compared to the existing FinFET systems.

Figure 5(b) shows the variation of IMD3 with respect toV_{GS}. IMD3 is defined as the input current at which the current of the fundamental signal and the third-order intermodulation harmonics are equal. For better linearity and less distortion, the value of IMD3 should be lower. Fig. 5(b) demonstrates that the IMD3 value for the GaN-SOI-TF-FinFET is the

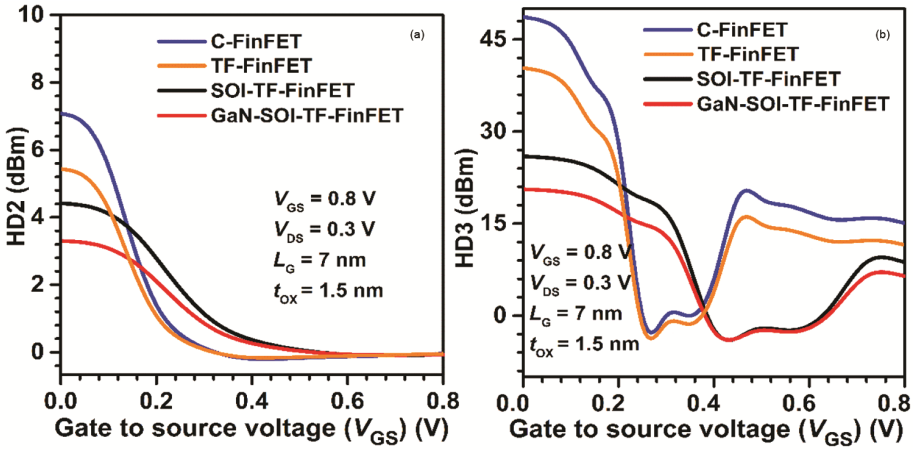

Fig. 6 — (a) HD2 for various FinFETs. (b) HD3 behavior of various FinFETs a the different V_{GS} values

lowest compared to the C-FinFET, TF-FinFET, and SOI-TF-FinFET. Therefore, the GaN-SOI-TF-FinFET provides better linearity and reduced distortion.

The mathematical expressions for IIP3 and IMD3[12] are as follows:

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3}\times R_s} \quad ...(3)$$

$$IMD3 = (\frac{9}{2} \times (VIP3)^3 \times g_{m3})^2 \times R_s \quad ...(4)$$

The IIP3 value is given with a source resistance (R_S) of 50 Ohms. A larger IIP3, as shown in equation (3), indicates a higher first-order transconductance value (g_{m1}) and a lower value of g_{m3} . Consequently, this results in a larger drain current and a less distorted signal for the GaN-SOI-TF-FinFET. The lower IMD3 value, as shown in equation (4), for the GaN-SOI-TF-FinFET corresponds to a lower g_{m3} , thereby producing a more linear and less distorted signal.

Figures. 6(a&b) show the variation of HD2 and HD3. For a design system to achieve minimal distortion, these values should be as low as possible. The observations in these figures indicate that the HD2 and HD3 values are lowest for the GaN-SOI-TF-FinFET compared to the C-FinFET, TF-FinFET, and SOI-TF-FinFET. Thus, the proposed GaN-SOI-TF-FinFET demonstrates superior undistorted performance in terms of second and third-order harmonics. The mathematical equations for HD2 and HD3[12] are as follows:

$$HD2 = 0.5\, V_a \frac{\frac{dg_{m1}}{dV_{GT}}}{2g_{m1}} \quad ...(5)$$

$$HD3 = 0.25\, V_a^2 \frac{\frac{d^2g_{m1}}{dV^2_{GT}}}{6g_{m1}} \quad ...(6)$$

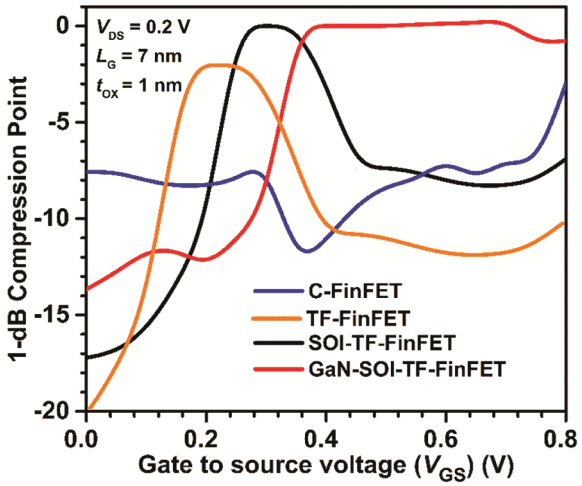

Fig. 7 — 1-dB Compression Point (P1dB) for various FinFET at the different V_{GS} values

where V_a is the voltage of the AC signal as of 50 V. As g_{m1} is the minimum for GaN-SOI-TF-FinFET, the values HD2 and HD3 arethe minimum for the proposed system.

Figure 7 illustrates the variation of the P1dB against V_{GS}. This represents the output power level at which the output power deviates by 1-dB from the theoretically linear value. This is the point where the signal begins to compress, linearity breaks down, nonlinearity starts, distortion begins, and the signal starts to saturate. The 1-dB compression point should be as high as possible for improved linearity and minimal distortion. According to the graph, the P1dB is highest for the proposed GaN-SOI-TF-FinFET compared to the C-FinFET, TF-FinFET, and SOI-TF-FinFET. Therefore, the GaN-SOI-TF-FinFET provides better linearity and less signal distortion than existing technologies.In this work, the proposed GaN-SOI-TF-

Table 2 — Various parameters for analogperformance, linearity, and distortion-free operation in different device types

Device Type	I_{DS} (mA)	g_m (mA/V)	g_{m2} (mA/V^2)	g_{m3} (mA/V^3)	IIP3 (dBm)	IMD3 (dBm)	HD2 (dBM)	HD3 (dBM)	P 1dB
GaN-SOI-TF-FinFET	0.12	0.15	0.08	0.6	6	-4	3.4	21	0
SOI-TF-FinFET	0.09	0.12	0.11	0.9	2	-2	4.4	27	-1
TF-FinFET	0.08	0.1	0.13	1.3	0	4	5.6	39	-2
C-FinFET	0.075	0.09	0.14	1.6	-3	32	7.8	48	-8

FinFETid compared with existing C-FinFET, TF-FinFET, and SOI-TF-FinFET designs. As detailed in Table 2, our analysis demonstrates that the GaN-SOI-TF-FinFET offers superior analog performance, linearity, and distortion characteristics,making it ideal for high-frequency RF applications.

5 Conclusion

The analog, linearity, and distortion performance of the proposed GaN-SOI-TF-FinFET have been compared with C-FinFET, TF-FinFET, and SOI-TF-FinFET. As summarized in Table 2 and as per the result analysis, the proposed GaN-SOI-TF-FinFET demonstrates the highest drain currents (I_{DS}) and transconductance (g_m) parameters compared to existing FinFETs, indicating superior analog performanceandalso highlights that the proposed device also excels in parameters such as gm_2, gm_3, IIP3, IMD3, P1dB, HD2, and HD3, resulting in better linearity and distortion-free performance. Therefore, the GaN-SOI-TF-FinFET is a promising option for future system designs requiring excellent analog, linearity, and distortion-free performance in electronic applications for better power handling capacity and robustness for RF Signal operations.

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