Indian Journal of Pure & Applied Physics
Vol. 64, January 2026, pp. 7-17
DOI: 10.56042/ijpap.v64i1.14342

Ku-Band Ring Oscillator Architecture with Frequency Tuning and Phase Noise Mitigation

Rachana Arya[a, b*] & B K Singh[c]

[a]Veer Madho Singh Bhandari, Uttrakhand Technical University, Dehradun 248 007, India

[b]Department of Electronics and Communication Engineering, Bipin Tripathi Kumaon Institute of Technology, Uttarakhand 263 653, India

[c]Department of Electronics and Communication Engineering, Birla Institute of Applied Sciences, Bhimtal, Uttarakhand 263 136, India

Received:12th October 2024; accepted:12th November 2025

This study presents a 14.5 GHz Ku-band Voltage-Controlled Ring Oscillator (VCRO) designed in 45 nm CMOS technology, operating with a supply voltage from 0.1V to 1.3V and covering a frequency range of 0.034 GHz to 16 GHz. At 1.3V, the simulated delay time is 0.04 ns, while at 1V, it increases to 0.068 ns. The design achieves a phase noise of –80.17 dBc/Hz at 1 MHz offset and –105.3 dBc/Hz at 100 MHz offset, with a power consumption of only 3.26 µW at 1V. The five-stage ring oscillator demonstrates a 23.5% tuning range, spanning 11.2 GHz to 16 GHz. By utilising 45 nm CMOS scaling, the proposed VCRO attains enhanced power efficiency, frequency stability, and integration capability. The delay-stage optimisation effectively minimises phase noise while preserving a broad tuning range. Compared with existing designs, this oscillator exhibits superior frequency stability and power-performance trade-off, efficiently balancing phase noise, tuning range, and power consumption. Despite challenges from device variability and limited voltage headroom in advanced nodes, the proposed VCRO sustains low phase noise and stable frequency operation, establishing a robust low-power solution for Ku-band and next-generation CMOS communication systems.

Keywords: Voltage control ring oscillator, Delay, 45 nm Technology, Noise margin, Power utilisation

1 Introduction

1.1 Research Motivation

The primary motivation for this research is to address several challenges associated with the design of voltage-controlled oscillators (VCOs) used in various communication systems. The link budget of wireless communication, which the VCO primarily sets, has a significant impact on the performance of a transceiver. Essential issues in VCO design include reducing the noise input of the VCO to the entire system, achieving a wide tuning range, minimising size, functioning on a low supply voltage, and maintaining suitable power consumption. Furthermore, sub-micron inductor design poses significant challenges for accurate on-chip modelling.

Ring oscillators play an indisputable role in electronic commerce. The enormous growth of the VLSI field led to an unreasonable increase in its values[1-2]. A steady cyclic signal is necessary for sampling, organising, and frequency synthesis in all contemporary communication structures. An integrated on-chip oscillator produces a clock signal. The design of the voltage control oscillator presents several challenges, including achieving a wide tuning range, minimising size (which is difficult due to the requirement for specific technological qualities), operating on a low supply, and maintaining an ideal power consumption.

Voltage oscillators can be broadly classified into two types: ring-type and LC-type oscillators[3]. The LC type exhibits specific characteristics, such as exceptional frequency performance and superior phase noise, due to its high-quality factor. The centre frequency is greatly affected by the inductor and capacitors. This oscillator's characteristic impedance is directly correlated with the values of the inductor[4].

Since the advent of VSATs (Very Small Aperture Terminals), Ku-band has been used more frequently in a variety of applications. This is due to its effectiveness, robustness, and low equipment utilisation, which reduces complexity and logistical costs[5]. The Ku-band frequency in the frequency spectrum ranges from 12 to 18 GHz, corresponding to wavelengths between 2.5 and 1.7 millimeters. The satellite communications industry has utilised Ku-band extensively since NBC started using it as a direct broadcasting option in 1983. Digital TV services, including sports, conference calls, foreign content, news feeds, educational programs, and other

*Corresponding author: E-mail: rachna009@gmail.com

backhauls, are primarily provided by powerful satellites. The usage of it varies according to the locale[6–7].

The RO is produced more frequently than any other integrated circuit. A variable negative feedback circuit is created by the RO, which is essentially a closed loop consisting of an odd number of identical inverters. The oscillation time of an inverter ring is double the total of the ring's gate delays. First, an Ethernet controller utilised a voltage-regulated VCO-ring CMOS inverter-based oscillator to recover clocks[8–9]. RO occupies a substantial amount of the minimal chip area. Additionally, it can oscillate at extremely high frequencies; the duration of the oscillation is only limited by the combined effect of several gate delays. The relaxation oscillator's maximum oscillation frequency is always lower than that of the RO[10].

Phase-locked loops (PLLs) are frequently used to provide clock pulses for various applications, including input and output interfaces, analog-to-digital (A-to-D) converters, mixer blocks for super-heterodyne receivers, and biomedical devices. The VCO circuit produces high-frequency signals when the phase and frequency detector's input wire is connected to the low reference[11]. The charge pump controls the VCO, which generates the high and low (sometimes referred to as up and down) signals. The VCO, which relies on the phase and frequency differences between the input and feedback signals, is a crucial component of the PLL[12]. To counteract the losses caused by the series resistance, power consumption increases when a parallel resistance is connected to sustain oscillations.

It can be challenging to maintain circuit complexity when eddy current induction, a larger layout area, and the resulting resonant frequencies are present. Ring oscillator architecture is an alternative that offers minimal power consumption and a broad frequency range. Phase-locked loops, analogue-to-digital circuits, and voltage-controlled oscillators all remarkably regulate these ring oscillators. Because they utilise less chip surface, these oscillators have a higher chip density. It does, however, have some serious issues, including frequency restrictions, the number of stages utilised, and the delay time between each inverter[13]. A 45-nm CMOS technique is used in the projected design to reach a maximum frequency of 5.2 MHz.

The objective of this article is to design a VCRO that can drive high capacitance loads with minimal latency, size, and power consumption, all without requiring additional clock-tree buffers. To reduce power consumption and shorten circuit delay times, a five-stage ring oscillator (FSRO) with the fewest possible transistors is also designed. Because 45 nm CMOS technology is used in the oscillator circuit design, a variable supply voltage is possible. This varying supply may raise the transconductance of the circuit by reducing the transistor threshold voltage. Consequently, the oscillator achieves a high figure of merit, low power consumption, and a wide frequency range.

1.2 Research Contribution

This work advances the field by providing a thorough design process for a CMOS five-stage current-starved ring oscillator. The suggested VCO shows notable improvements over earlier designs in terms of delay and power waste. In particular, it achieves good linearity and a wide tuning range of approximately 23.5% when the supply is varied. The durability of the design is confirmed by the parametric research conducted at various temperatures, control voltages, and processing corners. With an 869-μW delay and an RMS current of 17.2 mA, the suggested VCO achieves a centre frequency of 14.5 GHz. With a high-level noise margin of 0.27V and a low-level noise margin of -0.22V, it is ideal for Ku-band applications, including radar systems and satellite communications.

2 Literature Review

A three-stage ring oscillator (TSRO) operating at a supply voltage of 1 V was proposed. Ring oscillators, which can be detected and characterised using modelling resources, form the basis for examining variations in circuit behaviour caused by industrialised design and layout factors. Similar to an inductor, this type of oscillator was noise-free in contrast to LC, Hartley, Colpitt, and tuned oscillators, all of which were used in circuits[14-15]. Methodological variability, the moderate scaling of Complementary Metal Oxide Semiconductor (CMOS) transistors, and circuit design techniques. A ring oscillator with constant capacitors (1 pF) and variable capacitors (1 to 100 pF) has also been analysed.

CMOS VCOs suitable for PLL applications were presented. In this case, the oscillator output frequency of a VCO circuit was controlled by the control voltage[16]. Additionally, the Cadence Create Suite was used to design the Current starved voltage controlled

oscillator (CSVCO), which utilises GPDK 90 nm CMOS technology and operates at a 1.8 V supply voltage. When the control voltage reduced the VCO's frequency, the phase error was driven toward zero. A nonlinear VCO gain could considerably lower the PLL performance quality. A difficulty with this design is that the output oscillation frequency is not directly proportional to the control voltage.

High-frequency oscillators for clock generation, clock recovery, and high-speed communication were investigated using Cadence Virtuoso in 90 nm technology[17]. They created a CSVCO with and without a resistor, as well as a FSRO. Following its integration into a PLL, oscillation frequency and power consumption were used to compare performance[18]. The CSVCO's output waveform differed from a pure sine wave; however, the results showed that it could attain a higher frequency with less power consumption than the standard ring VCO, making it more suitable for high-speed communication[19].

A five-stage current-starved CMOS VCO for PLL applications was presented; however, power consumption remains a key concern in low-voltage operation[20]. The design employed a straightforward ring oscillator composed of cascading inverters, and the size of the transistors was crucial in determining the centre frequency of the VCO. Precise frequency tuning according to application requirements was made possible by minimising the frequency variation from the intended value through transistor dimension optimisation[21]. Although parasitic effects were shown to potentially impact overall power performance, the schematic-based design exhibited minimal power consumption, making it suitable for a variety of circuit applications.

A controller-based all-digital phase-locked loop (ADPLL) using a 45 nm CMOS process was proposed[22]. A differential ring oscillator (RO) utilising a differential buffer concept and a capacitive boosting technique was developed after the design began with an open-loop phase frequency detector. The ADPLL attained a locking frequency of 402 MHz when all components were integrated. The capacitive-boosted differential oscillator enabled operation at a lower supply voltage of 0.68 V, and the frequency controller block simplified the system by eliminating the need for a time-to-digital converter (TDC).

A high-frequency PLL architecture with a wide tuning range of 2.4-5 GHz for wireless applications was introduced[23]. The study encompassed design decisions, computations, simulations, theoretical modelling, and real-world applications. The adoption of a scaled supply voltage technique improved performance metrics and decreased the time required for numerical analysis and model identification, according to simulation data. Power consumption in the PLL circuits was still a problem for the design, though.

An ultra-low-power hybrid ring oscillator VCO was designed by integrating a conventional CMOS inverter with a current-starved power-switching inverter to enhance frequency range and tuning while reducing phase and output noise; however, implementation complexity may increase[24]. The results demonstrated high scalability and efficiency, along with enhanced sensitivity, a wider tuning range, and a higher oscillation frequency, all achieved with reduced power consumption.

The following are the primary difficulties with the earlier work.

The performance of the transceiver is directly impacted by the link budget of wireless communication, which the VCO primarily determines. Reducing the noise input of the VCO to the whole system is a constant source of difficulty and ongoing research. Moreover, several obstacles, including achieving a wide tuning range, reducing size (which is challenging due to the need for specific technological characteristics), operating on low supply, and maintaining an appropriate power expenditure, confront the design of the VCO. More significantly, compared to a discrete inductor, there is a discernible drop in inductance per unit area. Furthermore, exact on-chip modelling faces substantial hurdles when designing inductors at the sub-micron level. The more current pushed into the oscillator, the lower the noise level at its output. For oscillators, the trade-off between power consumption and power net poses an intriguing design challenge because high power consumption reduces device lifetime.

3 Structure of Ring Oscillator

The ring oscillator's preview is shown in Fig. 1. A portion of the throughput is supplied back to the three inverter stages, which are connected in series, to maintain the oscillations. A loop of "n" inverter stages, connected in reverse order, creates an oscillated output, which is the optimal RO[25-26]. Supporting the VCO, which is perhaps the most crucial block in the PLL, is the primary function of the RO. It is used to regulate mid-range frequency and

bandwidth. As the centre frequency shifts, the tuning range also shifts.

Non-linearity in the tuning range arises when the VCO's gain is altered. Moreover, the primary goal of the VCO is to maintain constant oscillation, which keeps the lock state in place[27]. However, the VCO's output is not ideally periodic; instead, its input is a continuous error voltage. The primary source of supply noise in all electronic equipment is increased output, which results in jitter. Using an odd number of inverters in the circuit will not result in a fixed operating point. When the output oscillates and fulfils a closed-loop system's gain (higher than 1), the first criterion is met. According to the second standard, a 180° phase shift requires at least three holdup cells.

The propagation delay is seen in Fig. 2. To achieve the fastest oscillation, three inverter stages are needed. The planned RO is deliberately organised by minimising the number of phases that cause delays because it is recognised that adding additional processes increases power consumption. To reduce power consumption, fractional positive feedback is also recommended.

In a FSRO, the first inverter switches its output to logic “1” at time t_1. The output of the first stage toggles to logic "0" as a result of this signal passing through the subsequent two inverters and feeding back to it[28]. Continuous oscillations are produced when the output switches once more as the new state moves through the loop. A complete cycle happens when the signal completes two transitions, from low to high and from high to low, and each inverter adds a propagation delay. The sum of all stage delays is twice the overall oscillation period. However, the average propagation delay can be regarded as a reliable approximation because the rising and falling transition periods are not the same[29]. The clock, input, and output waveforms are designated A, B, and C in Fig. 2, together with the relevant input-output delays. Every inverter has a single fan-out. Due to its straightforward transistor structure, the RO features a compact layout and low power density. For high-speed applications, it offers a broad tuning range and is simple to tune.

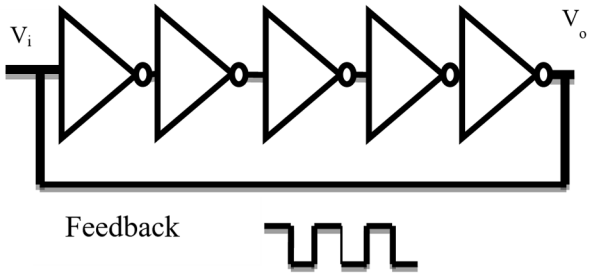

Fig. 1 — Preview of single-terminated 5-stage ring oscillator

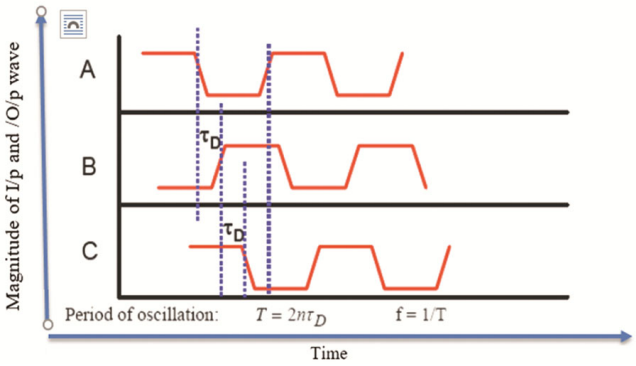

Fig. 2 — Ring oscillator output response

It is considered that $T = 2n\tau_D$, where τ_D represents the delay for each stage, and the oscillation frequency is determined by T, which is the overall oscillation period of the three-stage ring oscillator[30]. A greater oscillation frequency results from a reduction in the overall delay caused by a decrease in the number of delay cells. By adjusting variables such as supply voltage, inverter drive strength, and load capacitance, the RO's performance can be managed. Equation (1) expresses the 5-stage ring oscillator's transfer function G (iω).

$$G_i(\omega) = -\left(\frac{A}{1+i\omega_\tau}\right) \quad \ldots (1)$$

Barkhausen's requirement requires that the overall circuit's phase shift be 180 °. Consequently, each step of this oscillator needs to contribute a 36 ° phase shift[31]. At the oscillation frequency, the size of the gain should be at least 1. The angular frequency determines the oscillation frequency. Consequently,

$$\omega = \frac{\tan\left(\frac{\pi}{5}\right)}{\tau_D} \quad \ldots (2)$$

Each inverter stage's small-signal voltage gain can be stated as

$$A_V = g_m R_d \quad \ldots (3)$$

where g_m is the CMOS transistor's transconductance, which indicates how well the transistor converts input

voltage to output current, and R_d is the drain node's effective load resistance. For oscillation to take place, $A_v \geq 1$. This condition ensures that the amplifier gain in each stage maintains continuous oscillations by compensating for the energy wasted in a single cycle owing to resistive and capacitive effects.

3.1 Important Oscillator Performance Elements

The trade-offs of phase noise, power consumption, signal swing, silicon area, and other factors significantly increase the workload of oscillator design, mainly when they are employed in RF transceivers. Knowing and comprehending the fundamental theories from the perspective of circuit design is essential. The essential design factors are enumerated as follows:

3.1.1 Frequency Range

An R.F. oscillator needs to be capable of operating frequency changes within a given range. An IEEE 802.11b transceiver, for instance, requires a bandwidth coverage of 100 MHz, ranging from 2.4 GHz to 2.5 GHz. However, the range needs to account for an extra margin to accommodate process, voltage, and temperature (PVT) mismatch[31]. The intended frequency tuning range of this VCO will be 2.205 GHz to 2.695 GHz (10%) if the designer decides to include 5 % margin.

3.1.2 Output Voltage Swing

An R.F. oscillator should have an output swing that is sufficiently large to drive the load circuit and reduce the switch's on-resistance or increase the injection-locked frequency divider in the PLL's lock range[32]. The single-ended output swing in the 130 nm process, for instance, should be configured between 0.2 V_{pp} and 1.0 V_{pp} with $V_{ds,\ min}$ = 100 mV. This example illustrates a nominal voltage of 1.2 V. An output buffer is introduced between the oscillator and the load circuit to both isolate the load's impact and enhance the signal.

3.1.3 Phase Noise

Phase noise is often a crucial factor in oscillator design, particularly in environments where circuit and external noise sources are substantial. To illustrate, let's look at a perfect LC oscillator that generates a pure sinusoidal output, which manifests in the frequency domain as a single impulse[33]. However, in real-world applications, sidebands around the carrier frequency emerge due to spectral line broadening caused by resonant tank flaws and noise contributions from active devices.

As the frequency offset from the carrier increases, the LC tank provides greater noise suppression due to its frequency-selective nature. The ratio of the power spectral density at a specific offset frequency to the carrier power, represented in dBc/Hz, is used to quantify phase noise (PN). The methods for reducing noise contributions from active devices in oscillator design are the primary focus of this study. The following section discusses the suggested mitigation techniques and a thorough examination of various noise sources.

3.1.4 Output Waveform

The application and load circuit determine the necessary oscillator waveform. For instance, a sinusoidal LC-tank VCO output can be transformed into a square wave using an output buffer, but a switch-mode mixer requires a square wave with a 50 % or 25 % duty cycle for practical switching. A square wave, on the other hand, is not necessary for an active mixer[34], as it would result in higher power consumption. Therefore, whether a sinusoidal or square waveform is required ultimately depends on the load circuit.

3.1.5 Power Consumption

The power source voltage affects the amount of electricity the VCO dissipates. One design parameter is not the power consumption. In reality, additional design factors, such as frequency, PN, and output swing, are typically traded off against power.

3.2 0.1 V to 1.3 V Supply Variation for a Single-Bit Delay Cell

The inverter in this delay cell can function in both active and inactive states due to the symmetric features of the P-type and N-type MOSFETs that connect the CMOS transistors. As pull-up and load resistors for logic "1" signals, respectively, both transistors in this configuration function, and the NMOS acts as a pull-down transistor for logic "0" signals. As a result, each transistor makes an equal contribution to the circuit[35]. There are two main expenses associated with this circuit: the leakage current power cost and a modest steady-state power cost.

The CMOS inverter's input and output waveforms have been displayed in Fig. 3. The time constant of the projected circuit affects the inverter's propagation delay. The values of the load capacitor and pull-down resistor affect the time constant. The capacitance related to the output, which is composed of wire capacitances, input capacitance of gates connected at load, and diffusion capacitances (Drain) of NMOS

and PMOS transistors. Assuming a static PMOS switch, let's examine the transition from low to high. When charging C_L using PMOS internal resistance R_p, the gate's response time is measured.

The circuit's propagation delay is therefore proportional to the time constant. A fast gate is thus constructed, either by decreasing the PMOS resistance or by selecting a low output capacitance.

Figure 4 illustrates a FSRO. A low signal is sent to the output of the first inverter while a high digital signal is applied to the input and travels to the cell. This signal is transmitted back towards the input terminal once more, and the sequence is initiated once more. Regarding the inverter circuit, when a low signal is applied to the input, PMOS and NMOS are turned on and off, respectively, resulting in the production of a high signal at the output. The input terminal for the following stage receives this high signal. This will cause the NMOS to turn on and the PMOS to turn off, resulting in a low signal.

The connection between the input and output frequencies can be stated as

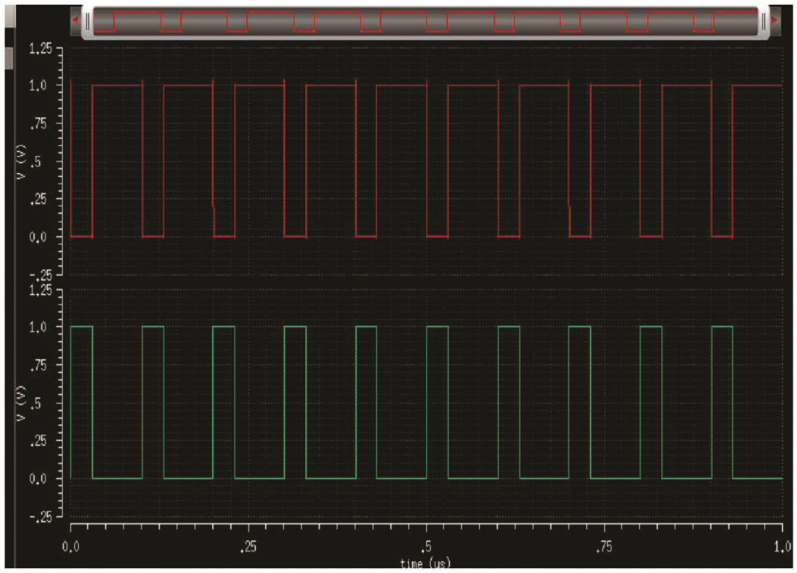

Fig. 3 — Simulated inverter waveforms at both the input and output

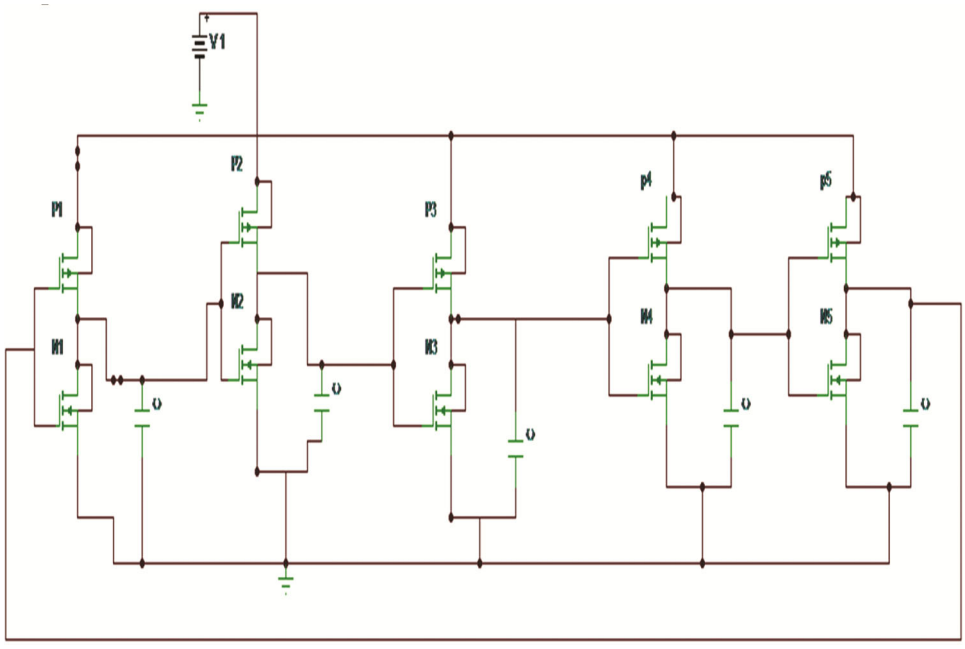

Fig. 4 — Simulated CMOS ring oscillator with time delay of input waveform

$$f_{out} = f_o + K_{VCO} V_{in}(t) \quad \ldots (4)$$

where f_0 is the oscillator's free-running frequency, and K_{VCO} is its sensitivity. Furthermore, the current frequency, $f_{out}(t)$, is equivalent to a derivative of the instant phase, $\Phi_{out}(t)$. This can be represented as:

$$\phi_{out}(t) = 2\pi \int f_{out}(t) dt \quad \ldots (5)$$

Higher-order variations are eliminated in this formulation by the PLL loop's low-pass filter, leaving only the steady-state component of the signal. As a result, the oscillation frequency is determined by

$$f_{osc} = \frac{1}{2n\Delta t} \quad \ldots (6)$$

where Δt is the propagation delay per stage, and N is the number of delay stages. To be used in the filter, the oscillator must enable modification of the output frequency while it is in operation[36-37]. Since the number of inverters can only be determined during circuit design, Δt must be adjustable to ensure voltage-controlled operation. As a result, the control voltage V_{in} changes the output frequency during operation by dynamically adjusting the propagation delay.

The propagation delay of a single inverter stage must be accurately estimated to determine the oscillation frequency. As shown in Fig. 5, the CMOS inverter transistors can be modelled as resistive switches to get a simplified approximation. The charging and discharging behaviour of the load capacitance, which directly controls the inverter delay, can be easily analysed using this resistive model. The overall oscillation frequency can therefore be estimated analytically by approximating the ring oscillator's total delay as the sum of the cumulative delays of all inverter stages.

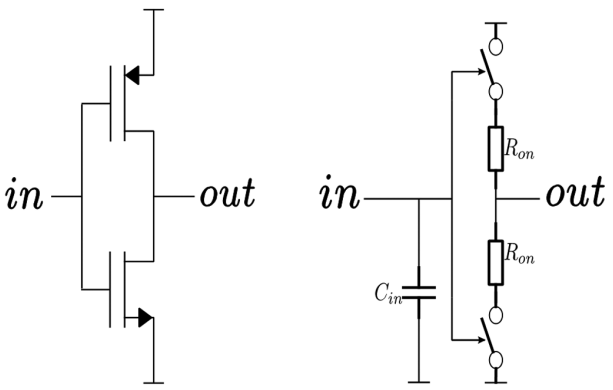

Fig. 5 — Inverter as a delay switch

Anytime the load capacitance C_L and the on-circuit resistance, which appear when the inverter is turned on, form a first-order circuit. The resulting delay can be roughly estimated as t_{delay} (τ_n) = R_{on} C_L.

The next step involves approximating the dominant parasitic capacitances in the CMOS inverter, mainly those that make a substantial contribution to the overall load capacitance, assuming that they are secondary to the transistors' gate-to-source capacitance (C_{gs}). Consequently, while calculating the inverter cell delay in Eq. (7), only C_{gs} is taken into account. The generated delay time expressions successfully show the design trade-offs involved in optimizing oscillator performance, despite the slight inaccuracies introduced by this simplification[38]. Additional parasitic capacitances, such as drain-to-bulk and connection capacitances, should be added to the model for improved accuracy.

$$C_L = C_{gs_n} + C_{gs_p} = C_{ox}(W_n L_n + W_p L_p) \quad \ldots (7)$$

This is an extra approximation, as a simple algebraic model is no longer valid for contemporary CMOS processes. These formulas can be combined to approximate the time constant. Since nMOS and pMOS transistors have different electron mobilities, the word should not be used too literally[10]. However, by scaling the width of the pMOS transistor in accordance with the width of the nMOS transistor properly, an equal time constant may be produced for both transistors.

$$\tau_n = \frac{W_{total} L_n C_{ox}}{\mu_n C_{ox} \frac{W_n}{L_n}(V_{gs} - V_t)} = \frac{W_{total} L_n^{\,2}}{\mu_n W_n (V_{gs} - V_t)} = \frac{L_n^{\,2}}{\mu_n \alpha (V_{gs} - V_t)} \quad \ldots (8)$$

$$f = \frac{\mu_n \alpha (V_{gs} - V_t)}{n L_n^{\,2}} \quad \ldots (9)$$

In Eq. (9), α is the width of the nMOS transistor divided by the total width. To adjust the oscillation frequency, several options are available. However, while the VCO is running, the output frequency must be adjustable. The V_{gs} may be utilised for tuning by adjusting the supply voltage of the inverters. A change in V_{dd} will also affect the logical levels. Consequently, V_{gs} will change. By substituting the value of V_{gs} = V_{dd} - V_{in} in Eq. (4), the following equations can be derived.

$$f_0 = \frac{\mu_n \alpha (V_{dd} - V_t)}{nL_n^2} \quad \ldots (10)$$

$$K_{VCO} = -\frac{\mu_n \alpha}{nL_n^2} \quad \ldots (11)$$

Conversely, the channel length (L) significantly affects the output characteristics. When the device length is doubled, the output frequency equations anticipate a quadratic rise in oscillation frequency, suggesting that the simulation results might not be entirely accurate[39]. As a result, although these analytical formulations are useful for analysing the trade-offs between different design parameters, they are insufficiently accurate for analytically calculating the precise size of a VCO[40-41].

This observation is further supported by the output frequency curve, which tends to grow more sharply with increasing input voltage levels (especially when V_{GS} approaches the threshold voltage). This behaviour implies that, as shown in Fig. 6, the transistors operate in a transient region between saturation and cut-off rather than staying entirely in saturation. At the same time, the output frequency exhibits a near-linear dependence at low input levels.

The following parameters can describe the voltage transfer characteristics (VTC) of the CMOS inverter.

The high voltage input (V_{IH}), with a value of 0.55V, is the lowest input level at which the inverter output remains at logic "1." The low voltage output (V_{OL}) indicates the low-level output at point B, which is 0.18V, whereas the low voltage input (V_{IL}) is equivalent to 0.4V, the maximum input level at which the output remains at logic "0."The noise margins, which measure the inverter's resistance to input signal disruptions, are defined by the difference between the high-level and low-level voltages. The high-level noise margin (NM H) is computed as follows: V_{OH} - V_{IH} = 0.82-0.55=0.27V, and the low-level noise margin = V_{IL}- V_{OL} =0.4 - 0.18 = 0.22V.

4 Simulation Results and Discussion

The oscillation frequency fluctuation as a function of control voltage is shown in Fig. 7. As can be seen, up to approximately 0.7V, the oscillation frequency increases roughly linearly with the applied control voltage; thereafter, the rate of change begins to saturate. At V1 = 0.3V, the associated frequency (f_1) is 1.8 GHz, but at V2 = 0.7V, the frequency (f_2) rises dramatically to 11.4 GHz. This behaviour illustrates the VCO's large tuning range.

For phase-locked loop applications, predictable frequency control is ensured by the near-linear region between 0.3 V and 0.7 V. The transistor's passage from the saturation area into the velocity-saturation regime at higher gate voltages is responsible for the gradual saturation trend that is visible beyond this region. This feature suggests that the frequency sensitivity (K_{VCO}) is voltage-dependent and exhibits greater linearity in the middle of the range.

Based on the simulation analysis, the frequency at 1V is around 14.4 GHz. Furthermore, the capacitors in each step calculate the rising and falling durations for each delay cell output. It is essential to note that the circuit's functioning is affected by the supply voltage when this ring oscillator is in use. The relationship between propagation delay and supply

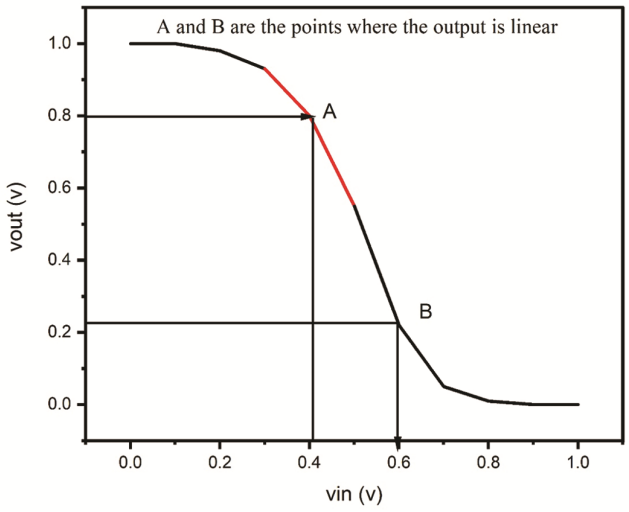

Fig. 6 — Voltage Transfer characteristics with linear points A and B

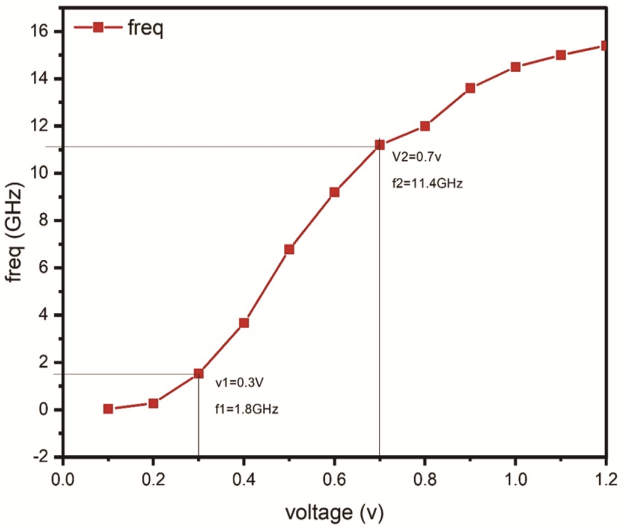

Fig. 7 — Frequency at V1 and V2 (as linear analysis)

voltage (V_{dd}) is illustrated in Fig. 8. As shown, the delay exhibits a sharp exponential decline with an increase in V_{dd} up to approximately 0.3V, after which the reduction becomes insignificant, and the delay stabilizes at a low value.

Propagation latency is enhanced at lower voltages, approximately 50 ns at V_{dd} = 0.1V, because carrier mobility and driving current are significantly reduced. The delay quickly decreases to less than 5ns when V_{dd} rises to 0.3V, indicating the high voltage dependence of switching speed in subthreshold and near-threshold areas. It has been observed that as the voltage increases, the gate delay decreases, and vice versa. The dimensions of PMOS for this structure are L_P = 45 nm and W_P = 450 nm. L_n = 45 nm and W_n = 180 nm are the dimensions of NMOS.

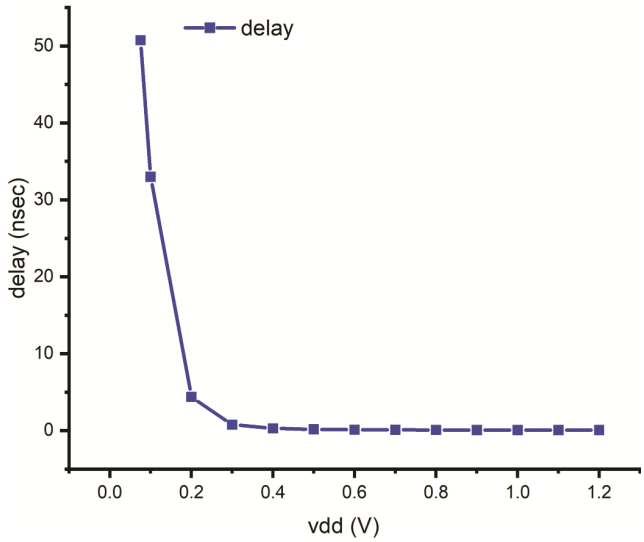

Fig. 8 — Delay at voltage ranges from 0.1 V to 1.2V

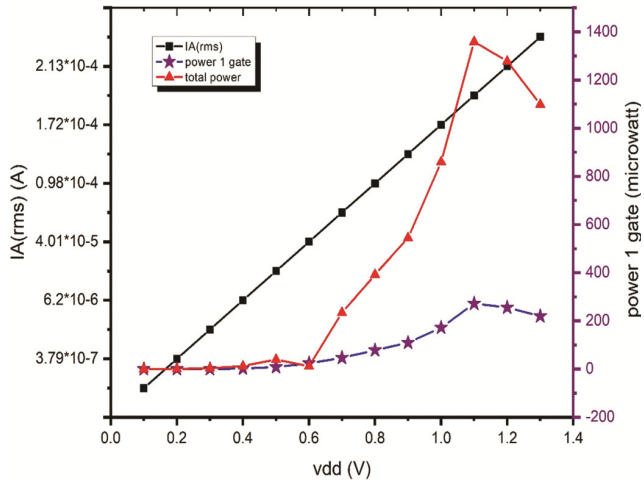

Fig. 9 — Simulated analysis of one cell delay, total power, and current drawn by a five-stage ring oscillator

This FSRO has a total duration of 0.068 nanoseconds. To determine the amount of power consumed at each voltage level, the root mean square value of the current was recorded. The suggested ring oscillator (RO) has a frequency tuning range of 0.030 GHz at 0.075V to 16 GHz at 1.3V, as shown in Fig. 9. To verify the theoretical and mathematical calculations, a CMOS RO was created and simulated utilising 45 nm CMOS technology. Supply voltage of 1V, load resistance of 50 Ω, load capacitance of 0.01 pF, and transistor dimensions of W/L=180 nm/45 nm for nMOS devices and W/L=450 nm/45 nm for pMOS devices.

The oscillator circuit's overall power consumption ranges from 19.5 nW at the lowest operating voltage to 1098.5 µW at the highest control voltage. Accordingly, depending on the applied voltage level, the power consumption per gate varies from 3.9 nW to 219.7 µW. The power-delay product (PDP) consistently declines with increasing supply voltage, as shown in Fig. 9, according to the delay study conducted across the same voltage range.

As shown in Fig. 10, the phase noise is -80.17 dBc/Hz at a 1 MHz offset and -105.31 dBc/Hz at a 100 MHz offset frequency. The sweep range is 0.034–16 GHz. Effective noise isolation within the architecture is demonstrated by the output buffer and EF buffer sections, which exhibit comparatively better noise performance at higher offset frequencies. The accuracy of the suggested analytical phase noise model is confirmed by the strong correlation between the computed and simulated results (as indicated by the dotted line). Overall, the findings support the In-Triggered CMOS VCO's superior phase noise

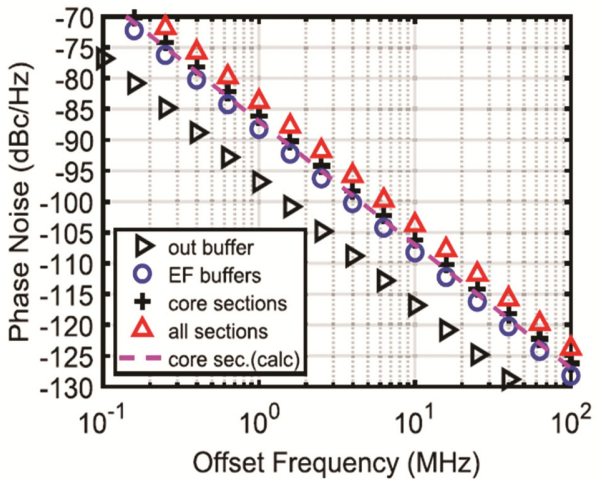

Fig. 10 — Relational offset frequency versus phase noise

Table 1 — The suggested VCOs' comparison with earlier findings

Parameters	References								
	[36]	[38]	[39]	[40]	[41]	[42]	[43]	[44]	This work
Technology / Vdd	45nm, 2V	180nm, 1V	180nm, 1.2V	90nm, 1V	90nm, 1.2V	65nm, 0.75V	45nm, 1.2V	45nm, 1V	45nm, 1V
Structure	Ring	Ring	Ring	Ring	Ring	Ring	Ring	Ring	Ring
Ln=Lp	45 nm	180	180	90 nm	90 nm	60 nm	45 nm	45 nm	45nm
Wn	1μm	—	900 nm	—	—	24 μm			180nm
Wp	2μm	—	560 nm	—	—	48 μm			450nm
Voltage range	1.7-1.8 V	0.62-1V	0.2 V and 1.6 V	1.2V	1.2 V	0.75V	1.2 V	0.8-1.2V	0.075-1.3V
Frequency range (GHz)	24-25 (GHz)	1.03 (GHz)	573 to 852.8 MHz	1.3–1.5 (GHz)	1.33 (GHz)	4.72-6.12 (GHz)	1.33(GHz)	0.625-4.88 (GHz)	0.034-16 (GHz)
Consumed power	3.43 mW	2.5mW	0.965 mW	46.05 μW	0.0446	15.45 mW	0.053 mW	0.0293 mW	3.26 μW
Tuning range (%)	2.06	53	8.6	--	98	95.48	98	95.09	23.5
Phase Noise dBc/ Hz at 1MHz offset	-71.61	-105.5	-108.03	−78.28	--	−103.2	-95.15	-125.92	-80.17

performance and stability, both of which are critical for high-frequency, low-power PLL applications.

4.1 Comparative Methods

This section compares the suggested work in this paper with other available literatures[42-43]. The suggested CMOS ring VCO, developed in 45 nm technology, provides an exceptional balance between frequency tunability, power efficiency, and phase noise performance, as indicated by the comparative analysis presented in Table 1. The proposed architecture achieves effective oscillation at a minimum supply voltage of 0.075 V, extending up to 1.3 V, while maintaining stable operation. In contrast, conventional ring oscillators require higher bias voltages and experience significant dynamic power losses. The design's ability to sustain high-speed performance over a broad control voltage range is demonstrated by its maximum oscillation frequency of 16 GHz, confirming its suitability for broadband PLL applications.

The suggested design achieves nearly 99.1% lower power consumption than the 45 nm, 2V implementation[36]. Over 98 % lower consumption than numerous higher-technology node counterparts, when compared quantitatively with previous research[44], and compared to previous oscillators, which were usually limited to below 6 GHz. The oscillation frequency of the current-starved ring VCO changes from 0.034 GHz at 0.075 V to 16 GHz at 1.3 V, achieving a broad tuning range of 23.5 %, according to experimental evaluation.

When compared to earlier CMOS VCO architectures working under comparable conditions, the overall power consumption is as low as 3.26 μW, a 99 % reduction. The oscillator's spectrum stability is confirmed by the observed phase noise of –80.17 dBc/Hz at a 1 MHz offset, and the delay–voltage analysis shows a sharp decrease in propagation delay with increasing supply voltage, ensuring dependable operation over a broad input range. Additionally, as the voltage increases, the power-delay product (PDP) steadily decreases, exhibiting exceptional energy efficiency.

These outcomes collectively validate the efficacy of VCO performance within stringent low-voltage constraints. The thesis goals of creating a low-power CMOS architecture based on locked-loop principles are directly aligned with the improvements in tuning range, energy efficiency, and phase stability that were attained. Therefore, the suggested design provides a scalable and technologically compatible foundation for upcoming high-speed, low-jitter, and energy-efficient mixed-signal integrated circuits, while also advancing the practical implementation of low-power PLL systems.

5 Conclusion

This paper examines the design process of a five-stage current-starved ring oscillator implemented in CMOS technology. At a central frequency of 14.5 GHz, the suggested current-starved voltage-controlled oscillator (VCO) exhibits effective operation with low power dissipation and little delay. Supply voltage, tuning range, power dissipation, maximum output power, and noise margin are important factors assessed during 1.6 GHz operation. When compared to previous designs, the suggested design achieves the shortest delay and much lower power dissipation, as shown in Table 1.

A significant advantage of the presented VCRO is its 23.5 % tuning range, achieved with variable supply

voltage and exhibiting excellent linearity across the control voltage range. A comprehensive parametric analysis conducted at various temperatures, control voltages, and process corners validates the robustness of the circuit. Simulation results confirm a delay of 869 μW, an RMS current of 17.2 mA, and noise margins of 0.27 V (high level) and –0.22 V (low level). The combination of wide tuning range, low power consumption, and stable frequency operation makes the proposed ring VCO highly suitable for Ku-band satellite communication and short- to mid-range RADAR applications.

References

1 Kirankumar H L, Rekha S & Laxminidhi T, *Circuits, Syst Signal Process*, 39 (2020) 3819.
2 Jyosthna I, Suman S & Bose R, *Int J Advanced Sci Technol*, 29 (2020) 7862.
3 Sharroush S M & Badry E, *Int J Circuit Theory Appl*, 51 (2023) 3480.
4 Arya R & Singh B K, *Comput Syst Sci Eng*, 46 (2023) 93.
5 Choudhary A & Mandilya R, *Int J Innovative Res Sci Eng Technol*, 7 (2018) 2035.
6 Arya R & Singh B K, *Phys Scr*, 100 (2025) 015040.
7 Anushkannan N K & Mangalam H, *Circuits Syst*, 7 (2016) 4169.
8 Muddi V, Shinde K D & Shivaprasad B K, *Int Conf Control Instrument Comm Comput Technol (ICCICCT*), *Kumaracoil,* (2015) 335.
9 Kazemi Z, Shalikar S, Buhari A M & Maleki S A M, *Int J Electr Electron Data Commun*, 3 (2015) 34.
10 Raj T H P, Selvakumar J & Praveen Kumar S, *Int J Eng Technol,* 7 (2018) 871.
11 Sandhiya S, Revathi R & Vinothkumar B, *Int Res J Eng Technol*, 5 (2018) 844.
12 Balikai V & Kittur H, *Circuit World*, 47 (2020) 71.
13 Sulaiman D R, *J Electr Syst*, 16 (2020) 332.
14 Maiti M, Majumder A, Chakrabartty S, Song H & Bhattacharyya B K, *Microelectron J*, 98 (2020) 1.
15 Agrawal A & Khatri R, *Int J Comput Appl*, 122 (2015) 26.
16 You S, Zhang C, Yuan F, Zhang Y & Zhang Y, *Photonics Electromagnet Res Symposium*, Xiamen, China, (2019) 2180-2185, doi: 10.1109/PIERS-Fall48861.2019.9021850.
17 Das K, Pradhan N, Kumar V & Jana S K, *Proc 3rd Int Symp Devices Circuits Syst*, (2020) 20.
18 Parashar V S, Dhanush T N, Bharadwaj D A & Premananda B S, *Wutan Huatan Jisuan Jishu*, 16 (2020) 195.
19 Shobha K M, Sudhakara H M, Praveen J & Rao A R, *Int J Innovative Res Electr Electron Instrument Control Eng,* 4 (2016) 398.
20 Kong L & Razavi B, *IEEE J Solid-State Circuits*, 51 (2016) 626.
21 Yao L I, Zhou B & Wang Z, *IEEE Access*, 9 (2021) 149807.
22 Deshmukh A A, Gamad R & Mishra D K, *IOSR J VLSI Signal Process*, 10 (2020) 32.
23 Castro M B, Souza R R N, Junior A M P, Lima E R & Manera L T, *Analog Integr Circuits Signal Process*, 109 (2021) 647.
24 Verma S, Singh S, Pal B B, Kumar M, Verma S D K & Nath V, *Ind J Sci Technol*, 9 (2016) 1.
25 Hathwalia S, *J Eng Res Appl*, 9 (2019) 52.
26 Badal M T I, Alam M J, Reaz M B I, Bhuiyan M A S, & Jahan N A, *J Eng Sci Technol*, 14 (2019) 1776.
27 Mestice M, Neri B, Ciarpi G & Saponara S, *Sensors*, 20 (2020) 1.
28 Marvast F T, Abouei J, Marvast M J T & Mehrizi P A, *IOP Conf Ser Mater Sci Eng*, 9 (2021) 33.
29 Belorkar U A & Ladhake S A, *Ind J Sci Technol*, 9 (2019) 1.
30 Saw S K, Ragavraju S K & Nath V, *Int J Appl Eng Res*, 10 (2015) 758.
31 Tu C C, Wang Y K & Lin T H, *IEEE J Solid-State Circuits*, 52 (2017) 2523.
32 Sajotra D, Dhariwal S & Mishra R S, *Ind J Sci Technol*, 9 (2016) 1.
33 Sharma G K, Johar A K, Kumar T B & Boolchandani D, *Analog Integr Circuits Signal Process*, 103 (2020) 17.
34 Yadav R, Dahiya P K & Mishra R, *Sadhana - Academy Proceed Eng Sci*, 45 (2020) 1.
35 Singh S, Jain S & Mishra O, *J Xi'an Shiyou University*, 18 (2020) 237.
36 Murakami S, Hayashi K, Arata S, Xu G, Bui C D, Kobayashi A & Niitsu K, *Sensors Mater*, 32 (2020) 2607.
37 Askari S, Saneei M & Salem S, *Radioelectron Comm Syst*, 62 (2019) 232.
38 Kabirpour S & Jalali M, *Integration*, 69 (2019) 1.
39 Dharani B & Nanda U, *Silicon*, 14 (2022) 6599.
40 Amin M & Leung B, *IEEE Trans Circuits Syst II,* 63 (2016) 433.
41 Ciarpi G, Monda D, Mestice M, Rossi D & Saponara S, *Electron*, 12 (2023) 1.
42 Singh B, Kumar S & Chauhan R K, Analog *Integr Circuits Signal Process,* 114 (2023) 31.
43 Madheswaran S & Panneerselvam R, *Int J Electrical Comput Eng*, 14 (2024) 1398.
44 Jin J, Zhou K Q & Zhao L, *IEEE Access*, 5 (2017) 5306.