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Reliability Investigation of Interfacial Defects in InGaAs-SOI-FinFET for High-Performance Applications

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This work investigates the reliability of interfacial defects in Indium Gallium Arsenide (InGaAs) SOI-FinFETs for high-performance applications. $In_{0.53}Ga_{0.47}As$ is a promising material for next-generation transistors due to its high electron mobility, which is essential for high-speed and high-frequency applications. However, the presence of interface trap charges (ITCs) can significantly impact device performance and reliability. We comprehensively analysed ITCs in InGaAs SOI-FinFETs, examining their effects on the linearity performance parameters such as VIP2, VIP3, IIP3, IMD3, HD2 and HD3. All the results indicate that optimizing the interface quality is crucial for enhancing the reliability and performance of InGaAs SOI-FinFETs. This work provides valuable insights into the defect mechanisms and offers guidelines for improving the fabrication processes to achieve more reliable high-performance InGaAs-SOI-FinFETs. Therefore, InGaAs-based FinFET is the most suitable high-performance semiconductor device for next-generation use. InGaAs, with its superior electron mobility and high saturation velocity, offer substantial benefits for high-frequency and high-speed applications, which make it a desirable substitute for silicon.

Keywords: InGaAs-SOI-FinFETs; Interface Trap Charges (ITCs); Reliability; Materials

1 Introduction

As the semiconductor industry continues pushing the limits of Moore's Law, searching for materials that offer superior performance and energy efficiency is paramount. Indium Gallium Arsenide (InGaAs) has emerged as a leading candidate for next-generation Fin Field-Effect Transistors (FinFETs) due to its excellent electron mobility and direct bandgap properties[1, 2]. These characteristics make InGaAs an ideal material for high-speed and low-power applications, which are crucial for advancing computing and communication technologies[3, 4]. InGaAs FinFETs offer several advantages over traditional silicon-based transistors. The high electron mobility of InGaAs enables faster switching speeds and higher drive currents, essential for improving integrated circuits' performance. Additionally, the direct bandgap of InGaAs allows for efficient electron transport, reducing power consumption and heat generation, which are critical factors in modern electronic devices. However, the integration of InGaAs into FinFET structures presents several challenges. The fabrication processes need to be precisely controlled to ensure high-quality interfaces and minimize defects. Interfacial defects, in particular, can significantly impact the performance and reliability of InGaAsFinFETs[5-7]. These defects can introduce trap states that degrade carrier mobility, increase leakage currents, and lead to threshold voltage instability[8-10].

The continuous scaling of semiconductor devices has pushed the boundaries of material engineering and device architecture, leading to the exploration of new materials and structures for improved performance[11, 12]. One such promising candidate is the InGaAs-SOI-FinFET[13]. This advanced device architecture combines the high electron mobility of indium gallium arsenide (InGaAs) with the benefits of SOI technology[14-21], offering significant potential for high-speed and low-power applications. However, the reliability of InGaAs-SOI-FinFETs remains a critical concern, particularly due to interfacial defects that can significantly impact device performance and longevity. Interfacial defects, such as traps at the semiconductor-oxide interface, can lead to increased leakage currents, threshold voltage shifts, and reduced carrier mobility, thereby degrading the overall device reliability[22-24].

This investigation focuses on understanding the nature and impact of interfacial defects in InGaAs-SOI-FinFET. By employing advanced characterisation techniques and simulation tools,

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we aim to identify the types of defects present, their origins, and their effects on device performance. Furthermore, strategies for mitigating these defects through material engineering and process optimization will be explored to enhance the reliability of InGaAs-SOI-FinFET for high-performance applications[25, 26]. The insights gained from this study will provide a deeper understanding of the interfacial defect mechanisms in InGaAs-SOI-FinFETs, paving the way for the development of more reliable and efficient semiconductor devices for future technologies.

2 Description of the Device Architecture and Simulation

Figure 1 depicts the device architecture. Fig. 1(a) and Fig. 1(b) show the 2D side and cross-sectional view perspectively at a channel/gate length (L_G) of 7 nm. The high-k gate oxide, HfO_2, is fixed on all three sides of the fin and has a thickness (t_{ox}) of 1 nm. The fin height/width ratio (H_{fin}/W_{fin}) of 2 is taken into consideration in the suggested structure since the fin height (H_{Fin})is 8 nm, and the fin width (W_{Fin}) is 4 nm. The concentration of doping in the source and drain regions is 10^{20} cm^{-3} (n-type), respectively, whereas the channel is doped with5×10^{16} cm^{-3} (p-type)[27]. All the parameters used in the proposed device are shown in Table 1. Conventional FinFET (C-FinFET) has silicon as a channel material, SiO_2 as an oxide material, and no buried oxide present.

ATLAS is a powerful 3D device simulator that is used to simulate the device[28]. Scientists and engineers frequently modify the simulation parameters to correspond with the properties of the apparatuses they utilise. We numerically resolve our device using the Lombardi model, often called the Constant Voltage and Temperature mobility model (CVT). This model takes into consideration the effects of ionised impurity scattering. The recombination effects of the device are analysed using the Shockley Read Hall (SRH) model, which simulates leakage current due to temperature variables. In addition, the Newton solution iteration employs the decoupling strategy, commonly referred to as Gummel's method [28]. The device temperature remained constant throughout the experiment at T = 300 K.

3. Results and Discussion

Figure 2 shows the impact of interface traps on I_{DS} vs. V_{GS} characteristics of C-FinFET and InGaAs-SOI-FinFET.The reliability of trap charges in the transfer characteristics is a critical factor in the performance and stability of various semiconductor devices, including transistors, sensors, and memory devices. Trap charges are defects or impurities that can capture and release charge carriers (electrons or holes) in the semiconductor material, influencing the device's electrical properties[29-32]. Intrinsic traps are inherent to the semiconductor material, arising from imperfections in the crystal lattice. Extrinsic traps are due to impurities or defects introduced during the fabrication process. Fig. 2(a & b) show the impact of ITCs at the InGaAs/HfO_2 interface on the transfer characteristics of C-FinFET and InGaAs-SOI-FinFET, respectively. When ITCs are present at the interface, the drain current does not change much in the InGaAs-SOI-FinFET. However, a change in drain

Table 1 — Devices Process Parameters

Parameter	InGaAs-SOI-FinFET
Gate Length (L_G)	7 nm
Source and Drain Length (L_S/L_D)	5 nm
Fin Height, (H_{FIN})	8 nm
Fin Width (W_{FIN})	4 nm
Oxide Thickness (t_{OX})	1 nm
Channel Doping	5.0×10^{16} cm^{-3}
Source and Drain Doping	1.0×10^{20} cm^{-3}
Channel Material	InGaAs
Oxide Material	HfO_2
Buried Oxide	Present
Interfacial Trap Charge Density	1.0×10^{12} cm^{-2}

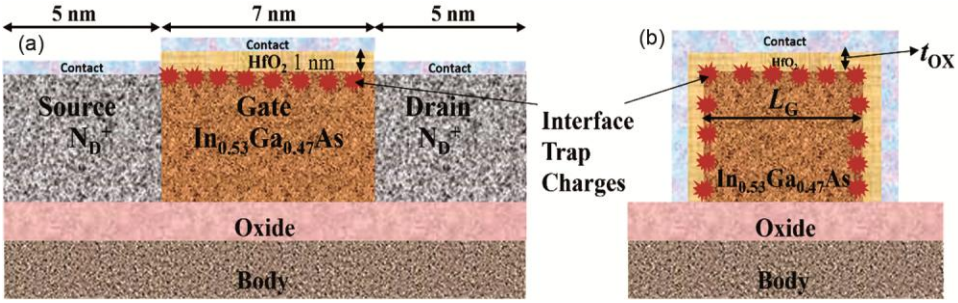

Fig. 1 — (a) 3D architecture and (b) Lateral view of InGaAs-SOI-FinFET

current is reflected for the C-FinFET. So, InGaAs-SOI-FinFET shows reliability over the trap charges present at the interface of InGaAs/HfO_2 due to the device's InGaAs architecture.

Figure 3(a & b) show the impact of interface traps on the transconductance (gm) of C-FinFET and InGaAs-SOI-FinFET, respectively. Interface traps have a substantial impact on the transconductance of C-FinFET due to their influence on carrier mobility and threshold voltage, as shown in Fig. 3(a). The sensitivity of InGaAs to interface defects exacerbates these effects, leading to less significant reductions in transconductance. Mitigating these impacts through improved materials, advanced fabrication techniques, and optimized device design is crucial for enhancing the performance of InGaAs-SOI-FinFET, as shown in Fig. 3(b)[33].

Figure 4(a) shows the impact of ITCs at the InGaAs/HfO_2 interface on the switching ratio of InGaAs-SOI-FinFET and C-FinFET. When ITCs are present at the interface, the on-current does not change much in the InGaAs-SOI-FinFET (as shown in Fig. 2(b), and a similar trend is observed for off-current. However, a change in on-current is reflected for the C-FinFET and impacted the device's performance. So, InGaAs-SOI-FinFET shows reliability over the trap charges present at the interface of InGaAs/HfO_2compared to C-FinFET. The impact of interface trap charges on the subthreshold swing (SS) of InGaAs-SOI-FinFETs is a crucial aspect of device performance. Subthreshold swing is a key parameter that characterizes the efficiency of a transistor in switching from the off state to the on state. Interface traps are defects located at the semiconductor-insulator interface that can trap and release charge carriers. These traps can be acceptor-like or donor-like, and they significantly affect the

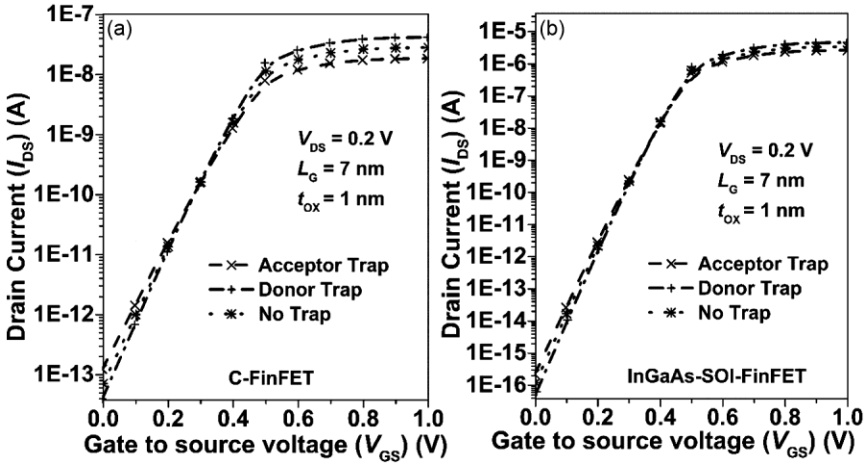

Fig. 2 — Influence of Interface traps on I_{DS} vs. V_{GS} characteristicsof (a) C-FinFET and (b) InGaAs-SOI-FinFET

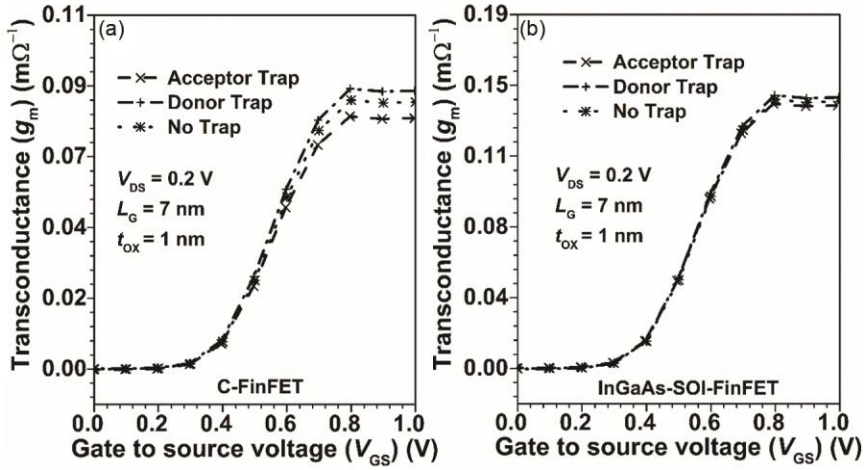

Fig. 3 — Influence of Interface Traps on g_m of (a) C-FinFET and (b) InGaAs-SOI-FinFET

device's electrical characteristics. Interface traps contribute to an increase in the subthreshold swing by introducing additional capacitance and increasing the number of states that need to be inverted. Fig. 4(b) reflects that InGaAs-SOI-FinFET shows more reliability over the trap charges present at the interface of InGaAs/HfO_2 compared to C-FinFET, where the Si/SiO_2 interface is considered. Therefore, it can be observed that interface trap charges do not impact the subthreshold swing in InGaAs-SOI-FinFET much as they do not increase leakage currents or capacitance and cause threshold voltage instability. Mitigating these impacts through advanced passivation techniques, optimized device design, and improved fabrication processes is essential for achieving better subthreshold performance in InGaAs-SOI-FinFETs.

Interface trap charges significantly impact the surface potential in C-FinFETs by modulating the electric field, causing potential fluctuations, and shifting the threshold voltage. These effects lead to degradation in mobility, increased subthreshold swing, and threshold voltage variability, as shown in Fig. 5(a). Fig. 5(a) reflects that InGaAs-SOI-FinFET shows more reliability over the trap charges present at the interface of InGaAs/HfO_2 compared to C-FinFET, where the Si/SiO_2 interface is considered. Therefore, it can be observed that interface trap charges do not impact the surface potential in InGaAs-SOI-FinFET. Further, the impact of trap charges is observed on the DIBL for C-FinFET and InGaAs-SOI-FinFET. Figure 5(b) shows the impact of ITCs at the InGaAs/HfO_2 interface on the DIBL of InGaAs-SOI-FinFET and C-FinFET. When ITCs are present at the interface, the DIBL does not have any impacton the InGaAs-SOI-FinFET. However, a major change in DIBL is reflected in the C-FinFET, which impacts the device's performance. So, InGaAs-SOI-FinFET shows

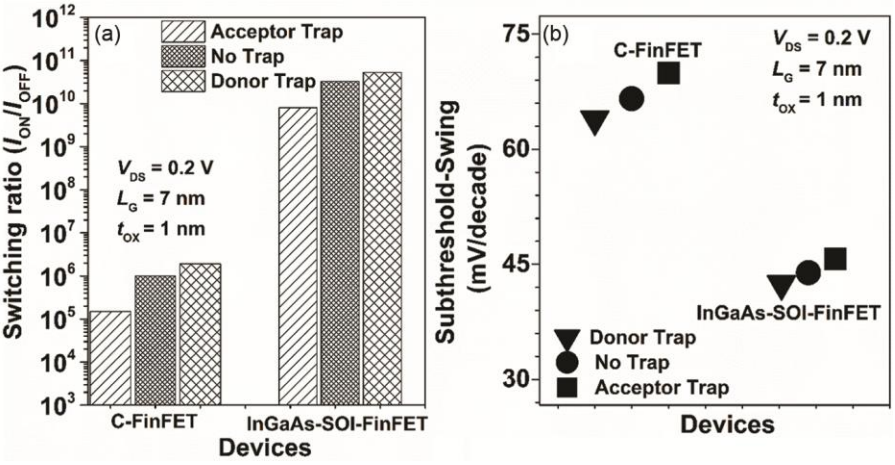

Fig. 4 — Influence of Interface Traps on (a) Switching ratio and (b) Subthreshold-swing of InGaAs-SOI-FinFET and C-FinFET

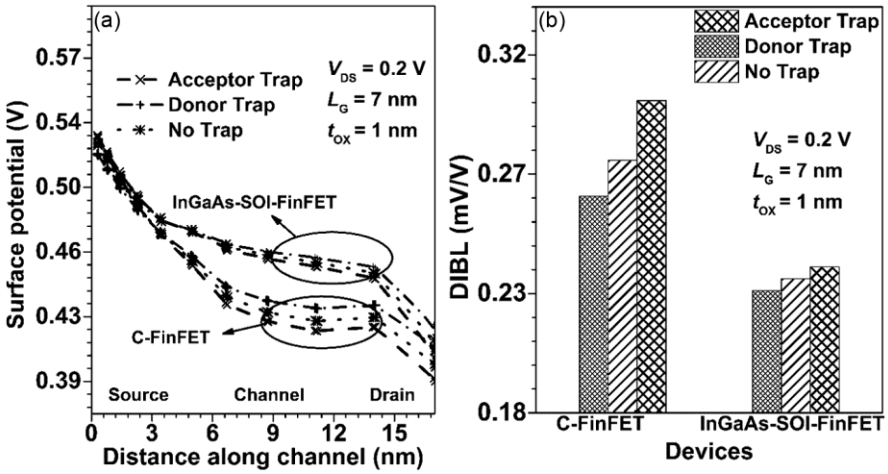

Fig. 5 — Influence of Interface Traps on (a) Surface potential (b) DIBL of InGaAs-SOI-FinFET and C-FinFET

reliability over the trap charges present at the interface of InGaAs/HfO_2 compared to the trap charges present at the interface of Si/SiO_2.

Figure 6(a) shows the impact of ITCs at the InGaAs/HfO_2 and Si/SiO_2 interfaces on the electric field of InGaAs-SOI-FinFET and C-FinFET, respectively. The impact of donor and acceptor trap charges is negligible on the drain and source sides. However, a very small effect is observed in the channel region. In the presence of donor trap charges, the electric field increases and reduces when acceptor trap charges are present as compared to the absence of trap charges due to a change in electron velocity. Hence, InGaAs-SOI-FinFET shows reliability over the trap charges. Electron mobility is evaluated when ITCs are present to show the device's reliability over trap charges. Fig. 6(b) shows the impact of donor, acceptor and no trap charges at the InGaAs/HfO_2 and Si/SiO_2 interfaces on the electric field of InGaAs-SOI-FinFET and C-FinFET, respectively. The impact of ITCs on electron mobility is negligible at the drain and source side. However, a very small effect is observed in the channel region. When donor ITCs are present, electron mobility increases and reduces when acceptor ITCs are present. Hence, InGaAs-SOI-FinFET shows reliability on electron mobility over the trap charges.

Further, the impact of traps on the higher order of transconductances has been observed to show the device and material reliability. Fig. 7(a & b) reflect the g_{m2} and $g_{m3,}$ respectively, for InGaAs-SOI-FinFET, and C-FinFET and calculated by using Eq. (1) [34] in the presence of donor and acceptor trap charges. Fig. 7(a & b) show that these higher-order transconductances are not impacted due to better control over short-channel effects in the InGaAs-SOI-FinFET structure compared to C-FinFET. The three-dimensional fin structure helps to mitigate issues like

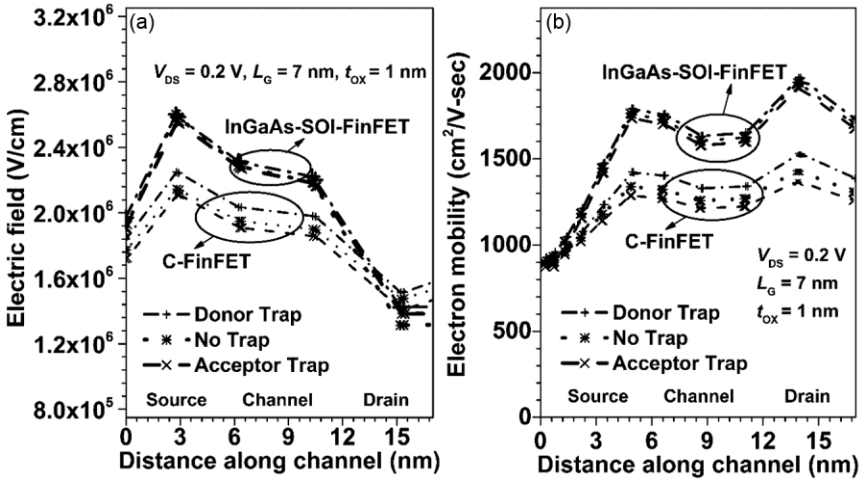

Fig. 6 — Influence of Interface Traps on (a) Electric field and (b) Electron mobility of InGaAs-SOI-FinFET and C-FinFET

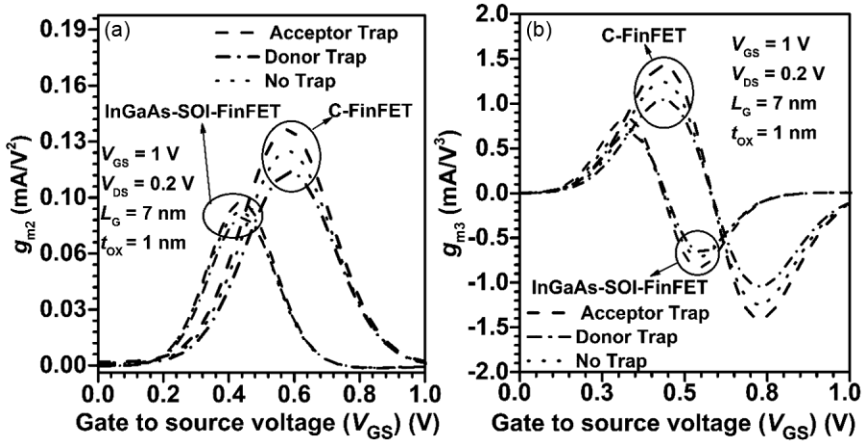

Fig. 7 — Influence of Interface Traps on (a) g_{m2}, and (b) g_{m3}; of InGaAs-SOI-FinFET and C-FinFET

drain-induced barrier lowering (DIBL) and subthreshold swing degradation, which can degrade transconductance in C-FinFET. InGaAs material and structure improve carrier mobility, and transport characteristics improve the higher-ordertrans conductance reliability over the trap charges. High-k (HfO_2) dielectrics with low interface trap densities are commonly employed to achieve better gate control and, consequently, higher transconductance. Hence, InGaAs-SOI-FinFET shows reliability on higher-order transconductances over the trap charges.

$$g_{mn} = \frac{1}{n!}\frac{\delta^n I_{DS}}{\delta V_{GS}^n}, \text{where } n = 1, 2, 3 \quad \text{... (1)}$$

The reliability of ITCs over VIP2 and VIP3 in FinFETs is critical for enhancing the performance of RF and linearity applications. Fig. 8(a & b) show the VIP2 and VIP3 for InGaAs-SOI-FinFET and compared with C-FinFET in the presence of interfacial trap defects. VIP2 and VIP3 are calculated by using Eq. (2) and (3)[35]. VIP2 and VIP3 are more reliable over ITCs in InGaAs-SOI-FinFET due to advanced gate dielectric materials with high-k (HfO_2) and low interface trap densities, which can improve gate control and reduce gate leakage, leading to better VIP2 and VIP3 figures of merit. Fig. 8(a & b) show the impact of donor, acceptor and no trap charges at the InGaAs/HfO_2 and Si/SiO_2 interfaces on VIP2 and VIP3 of InGaAs-SOI-FinFET and C-FinFET respectively. When donor ITCs are present, VIP2 and VIP3 reduce and increase when acceptor ITCs are present. Hence, InGaAs-SOI-FinFET shows reliability on electron mobility over the trap charges.

$$VIP2 = 4 \times g_{m1}/g_{m2} \quad \text{... (2)}$$

$$VIP3 = \sqrt{24 \times g_{m1}/g_{m3}} \quad \text{... (3)}$$

IIP3 (third-order input intercept point) and IMD3 (third-order intermodulation distortion)are evaluated using Eq. (4) and (5) [36] and plotted w.r.t gate voltage for InGaAs-SOI-FinFET and C-FinFET to show the reliability over trap charges, as shown in Fig. 9(a & b), respectively. Fig. 9(a) reflects that InGaAs-SOI-FinFET shows more reliability over the trap charges present at the interface of InGaAs/HfO_2 compared to C-FinFET, where the Si/SiO_2 interface is considered. Fig. 9(b) shows that InGaAs-SOI-FinFET inherently exhibits reduced distortion compared to C-FinFET due to reduced short-channel effects and improved gate control. This inherent linearity contributes to improved IIP3 and IMD3 performance.

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \quad \text{... (4)}$$

$$IMD3 = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right)^2 \times R_S \quad \text{... (5)}$$

Further, to evaluate the distortion, HD2 (Second Harmonic Distortion) and HD3 (Third Harmonic Distortion) are calculated using Eq. (6) and (7) [15, 18, 36] for InGaAs-SOI-FinFET and C-FinFET to show the reliability of the device and material over the ITCs present at the interface of InGaAs/HfO_2 and Si/SiO_2 interfaces as shown in Fig. 10(a & b). Fig. 10(a & b) reflect that InGaAs-SOI-FinFET shows more reliability over the trap charges present at the

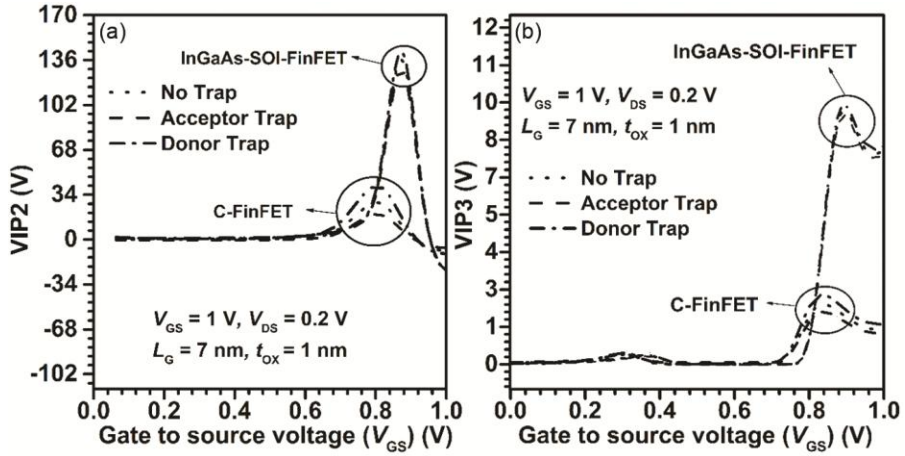

Fig. 8 — Influence of Interface Traps on (a) VIP2, and (b) VIP3; of InGaAs-SOI-FinFET and C-FinFET

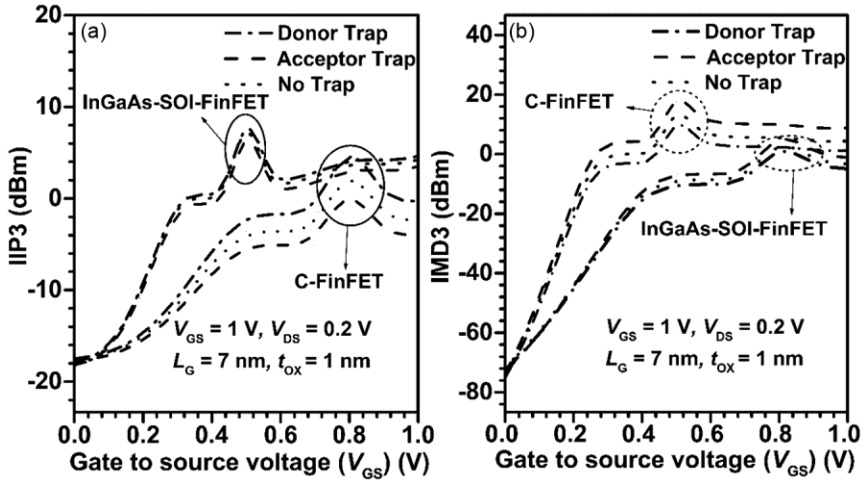

Fig. 9 — Influence of Interface Traps on (a) IIP3 and (b) IMD3; of InGaAs-SOI-FinFET and C-FinFET

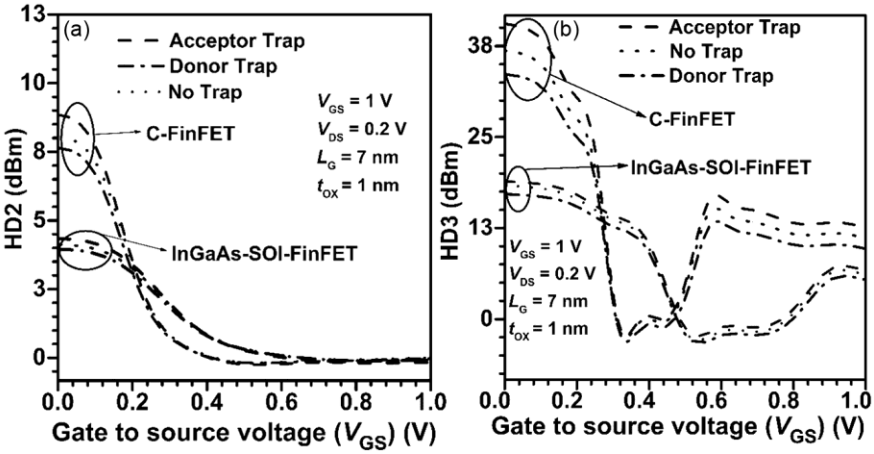

Fig. 10 — Impact of Interface Traps on (a) HD2, and (b) HD3; of InGaAs-SOI-FinFET and C-FinFET

interface of InGaAs/HfO_2 compared to C-FinFET, where the Si/SiO_2 interface is considered. Fig. 9(a & b) also reflect that InGaAs-SOI-FinFET inherently exhibits reduced harmonic distortion compared to C-FinFET due to improvement in transconductance and improved gate control. This inherent linearity contributes to improved HD2 and HD3 performance.

$$HD2 = 0.5V_a \frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \quad \text{... (6)}$$

$$HD3 = 0.25V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV^2{}_{GT}}\right)}{6g_{m1}} \quad \text{... (7)}$$

4 Conclusion

The reliability investigation of interfacial defects in InGaAs-SOI-FinFETs, assessed through critical linearity parameters such as VIP2, VIP3, IIP3, IMD3, HD2, and HD3, provides significant insights into the challenges and potential of this promising semiconductor technology. Harmonic distortion results (HD2, HD3 and IMD3) indicate that in the presence of interfacial defects, harmonic distortion is not much impacted as compared to C-FinFET and distortion is reduced by approximately 50% in the proposed device. It has also been observed that these interface defects adversely affect the VIP2 and VIP3, highlighting the need for improved interface quality to maintain high performance in high-frequency and analogue applications. Specifically, the IIP3 is significantly impacted, underscoring the necessity for precise control over fabrication processes to minimize defect densities.Moreover, our investigation reveals that targeted material engineering and process optimization can effectively mitigate the adverse effects of these interfacial defects. By employing

advanced techniques and refining the semiconductor-oxide interface, we can enhance the linearity and reliability of InGaAs-SOI-FinFETs. These improvements are crucial for achieving the high performance required for next-generation electronic devices.This work underscores the importance of addressing interfacial defects in InGaAs-SOI-FinFETs to ensure their viability for high-performance applications. By focusing on enhancing the linearity parameters, we can significantly improve the reliability and efficiency of these devices.

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