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A New Multiplier-less Memristor Emulator for Analog and Digital Applications

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Acharge controlled memristor circuit using the most adaptable analogue block called Current Backward Transconductance Amplifier (CBTA) and Operational Transconductance Amplifier (OTA) along with few passive elements is introduced. It uses only one CBTA, one OTA, three resistors and one capacitor for emulating grounded memristor. The proposed memristor emulator is simulated in Cadence Virtuoso tool using standard CMOS $90nm$ technology including post-layout simulation of CBTA and OTA silicon components. All the CMOS transistors operating with the ±1.2 V DC supply voltage. Moreover, this paper demonstrates the proposed memristor use in the analog and digital domains. Furthermore, off-the-shelf components (IC AD844AN and CA3080EZ) and passive components are used in an experimental setup to verify the proposed circuit.

Keywords: MOSFET, Grounded, Memristor, Hysteresis loop, Analog and digital circuit

1 Introduction

The fourth passive circuit component, the memristor, has drawn interest because of its capacity to store data and processes. The memristor is essentially a two-terminal device whose resistance value is based on the amount of current that previously passed through it[1–9]. The specific relationship that a memristor has between the time integrals of its voltage (flux) and current (charge) depends on the polarity and amplitude of the voltages that are applied across it. The initial research by Chua[1] was followed at the HP laboratories to build the memristor utilizing titanium oxide (TiO2). Here, the semiconductor layer divides into two separate resistive zones, denoted, respectively, as low resistance $(R_{on})$and higher resistance (R_{off})[4]. An external voltage may be used to shift the boundary between these two resistive zones. However, the memristor created by HP labs is not available on the commercial market at this time because of its high cost and intricate manufacturing process. This encourages researchers to investigate additional memristor design development for practical uses.

The memristorability to store data makes it useful in both analog and digital applications[10–16]. Examples of these include non-volatile memories[10], programmable analogue circuits[11], neuromorphic circuits[12], adaptive filters[13], chaotic circuits[14], and many more. Thus, designers have drawn memristor emulators in order to expand the possibilities in many digital[15] and analog[16] applications.

The memristor can be classified as either a grounded type[17–22] or a floating type[23–36] based on its uses and applications documented in the literature. In case of grounded type memristor, one terminal will be exposed to the input voltage while the other terminal will be grounded and the memristance state depends upon the input voltage with ground reference. Such memristors are used in chaotic circuits, filter circuits and amplifier circuits. Also, the majority of grounded type memristors studied so far[17–22] use a single active element[18–22], while one design uses four MOS transistors[17]. Nevertheless, the MOS capacitor used in the memristor circuit[18] restricts the circuit at lower frequency ranges since parasitic effects are only noticeable at higher frequencies. Moreover, many memristor circuit analyses are performed using only simulations[20-21]. On the other hand, the analysis of floating type memristors[23–36] uses several active components[23,25–28,30-33], with the exception of Refs[24,29,34-36]. Therefore, using additional hardware required more integrated circuit (IC) space. Additionally, the multiplier used in the memristor circuits[21, 27–28,31-33] raises the circuit's complexity and nonlinearity at the output. Nevertheless, the use of analog multipliers in emulator circuits results in a higher number of active components, making the

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circuit bulkier or larger on the chip and wasting a significant amount of power[37, 38]. In addition, several memristor circuits have only shown simulation results[17,20–21,23–24,31,33], but performing experimentation by using commercially available ICs increases the likelihood of actual IC implementation.

Further, a detailed comparison of the proposed memristor emulator circuit with other memristor circuits that have been reported in the literature is given in Table III. In Table III, many memristor circuits with different parameters are compared. These circuits continue to suffer from one or more of the following issues: (i) Required MOS capacitor[18]. (ii) Utilised an extra block in their circuit design known as a multiplier[21, 27-28,31–33]. (iii) lacking electrical tunability[17,20,27-33]. (iv) only either incremental type[25,27,33] or decremental type[29] simulation. (v) There is no experimental validation for the memristor circuits[17,20–21,23–24,31,33]. (vi) Comparatively high power consumption[19,31,34]. (vii) Comparatively large layout area[18,20,24,26,29-30,35-36].

The aim of this article is to design a charge-controlled memristor by means of a well-known analog active block called as current backward trans conductance amplifier (CBTA) and a single operational trans conductance amplifier (OTA**)**. With just one CBTA, one OTA, three resistors, and one capacitor, the suggested memristor emulator circuit is highly appealing for integrated circuit design. First, the mathematical equations for the memristor were established for both the ideal and non-ideal cases and then the circuit was simulated along with post layout simulation of silicon components CBTA and OTA using the Cadence Virtuoso tool with standard CMOS 90 nm technology. As anticipated, the simulation results of the pinched hysteresis curve across broad frequency ranges, from 100 Hz to 7 kHz, are achieved. Additionally, the pinched hysteresis curve is obtained for a range of capacitor values and temperature fluctuations between -40^{0}C to 120^{0}C. Likewise, the feasibility of the suggested memristor emulator has been validated in several process corners (FF, SS, FS, and SF) taking into account abrupt temperature fluctuations (-40^{0}C to 120^{0}C). Furthermore, by applying pulse input with appropriate values of amplitude, period, and pulse width, the suggested memristor non-volatility is confirmed. In addition, a simple Op-Amp based Schmitt trigger circuit and CMOS NAND logic circuit is implemented using the proposed memristor as an application. Also, a practical realization is also confirmed through the creation of an experimental setup with threeAD844AN and two CA3080EZ, five resistors and one capacitor. This setup validates the hysteresis curve and circuit workability at different operating frequencies and capacitance values as reported in the simulations. It is evident that the proposed memristor circuit, which is adequate for the integration of commercial ICs, as it is consistent with theoretical, simulations, and experimental findings.

2 General Model of Memristor

The discovery of memory elements has led researchers to focus on electrical components other than resistors, inductors and capacitors. Biolek and colleagues[9] proposed two concepts, rho (ρ) and charge (q), as seen in Fig. 1. The connection between charge and magnetic flux serves as the foundation for the fourth fundamental element, known as memristor (M).

The memristor, often referred to as a memory resistor, is a passive two-terminal element that has a unique nonlinear behavior not seen in other two-terminal components like resistors, inductors, and capacitors. In 1971, Professor Leon Chua first proposed the idea of a memristor[1], showing that the features of a memristor (M) could not be replicated by any combination of the well-known two-terminal passive components $(R, L,$ and $C)$.Furthermore, as indicated by the given Eq. (1), the memristor is the only two-terminal element capable of demonstrating the missing connection between electrical charge and flux.

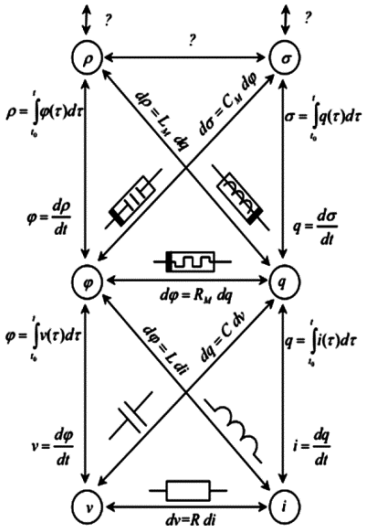

Fig. 1 — Relationship between memory and non-memory elements[9]

$$M = \frac{d\varphi}{dq} \quad \ldots (1)$$

There are two different types of memristors based on the characteristics of charge and flux: charge-dependent or current-controlled memristors, which relate to a single-valued function of charge, and flux-dependent or voltage-controlled memristors, which relate to a single-valued function of flux. The voltage equation of a charge-controlled memristor as shown in Eq. (2 (a) & 2 (b)):

$$v(t) = M(q(t))i(t) \quad \ldots (2\ (a))$$

$$M(q) = \frac{d\varphi(q)}{dq} \quad \ldots (2\ (b))$$

Similarly, the current equation of a flux-controlled memristoras shownin Eq. (3 (a) & 3 (b)):

$$i(t) = W(\varphi(t))v(t) \quad \ldots (3\ (a))$$

$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} \quad \ldots (3\ (b))$$

where, $M\ (q)$ and $W\ (\varphi)$ are the memristance and memductance with units of resistance and conductance, respectively.

Additionally, the universal relations of a current-controlled memristive system and a voltage-controlled memristive system are demonstrated by Eq. (4 (a) & 4 (b)) and (5 (a) & b (b)), respectively.

$$v(t) = R(x, i(t), t)\ i(t) \quad \ldots (4\ (a))$$

$$\frac{dx}{dt} = f(x, i(t), t) \quad \ldots (4\ (b))$$

$$i(t) = G(x, v(t), t)\ v(t) \quad \ldots (5\ (a))$$

$$\frac{dx}{dt} = f(x, v(t), t) \quad \ldots (5\ (b))$$

where $v(t)$ stands for the input voltage and $i(t)$ for the input current. Here, the state variable is represented by variable x, while the functions f, R, and G are explicit functions of time. It's also important to remember that most memristiveor nonvolatile memory devices in recent years have been simulated using the aforementioned equations.

3 Description of Proposed Memristor Emulator

The proposed memristor model is build using an analog active block known as Current Backward Transconductance Amplifier (CBTA)[39] and an Operational Transconductance Amplifier (OTA)[40] in order to get the equation for the charge-controlled memristor element. Subcircuit properties and proposed memristoremulator explained as follows:

3.1 CBTA

The CBTA has demonstrated its use in several current-mode and voltage-mode analog signal processing applications, including oscillators, immittance function simulators, and voltage- and current-mode filters[39,41–48]. The circuit symbol of the proposed active element, CBTA, is shown in Fig. 2(a). In this instance, the CBTA's input terminals are $p$and n, while its output terminals are w and z. The CBTAhasp, n, and z terminals which are high impedance;however, the w terminal is low impedance.The following is the definition of the CBTAideal terminal voltage-current equations:

$$I_z = g_m(V_p - V_n),\ V_w = V_z,\ I_p = I_w, I_n = -I_w \quad \ldots (6)$$

where g_m is the CBTA transconductance gain. As per the terminal equations mentioned above, the current flowing through the z terminal is determined by multiplying the transconductance g_m by the difference in voltages at p and $n$terminals. Thus, the CBTA's z terminal is referred to as the current output. The CBTA'sp and n terminals are referred to as the noninverting (positive) and inverting (negative) inputs, respectively. The voltage at the w terminal is the same as the voltage at the z terminal.

The CMOS implementation of the CBTA [Fig. 2(b)], comprises of portions for current conveyor[49] and Operational Transconductance Amplifier[50]. It is achieved by connecting proper outputs of these sections and modifying the dimension of CMOS transistors. Also, Table I provides information about the MOS transistors' aspect ratio that were utilized in the CBTA implementation[21]. Transistors M1–M15 create a current conveyor, whereas transistors M16–M23 are utilized to realize a transconductance stage [Fig. 2(b)]. To further aid in biasing, transistors M1 and M9 as well as the current source I_{REF} are used. Furthermore, [Fig. 2 (c)] shows the device's layout, which was made with the Virtuoso Layout Suite tool. The layout's total area, after the DRC and LVS tests, is $280.502\mu m^2$.

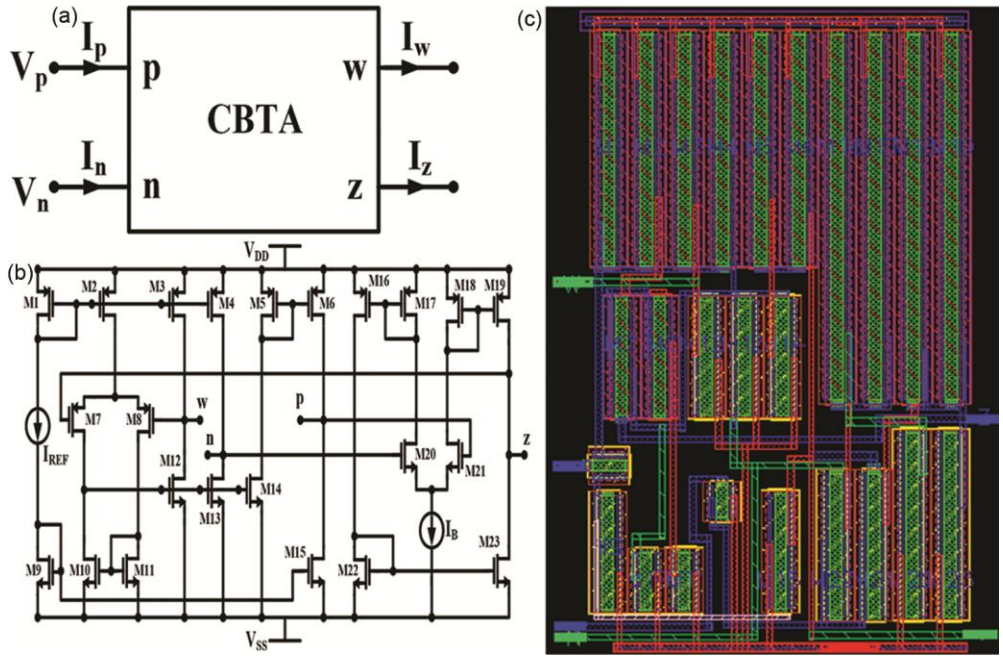

Fig. 2 — (a) Symbol of the CBTA element, (b) CMOS implementation for the CBTA[39], (c) Layout($20.18\mu m * 13.9\mu m$)

Table 1 — Transistor's aspect ratio of CBTA

PMOS Transistor's	W (μm)	L(μm)
M1-M6	7.2	0.36
M7-M8	3.6	0.36
M16-M19	11.52	0.36
NMOS Transistor's	W (μm)	L(μm)
M9, M12-M15	3.6	0.36
M10-M11	1.8	0.36
M20-M21	4.5	0.36
M22-M23	5.76	0.36

3.2 OTA

The Operational Transconductance Amplifier (OTA) is another active component used as tunable active element. Figure 3 (a- c) depicted the circuit symbol, MOS-based realization and layout diagram of OTA. In the OTA, the output (O) port receives a current equivalent to the differential input voltage ($V_P - V_N$)as a function of transconductance($\pm gm$). The following equations can be used to define OTA properties:

$$I_P = 0, I_N = 0, I_O = g_m(V_P - V_N) \quad \ldots (7)$$

The CMOS model of OTA is shown in [Fig. 3 (b)][40, 50] which consists of 11 transistors whose type and W, L descriptions are mentioned in Table 2. Furthermore, the device's layout, created using the Virtuoso Layout suite tool, is displayed in [Fig. 3 (c)]. Following the verification of DRC and LVS, the layout's total area is determined to be $303.43\mu m^2$.

4 Proposed Memristor Emulator

The proposedmemristor emulator configurations are shown in [Fig. 4 (a)]. Itemploys, one CBTA, one OTA, one capacitor and three resistors. From the figure, the voltage value at z terminal is the output of the OTA. The initial resistance R_S is connected to w terminal of the CBTA.Additionally, the Virtuoso Layout suite tool was used to build the device's silicon component layout, which is shown in Fig. 4(b). The layout of one-CBTA and one-OTA has been drawn after DRC and LVS check and the its layout area is found $719.404\mu m^2$.

As seen in Fig. 4(a), the input current of the memristor emulator is as follows:

$$I_{in} = \frac{(V_{in} - V_w)}{R_S} \quad \ldots (8)$$

Further, the equation of the V_{in} can be defined as:

$$V_{in} = I_{in} R_S + V_w \quad \ldots (9)$$

The output voltage (V_{R_2}) at the terminal of O is given by

$$V_{R_2} = V_z = V_w = g_m (V_P - V_N) R_2 \quad \ldots (10)$$

where g_m is the transconductance gain of the OTA and it can be defined as $g_m = k(V_B - V_t - V_{ss})$. Where $k = \mu_n C_{ox} \frac{W}{L} = k_n' (\frac{W}{L})$ is commonly stated as transconductance parameter of the MOSFET, the

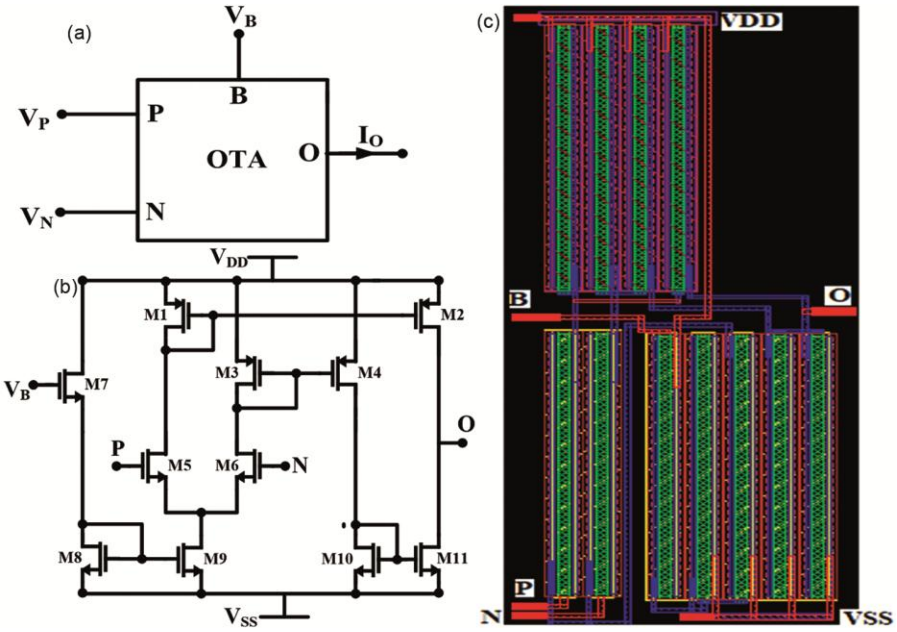

Fig. 3 — OTA structure (a) Symbol for a designed circuit (b) Designed circuit using MOS transistor's[40] (c) Layout ($28.2\mu m * 10.76\mu m$)

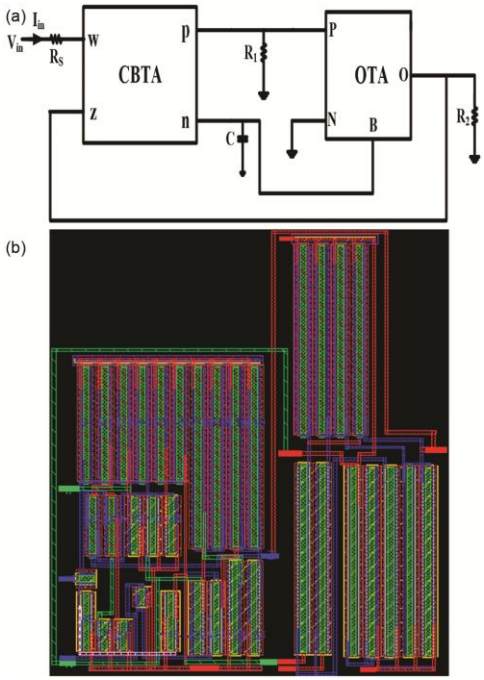

Fig. 4 — (a) Proposed memristoremulator circuits, and (b) Layout of Silicon components ($28.48\mu m * 25.26\mu m$)

first parameter $k_n^{'} = \mu_n C_{ox}$, is determined by the material manufacturing process and is often expressed as the process transconductance which is the function of mobility (μ_n) *and* gate-oxide capacitance (C_{ox}). For the purpose of obtaining the necessary resistance, it is easiest to select the second parameter, (W/L), also known as aspect ratio.

Table 2 — Transistor's aspect ratio of OTA

Transistor's	Type	W (μm)	L(μm)
M1-M4	PMOS	12	0.36
M5-M11	NMOS	12	0.36

Therefore, substituting the Eq. (10) in Eq. (9) would result the following equation as:

$$V_{in} = I_{in}R_S + g_m (V_P - V_N)R_2 \quad \ldots (11)$$

$$= I_{in}R_S + k(V_B - V_t - V_{ss})V_P R_2$$

$$= I_{in}R_S + k(V_C - V_t - V_{ss})V_P R_2$$

$$V_{in} = I_{in}R_S + k\left(\frac{-q(t)}{C} - V_t - V_{ss}\right)I_{in}R_1R_2$$

$$M(q(t)) = \frac{V_{in}}{I_{in}} = [R_S - kR_1R_2(V_t + V_{SS}) - \frac{kR_1R_2}{C}q(t)$$

$$M(q(t)) = \beta + \alpha q(t) \quad \ldots (12)$$

The Eq. (12) is satisfying the equation of charge controlled memristor, where α and β are defined as follows:

$$\alpha = -\frac{kR_1R_2}{C}, \beta = [R_S - kR_1R_2(V_t + V_{SS})$$

5 Effects of Non-Idealities and Parasitic Components

The following describes how non-idealities and parasitic elements affect the proposed memristor circuit.

5.1 Non-ideal Analysis

Considering the non-idealities of the CBTA[21], the terminal Eq. (6) mentioned above may be reformulated as follows:

$$I_z = \gamma_1 g_m(V_p - V_n),\ V_w = \alpha V_z,\ I_p = \beta_1 I_w, I_n = -\beta_2 I_w \quad \ldots (13)$$

Similarly, for an OTA the Eq. (7) can be rewritten as:

$$I_P = 0, I_N = 0, I_O = \gamma_2 g_m (V_P - V_N) \quad \ldots (14)$$

where α is non-unity voltage gain, β_1 and β_2 are non-unity current gain and γ_1 andγ_2 are non-unity trans conductance gain. After analysis, the amended equations for the proposed memristor emulator circuit are as follows:

The voltage at resistor $R_2$is given by:

$$V_{R_2} = V_z = \gamma_2 g_m\ (V_P - V_N) R_2 \quad \ldots (15)$$

Also, the voltage at w terminal is given by:

$$V_w = \alpha V_z = \alpha\gamma_2 g_m\ (V_P - V_N) R_2 \quad \ldots (16)$$

Therefore, substituting the Eq. (16) in Eq. (9) would result the following equation as:

$$V_{in} = I_{in} R_S + \alpha\gamma_2 g_m\ (V_P - V_N) R_2 \quad \ldots (17)$$

$$= I_{in} R_S + \alpha\gamma_2 k (V_B - V_t - V_{ss}) V_P R_2$$

$$= I_{in} R_S + \alpha\gamma_2 k (V_C - V_t - V_{ss}) V_P R_2$$

$$V_{in} = I_{in} R_S + \alpha\beta_1\gamma_2 k \left(\frac{-q(t)}{C} - V_t - V_{ss}\right) I_{in} R_1 R_2$$

$$M(q(t)) = \frac{V_{in}}{I_{in}} = [R_S - \alpha\beta_1\gamma_2 k R_1 R_2 (V_t + V_{SS}) - \frac{\alpha\beta_1\gamma_2 k R_1 R_2}{C} q(t) \quad \ldots (18)$$

According to Eqs. 13–18, these non-ideal errors might not have a significant effect on the memristor emulator's hysteresis or non-volatile properties. However, by operating the circuit within the proper frequency range, this little change may be minimised to its lowest possible value.

5.2 Parasitic Analysis

This section investigates the effects of CBTA and OTA parasitic on the performance of the proposed memristor that is being given. Due to the existence of several parasitic ports in the form of parasitic capacitors and resistors, [Fig. 4 (a)] circuit has been altered to resemble Fig. 5. In Fig. 5 the external resistances $R_1, R_2$and parasitic resistances R_{Pi} $(i = 1, 2, 3)$ are represented in terms of admittances as $G_1, G_2$and G_{Pi} $(i = 1, 2, 3)$, respectively, (where $G_i = 1/R_i, G_{Pi} = 1/R_{Pi}$). In Fig. 5, the parasitic can be seen as a parallel combination of resistors and capacitors at combined ports (p, P) as $C_{P1}||G_{P1}$, at combined port (n, B) as $C_{P2}||G_{P2}$,, at combined ports (O, z) as $C_{P3}||G_{P3}$and as a series parasitic at port w of CBTA as R_P. Parasitic capacitances (C_{Pi}) have a practical value within the range of fraction of picofarads, whereas parasitic admittances are reported to be in the range of tens of micromho. In light of this, min (C) >> (C_{P1}, C_{P2}, C_{P3}) and min (G_1, G_2) >> (G_{P1}, G_{P2}, G_{P3})[51]. Upon revisiting the circuit depicted in Fig. 5, the subsequent revised equation was generated to investigate the effects of diverse parasitic impedances on the operation of the proposed memristor circuit:

As seen in Fig. 5, the input current of the memristor is given by:

$$I_{in} = \frac{(V_{in} - V_w)}{R_{eq}} \quad \ldots (19)$$

where $R_{eq} = R_S + R_P$, then

$$V_{in} = I_{in} R_{eq} + V_w \quad \ldots (20)$$

The output voltage at the terminal of w is given by:

$$V_w = \frac{g_m V_P}{G_2 + SC_{P3}} \quad \ldots (21)$$

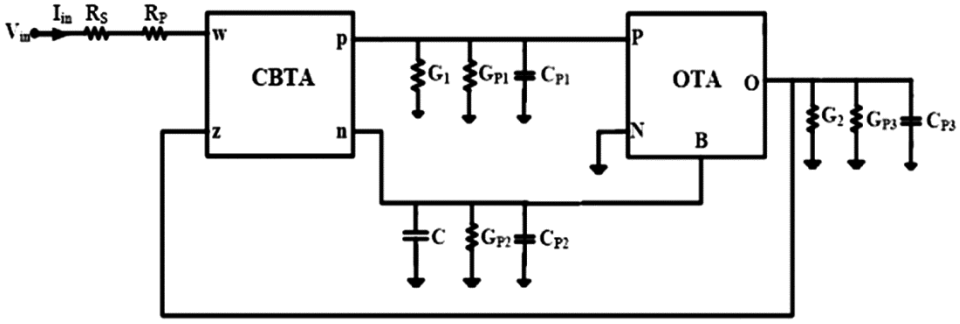

Fig. 5 — Proposed memristor emulator circuit in the presence of various port parasitic components

Substituting the Eq. (21) in Eq. (20) would result the following equation as:

$$V_{in} = I_{in}R_{eq} + \frac{g_m V_P}{(G_2 + SC_{P3})}$$

$$= I_{in}R_{eq} + \frac{g_m}{(G_2+SC_{P3})(G_1+SC_{P1})} I_{in}$$

$$V_{in} = I_{in}R_{eq} - \frac{k(\frac{I_{in}}{(G_{P2}+SC)} + V_t + V_{ss})}{(G_1 + SC_{P1})(G_2 + SC_{P3})} I_{in} \quad \ldots (22)$$

Here, $(\frac{G_{P2}}{C}) << \omega << (\frac{G_1}{C_{P1}}, \frac{G_2}{C_{P3}})$ and also $R_P << R_S$, then the above equation approximated as:

$$V_{in} = I_{in}R_S - k(\frac{q(t)}{C} + V_t + V_{ss})I_{in}R_1R_2$$

$$M(q(t)) = \frac{V_{in}}{I_{in}} = [R_S - kR_1R_2(V_t + V_{SS})] - \frac{kR_1R_2}{C} q(t) \quad \ldots (23)$$

As a result, from Eq. (23), the memristor value may differ from the optimal value. At low frequencies, its impact is minimal. Parasitic will influence the memristance value at higher frequencies.

6 Simulation and Experimental Results

To validate the theoretical interpretations, simulation and experimental research are conducted. Initially, Cadence Virtuoso Tool is used to simulate the proposed grounded memristor emulator circuit utilizing GPDK 90nm technology. For this, the supply voltages are used as $V_{DD} = -V_{SS} = 1.2V$. Additionally, the passive components such as external resistors values $R_S = 900\Omega, R_1 = 3k\Omega, R_2 = 1k\Omega$ and capacitor $C = 90nF$ are selected. Moreover, for CBTA the values of current sources are $I_{REF} = I_B = 100\mu A$ used. The proposed memristor circuit has a total power consumption of $2.76mW$.Further, simulations for transient analysis and the associated hysteresis curve, hysteresis analysis at different frequencies, hysteresis at temperature variations, hysteresis at capacitance value variations, process corner effects on hysteresis at different temperatures, non-volatility tests, and circuit application in analogue and digital domains are covered. Lastly, an experimental setup is built using readily available components, and the outcomes are monitored, in order to demonstrate the validity of the simulations.

6.1 Transient and Corresponding Hysteresis Analysis

A voltage-current waveform and a pinched hysteresis curve are shown in the simulation results for both pre-layout and post-layout shown in [Fig. 6 (a&b)] for the given sinusoidal input of voltage $300\,mV$ peak to peak and frequency $500\,Hz$. The comparison analysis reveals that there are not many parasitic effects, since the post-layout simulation results nearly match the pre-layout simulation results.

6.2 Hysteresis Curve at Various Frequencies

By adjusting the frequencies between $100Hz$and $7kHz$, the proposed memristor circuit is simulated. As seen in Fig. 7, the pinched hysteresis curves at various frequencies, including $300\,Hz$, $600\,Hz$, $900\,Hz$, $1.5\,kHz$, $2\,kHz$, and $3\,kHz$, are simulated, which clearly indicate that the lobe size of the pinched hysteresis curve diminishes with increasing frequency and at frequencies over $7\,kHz$, the proposed memristor functions as a linear resistor. As a result, the proposed memristor can function throughout a large frequency range.

6.3 Hysteresis Curve at Various Capacitance Values

The proposed memristor's operational range can also be tested by varying the capacitor that connects the n terminal of the CBTA with the B terminal of the

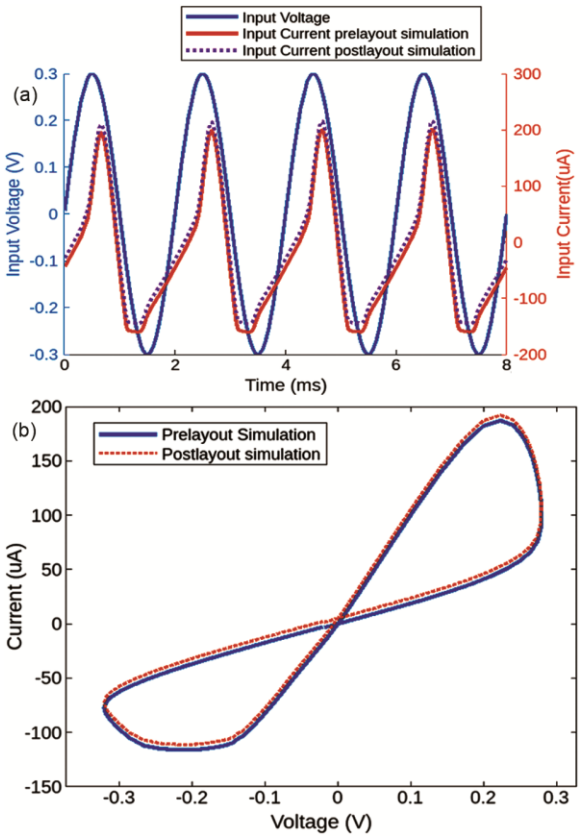

Fig. 6 — Transient analysis of pre-layout and post-layout simulation: (a) Voltage and Current waveform, and (b) Pinched Hysteresis Curve

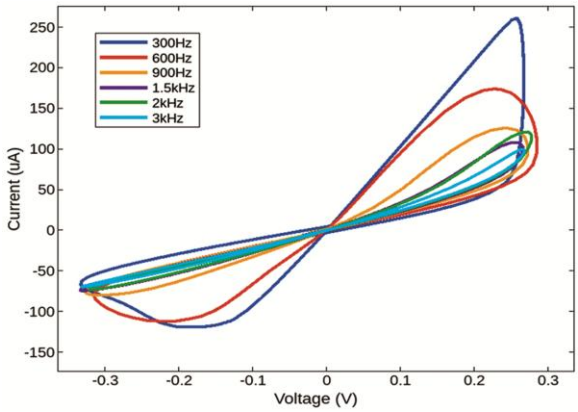

Fig. 7 — Hysteresis curve at different frequencies

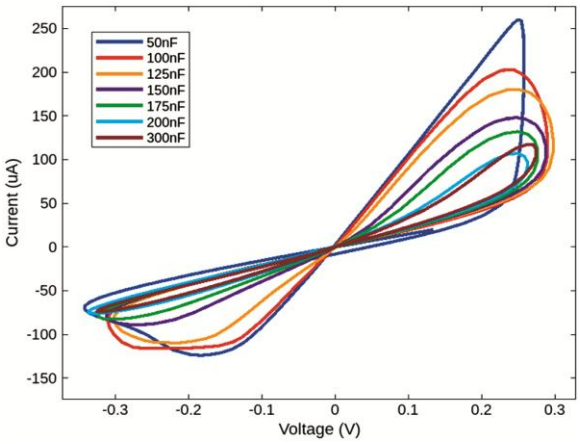

Fig. 8 — Pinched hysteresis curve at different capacitor values

OTA. Figure 8 illustrates the pinched hysteresis curves at $f = 500Hz$ for the capacitance values of $50nF$, $100nF$, $125nF$, $150nF$, $170nF$, $200nF$, and $300nF$.According to the graphs, the proposed memristor operates like a linear resistor at $800nF$ and beyond, and as capacitance grows, the lobe size of the pinched hysteresis curve diminishes.

6.4 Temperature Variation

At nominal-nominal (NN) process corner the proposed memristor circuit is simulated by varying temperature ranging from $-40^0C\ to\ +120^0C$. The pinched hysteresis curve for the varied temperature values $-40^0C, 0^0C, 40^0C, 80^0C$ and 120^0C at $f = 500Hz$ as given in the Fig. 9. It has been noted that the memristor circuit exhibits steady behavior across a broad temperature range.

6.5 Process Corner Variation

The performance of monolithic integration is significantly influenced by the process corners. The simulation of the memristor circuit is shown in [Fig. 10 (a-d)] at four distinct process corners: Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF), and Slow-Slow (SS).Thus, the proposed model performs well for a different process corner with wide range of temperatures.

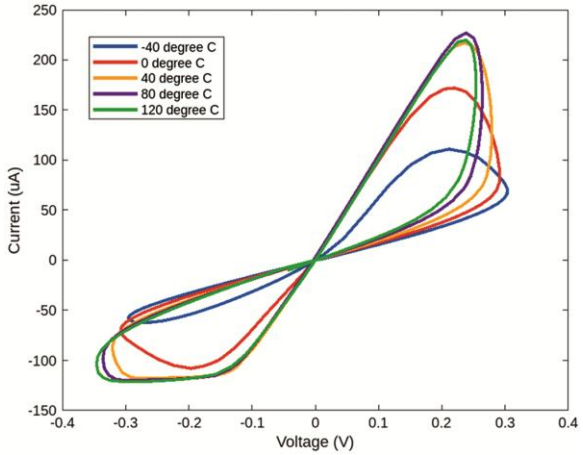

Fig. 9 — Pinched hysteresis curve at different temperature values

6.6 Non-Volatility Test

To validate the proposed memristor circuit's functioning, the non-volatility test needs to be proven. A pulse signal with a duration of $100\mu s$, a pulse width of $50\mu s$, and an amplitude of $40mV$ is delivered to the suggested memristor circuit in order to demonstrate this characteristic. The memristance varies in response to an input signal in incremental and decremental configurations, respectively, as shown in [Fig. 11(a & b)]. The figure makes it evident that the memristance value stays constant in the absence of an input signal.

6.7 Applications

As seen in Fig. 12, the proposed memristor model is implemented as a simple Schmitt trigger circuit utilizing an Op-Amp. The routine analysis provided in Eq. (24, 25) can be used to characterize the Schmitt trigger switching threshold voltages.

$$V_{TH} = V_{DD}\left(\frac{M_R}{R}\right) \quad \ldots (24)$$

$$V_{TL} = V_{SS}\left(\frac{M_R}{R}\right) \quad \ldots (25)$$

where V_{DD} & V_{SS} represent the Op-Amp circuit's supply voltages.The memristor's state can be changed at any instant of time to change the threshold voltage since the threshold voltage (V_{TH} , V_{TL}) is dependent on the memristancevalue M_R. A two-stage Op-Amp[30] is utilized in the simulation, with a supply voltage of around $1.2\,V$ and resistance set at $R = 100k\Omega$.

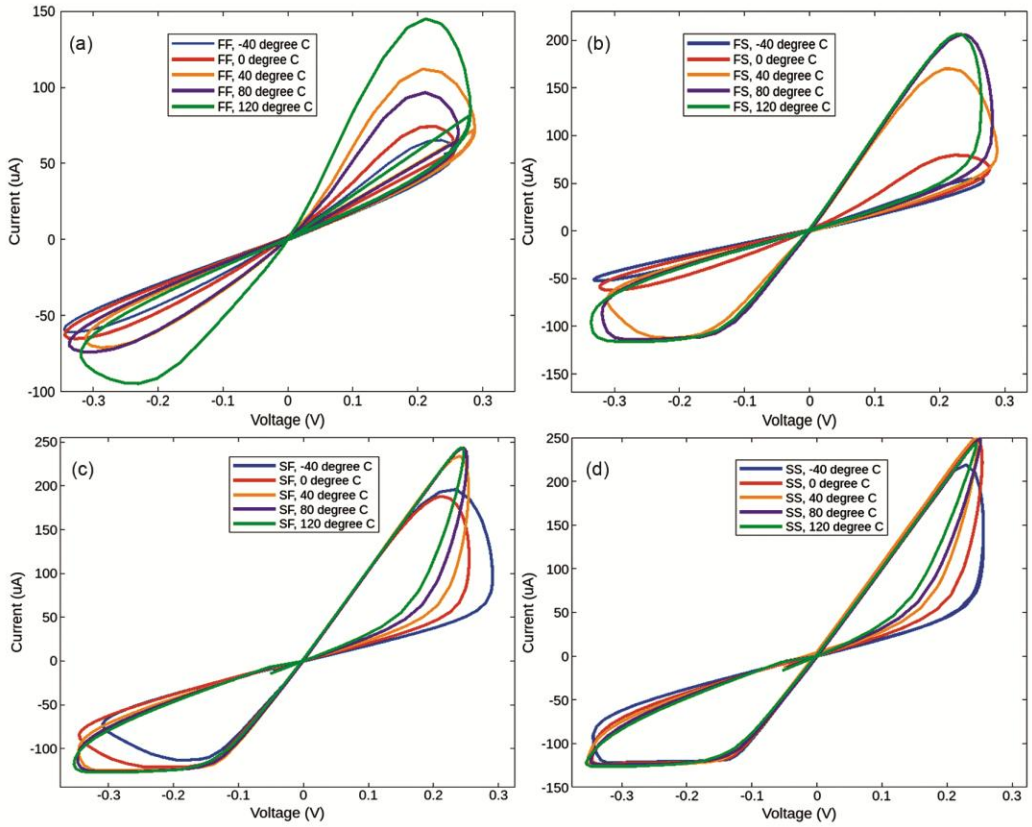

Fig. 10 — Process corner variations: (a) Fast-Fast (FF) (b) Fast-Slow (FS) (c) Slow-Fast (SF) (d) Slow-Slow (SS)

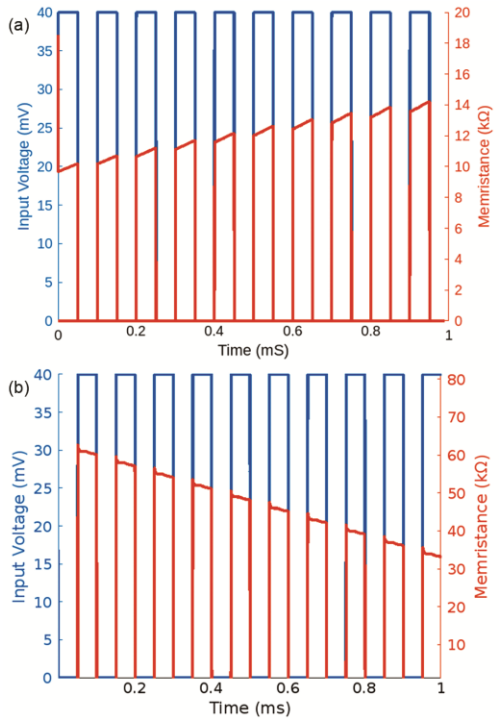

Fig. 11 — Memresistance changes in response to input voltage signal pulses. (a) Incremental type (b) Decremental type

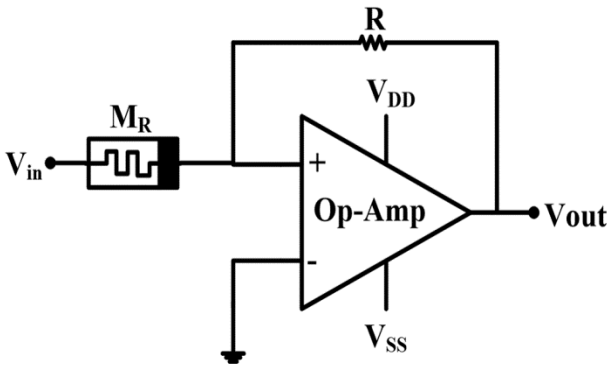

Fig. 12 — Schmitt trigger circuit based on Op-Amp and memristor

A sinusoidal input signal with a voltage of $300mV$ peak to peak and a frequency of $500Hz$ is applied. Figure 13(a, b) clearly illustrates the threshold voltage in transient response as well as the Schmitt trigger's hysteresis curve.

In addition to the Schmitt trigger, the implementation of the memristor 2-input CMOS NAND logic gate[52] is demonstrated in Fig. 14 (a), where V_1 , V_2 are inputs and V_{out} is output. Because of the interaction between the inputs at node X, the

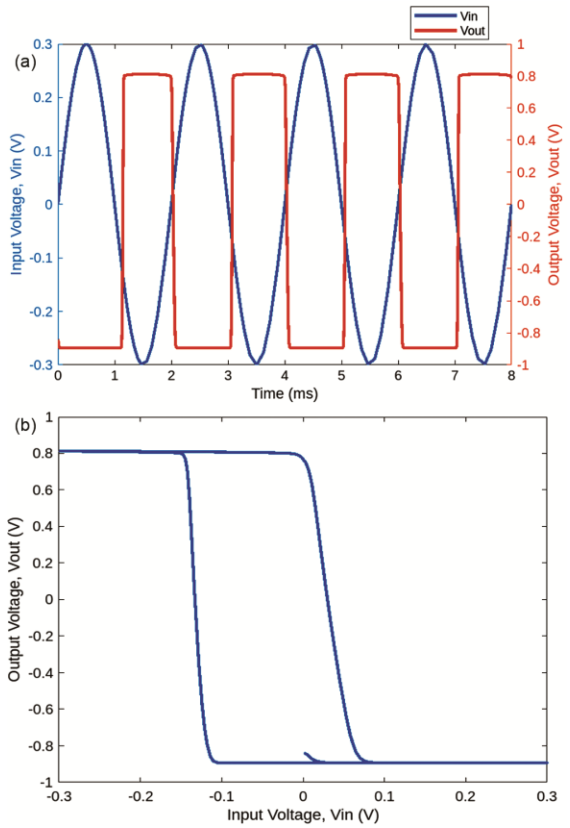

Fig. 13 — Schmitt trigger. (a) Input and output voltage waveforms (b) Hysteresis curve

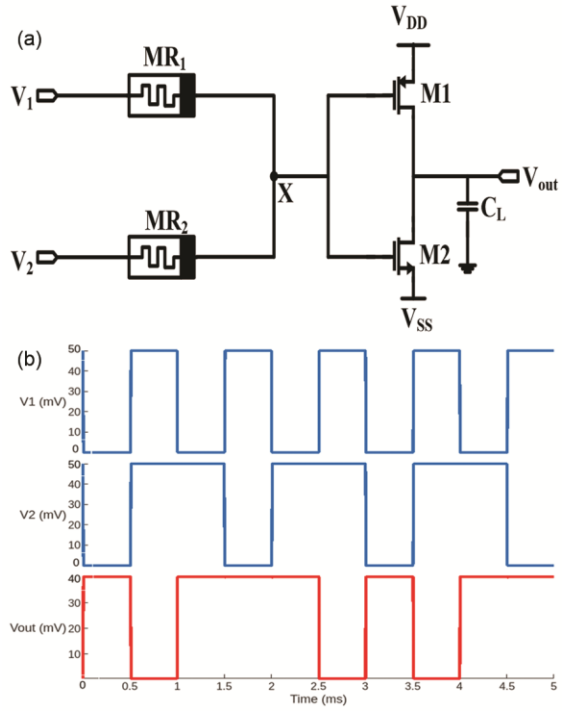

Fig. 14 — Memristor based CMOS NAND logic. (a) 2-input CMOS NAND logic gate (b) Input and output voltage waveform

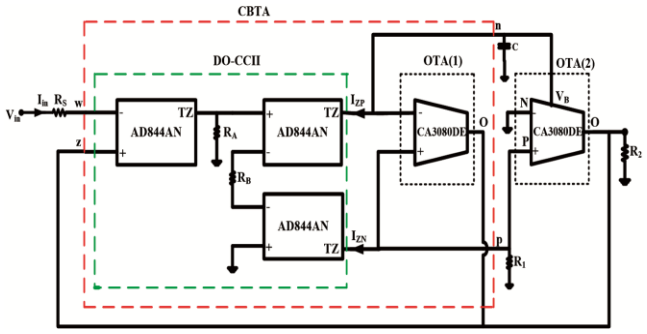

Fig. 15 — Schematic illustration of the proposed memristor model based on IC

voltage at that point (X) depends on the applied input voltages V_1 *and* V_2 as it can be observed. The CMOS inverter receives the voltage at node (X), which is determined by the input pattern. A memristor-CMOS NAND logic gate with a comparable transient response is shown in Fig. 14(b), which is the output of a CMOS inverter. Other applications can likewise be made of using proposed memristor circuit [53-54].

6.8 Experimental Results

Using commercially available IC CCII ($AD844AN$) and OTA ($CA3080DE$), the memristor circuit design, whose schematic as shown in Fig. 4 (a), is experimentally verified on a breadboard. Here three AD844 ICs are used to implement DO-CCII and in addition, two CA3080 are used, because one CA3080 (OTA (1)) is to build CBTA[39]combining with DO-CCII and the other CA3080 (OTA (2)) is for implementation of OTA as shown in the Fig. 15. The list of additional tools needed for experimental verification includes an oscilloscope, function generator, and power supply. combining with DO-CCII and the other CA3080 (OTA (2)) is for implementation of OTA as shown in the Fig. 15. The list of additional tools needed for experimental verification includes an oscilloscope, function generator, and power supply. The DC Supply voltages for proper operation of active components used are $\pm 7.5V$ and the passive component values are $R_S = 1k\Omega, R_A = R_B = 100\Omega, R_1 = 3.2k\Omega, R_2 = 1k\Omega$ and capacitor $C = 0.1\mu F$ are selected. The proposed memristor circuit's whole hardware configuration, together with the associated voltage and current waveform plots and pinched hysteresis curve at $f = 1\ kHz$, are shown in Fig. 16 (a-c). Lastly, Table 3 compares the proposed memristor to various other memristor circuits.

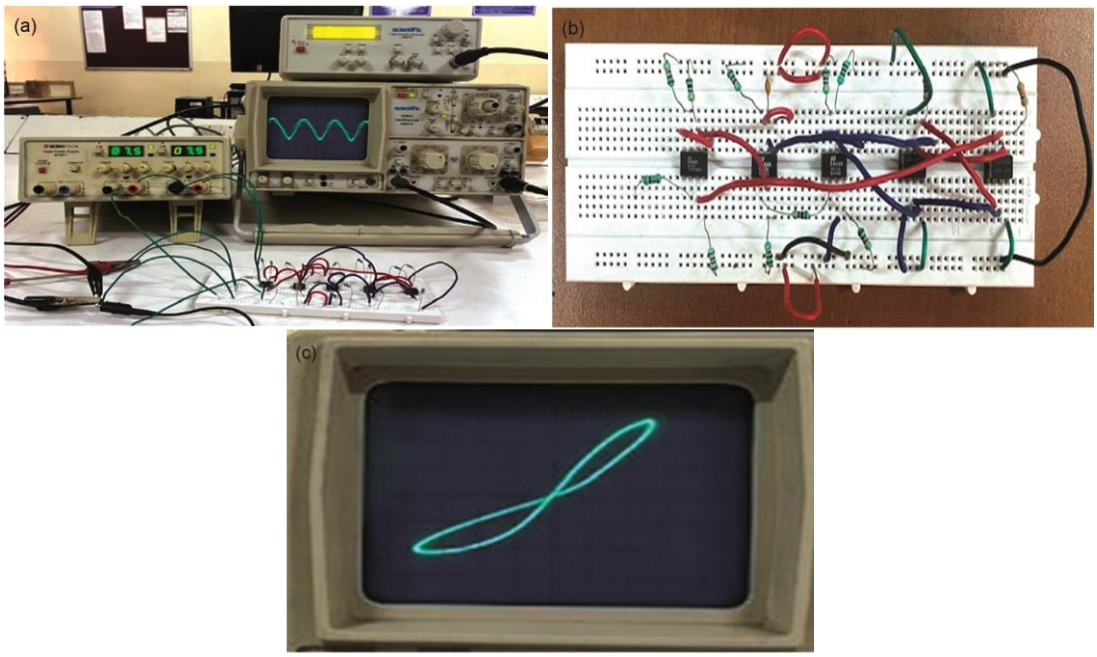

Fig. 16 — Experimental setup for the proposed memristor. (a) voltage and current waveform display in the experimental setup (b) Top view of circuit setup. (c) Pinched hysteresis curve at $f = 1kHz$

Table 3 — The proposed memristor circuit's comparison with other existing memristor models

Ref.	Grounded (G)/ Floating(F)/	No. of Active Elements	No. of Passive Components	Incremental/ Decremental Type	Simulation/ Experimental	No. of External Multiplier Used	Electronic Tunability (Yes/No)	Technology Used	Power Supply	Power Consumption	Layout Area	Max. Frequency of operation
17	Grounded	4-MOS	-	Incremental	Simulation	Nil	No	CMOS (180nm)	±0.9 V	-	366µm^2	100MHz
18	Grounded	1- VDTA, 1-MOS CAP	-	Both	Both	Nil	Yes	CMOS (180nm)	±0.9 V	-	1035µm^2	50MHz
19	Grounded	1-DVCCTA	3-R, 1-C	Both	Both	Nil	Yes	CMOS (250nm)	± 1.5V	4.88mW	-	1MHz
20	Grounded	1-CCCII	1-C	Both	Simulation	Nil	No	CMOS (180nm)	±0.9 V	-	7183µm^2	7.5M Hz
21	Grounded	1- CBTA, 1- MUL*	2-R, 1-C	Both	Simulation	1	Yes	CMOS (180nm)	±0.9 V	-	-	104MHz
22	Grounded	1-CFTA	1-C	Both	Both	Nil	Yes	CMOS (180nm)	±1.2V	-	-	9MHz
23	Floating	1-OTA 2-PMOS	1-C	Both	Simulation	Nil	Yes	CMOS (180nm)	± 1 V	-	-	Few Hz
24	Floating	1- VDTA	1-R, 1-C	Both	Simulation	Nil	Yes	CMOS (180nm)	±0.9 V	-	1064µm^2	50MHz
25	Floating	4-CCII, 3- OTA	6-R, 1-C	Incremental	Both	Nil	Yes	CMOS (180nm)	±15 V	1.2µW	-	10kHz
26	Floating	1-DO-OTA, 1-DVCC, 2-PMOS	1-C	Both	Both	Nil	Yes	CMOS (180nm)	±0.9V	-	10710µm^2	1.5MHz
27	Floating	5-CCII, 1 MUL*	4-R, 1-C	Incremental	Both	1	No	CMOS (180nm)	±10 V	-	-	20.2kHz

(*Contd.*)

Table 3 — The proposed memristor circuit's comparison with other existing memristor models (*Contd.*)

Ref.	Grounded (G)/ Floating(F)/	No. of Active Elements	No. of Passive Components	Incremental/ Decremental Type	Simulation/ Experimental	No. of External Multiplier Used	Electronic Tunability (Yes/No)	Technology Used	Power Supply	Power Consumption	Layout Area	Max. Frequency of operation
28	Floating	5-OPAMPs, 1-MUL*, 12-Transistors	8-R, 1-C	Both	Experimental	1	No	--	± 15V	-	-	800Hz
29	Floating	3-MOS	1-C	Decremental	Both	Nil	No	CMOS (180nm)	±0.9V	6.725nW	2803µm^2	100kHz
30	Floating	1-OPAMP, 1-MOS	3-R, 1-C	Both	Both	Nil	No	CMOS (90nm)	±1.5 V	1.75mW	812µm^2	20kHz
31	Both	1-DDCC, 1-MUL*	1-R, 1-C	Both	Simulation	1	No	CMOS (350nm)	±1.5 V	72.4mW	-	1MHz
32	Both	3-CCII (5-CCII(F)), 1-MUL, 1-Voltage Buffer(F)	4-R(6-R(F)), 1-C	Both	Both	1	No	-	-	-	-	5kHz
33	Both	2- AD844N, 1- MUL*, 2- PMOS	1-R(G), 1-C(G), 2-R (F)	Incremental	Simulation	1	No	CMOS (250nm)	±10 V	-	-	1kHz
34	Both	1-CCTA	3-R, 1-C	Both	Both	Nil	Yes	CMOS (180nm)	±1 V	18mW	-	20MHz
35	Both	1-CCCCTA	2-R, 1-C	Both	Both	Nil	Yes	CMOS (180nm)	±1.1 V	2.2mW	1848µm^2	1MHz
36	Both	1-CBTA	1-C	Both	Both	Nil	Yes	CMOS (180nm)	±1 V	-	1173µm^2	2MHz
Proposed	Grounded	1-CBTA, 1-OTA	3-R, 1-C	Both	Both	Nil	Yes	CMOS (90nm)	± 1.2V	2.76mW	719.4µm^2	7kHz
		3-AD844AN, 2-CA3080DE	5-R, 1-C						± 7.5V			26kHz

7 Conclusion

In this paper, presented a charge controlled memristor model that comes with the most flexible analogue blocks CBTA and OTA. The proposed memristor circuit is proven viable by the theoretical explanation that aligns with the simulation and practical data. Furthermore, the simulation and practical results meet three fingerprints of the memristor that ensure the memristor's basic properties. The proposed memristor model architecture has the following advantages: 1) minimal power consumption; 2) easy to use and adaptable design; 3) required fewer active and passive components; 4) broad frequency range ($100Hz - 7kHz$) of operation. Additionally, this memristor model can be used to digital and analogue circuits, such as signal processing circuits, neuromorphic circuits, and analogue computations. The proposed memristor model demonstrates every memristor property, which has been demonstrated theoretically, practically, and through simulations; as such, it is suitable for IC manufacture.

References

1 Chua L, *IEEE TCT*, 18 (5) (1971) 507.
2 Chua L O & Sung M K, *Proc IEEE*, 64 (2) (1976) 209.
3 Chua L O, *IEEE Expert Now Edu Course*, 2009.
4 Strukov D B, *et al.*, *Nature*, 453 (7191) (2009) 80.
5 Di Ventra M, *et al.*, *Proc IEEE*, 97 (10) (2009) 1717.
6 Yin Z, *et al.*, *IEEE TCS II*, 62 (4) (2015) 402.
7 Esch J, *Proc IEEE*, 97 (10) (2009) 1715.
8 Adhikari S P,*et al.*, *IEEE TCS I*, 60 (11)(2013) 3008.
9 Biolek D, *et al.*, *ECCTD*, Antalya, Turkey, 2009, 249.
10 Almurib H A F,*et al.*, *IEEE TCDS*, 10 (4)(2016) 292.
11 Pershin YV& Di Ventra M, *IEEE TCS I*, 57 (8)(2010) 1857.
12 Adam G C, *et al.*, *IEEE Trans Electron Devices*, 64 (1) (2017) 312.
13 Driscoll T, *et al.*, *Appl Phys Lett*, 97 (9) (2010) 093502.
14 Sharma P K, *et al.*, *IEEE Access*, 8 (2020) 171397.
15 Vourkas I, *et al.*, *Proc IVSW, St. Feliu de Guixols, Spain*, (2016)1.
16 Yu D, *et al.*, *IEEE Trans. Circuits Syst. I, Reg. Papers*, 61 (10) (2014) 2888.
17 Babacan Y, *et al.*, *IEEE Transactions on Electron Devices*, 65 (4) (2018)1 625.
18 Yeşil A, *et al.*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 38 (6) (2019) 1123.

19 Ranjan RK,*et al*., *AEU - Int J Electron Comm*, 82(2017) 177.
20 Yesil A & Babacan Y, *J Circuits Syst Comput*, 30 (2020) 2150151:1.
21 Ayten U E *et al*., *AEU - Int J Electron Comm*, 82 (2017) 109.
22 Prasad S S *et al*., *IEEE Access*, 9 (2021) 64065.
23 Babacan Y & Kaçar F, *Anal Integ Signal Proc*, 90 (2017).
24 Vista J & Ranjan A, *EEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40 (2) (2021) 364.
25 Sözen H & Çam U, *Anal Integ Signal Proc*, 89 (3) (2016) 655.
26 Yesil A, *et al*., *AEU-Int J Electron Comm*, 123 (2020) 153315.
27 Sánchez-López C, *et al*., *IEEE Trans Circuits Syst II, Exp Briefs*, 61 (5) (2014) 309.
28 Kim H, *IEEE Trans Circuits Syst I, Reg Papers*, 59 (10) (2012) 2422.
29 John V & Ranjan A, *IEEE Transactions on Very Large - Scale Integration (VLSI) Systems*, (2019) 1.
30 Suresha, B. *et al*., *Analog Integrated Circ Sig Proc*, 118 (2024) 77.
31 Yeşil A, *et al*., *Microelectron J*, 45 (3) (2014) 282.
32 Zhao Q, *et al*., *Chaos*, 29 1 (2019) 013141.
33 Sharma V K, *et al*., *Procedia Comp Sci*, 171 (2020) 1064.
34 Sagar, *et al*., *Chaos, Solitons & Fractals*, 183 (2024) 114824.
35 Kumar P, *et al*., *AEU - Int J Electron Comm*, 190 (2025) 155624.
36 Kumar A & Chaturvedi B, *Electronics 2024*, 13(2024)3331.
37 Biolek D, *et al*., *Proceedings of IEEE Asia-Pacific conferences on circuits and systems*, (2010)800.
38 Vista J & Ranjan A, *Analog Integr. Circuits Signal Process*, 104 (1) (2020) 37.
39 Ayten U E, *et al*., *AEU - Internat J Electron Comm*, 64 (6) (2010) 503.
40 Raj A, *et al*., *Analog Int Circuit Sig Proc*, 109 (2021) 47.
41 Ayten U E, *et al*., (2014), https://api.semanticscholar.org/CorpusID:8707688.
42 Sagbas M, *et al*., (2013), https://api.semanticscholar.org/CorpusID:18594008.
43 Ayten U E, *et al*., *Radio Engg*, 21 (2012) 11.
44 Koksal M *et al*., *Circuits Syst Signal Process*, 31 (2012) 435.
45 Ayten UE *et al.*, (2012), *International Journal of Electronics*, 99:8, 1133-1144,
46 Sagbas M & Köksal M, *J Circuits Syst Comput*, 21 (2012) n.
47 Sagbas M, *AEU - International J Electron Comm*, 65 (10) (2011) 798.
48 Sagbas M, *et al.*, *IET Circuits Devices Syst*, 4 (2010)78.
49 Güneş E O *et al*., *Analog Integrated Circ Sig Process*, 66(2011)81.
50 Kaewdang K & Surakampontorn W, *AEU – Int J Electron Comm*, 61 (5) (2007) 300.
51 Shankar C & Singh S V, *Ind J Pure App Phys*, 57 (2019) 52.
52 ChoK, *et al*., *Microelectron J*, 46 (3) (2015) 214.
53 Ghosh M, *et al*., *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 42 (3) (2023) 978.
54 Abuelma'atti M T & Khalifa Z J, *Analog Int Circ Sig Process*, 86 (2016) 141.