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CMOS Mutator Circuits based on VD-DIBA for Realization of Meminductor/Memcapacitor and its Application

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In this research, meminductor and memcapacitor mutators have been introduced by utilizing voltage differencing differential input buffered amplifier in conjunction with a memristor and one capacitor. Notably, the memristor integrated into the proposed design is composed solely of transistors and a capacitor. It is asserted that CMOS-based memristors offer substantial advantages over their counterparts constructed from active blocks, as commonly found in existing literature, particularly in terms of integration, compatibility, power efficiency, reliability, and cost-effectiveness. The memcapacitor mutator can be easily derived from the meminductor mutator and vice versa by swapping the positions of the capacitor and memristor. Simulation of the proposed designs is carried out with the help of LTSPICE tool with TSMC 180nm CMOS technology parameters. The results obtained demonstrate that these designs exhibit commendable performance characteristics across a wide spectrum of frequencies, and notably, they successfully withstand scrutiny under the non-volatility test. Additionally, adaptive learning circuit is designed using the proposed mutator to corroborate the effectiveness of the design.

Keywords: VD-DIBA, Memristor, Meminductor, Memcapacitor, Mutator, Adaptive learning circuit

1 Introduction

In circuit theory, conventional circuit elements namely resistor, capacitor, and inductor are very popular but a new element which has drawn worldwide attention of researchers and practicing engineers is the "memristor". It has a very unique characteristics which cannot be obtained using any conventional circuit element or using the combination of more than one circuit element. Therefore, in recent years, memristor has emerged as a promising paradigm in the field of electronics, offering unique characteristics that distinguish it from conventional circuit elements. The term "memristor", coined by Prof. Leon Chua in 1971, refers to a two-terminal non-volatile memory device, embodying the fourth fundamental circuit element alongside resistors, capacitors, and inductors[1]. Unlike traditional components, memristors exhibit changes in resistance based on the direction and magnitude of applied voltage. This intrinsic property allows memristor to retain a memory of the amount of charge that has flowed through them, rendering them particularly suitable for many applications ranging from non-volatile memory to neuromorphic computing.

The non-volatile nature of the memristor means that the information stored in memristor persists even when power is turned off, providing a foundation for robust and energy efficient memory solutions. Memristors exhibit unique property of resistance modulation, which hold significant promise for a range of applications and therefore it is being used in electrical, electronics, and computer engineering. Since memristors are a relatively novel and complex electronic component, emulators play a crucial role in understanding, testing, and developing applications for memristor-based systems without the need for physical prototypes. It allows researchers and engineers to explore the potential of memristors in different contexts, such as non-volatile memory, neuromorphic computing, and analog signal processing, without the need for physical memristors. As we embark on harnessing the potential of memristors, the development of effective tools for exploration and experimentation becomes paramount. In this context, the memristor emulator emerges as a critical instrument, serving as a bridge between theoretical concepts and practical implementations.

In 2008, HP Laboratory achieved a significant milestone by creating the first physical manifestation of a memristor based on TiO_2[2]. After successful implementation of many memristor emulators

researchers and engineers are now trying to emulate the behaviour of two other memory elements namely meminductors and memcapacitors [3]. Memristor is an acronym of memory and resistors. Similarly, meminductor and memcapacitor are concatenations of memory & inductor, and memory & capacitor, respectively. These elements are treated as extensions of memristors and widely being used in various applications such as neuromorphic computing, chaotic oscillator, security, etc.

The key parameters defining these memelements are Φ (induced flux), ρ (time-integral of flux), q (electric charge) and σ (time-integral of charge). The relationship among these circuit parameters for three memelements is depicted in Fig. 1.

Recent research has explored the grounded[4–10] and the floating structure[11–18] of memristor emulators when analyzing them structurally. Also, mutator structure applications have been presented[19], which transform the memristor into a meminductor and memcapacitor. In 2010, an operational amplifier, resistor, memristor and capacitor were used to create the first memcapacitor and meminductor emulator[20]. Floating meminductor and memcapacitor emulators are constructed with a memristor, two single-output/double-output current conveyors, and passive elements[21].

The description of a memristor-less memcapacitor and meminductor emulator employing a multiplier, a current-controlled current source, operational amplifiers, resistors and capacitors has been provided by Fouda and Radwan in 2012[22]. Next, a memcapacitor emulator has been designed using the memristor model which is light-dependent, and it requires five op-amps, a capacitor and a few resistors[23]. In 2013 an expandable memcapacitor mutator has been reported where the mutator consists of resistor and capacitor as two CFOAs, and the output port is terminated using a memristor emulator[24]. There has been a study on a floating memcapacitor that uses a memristor, four

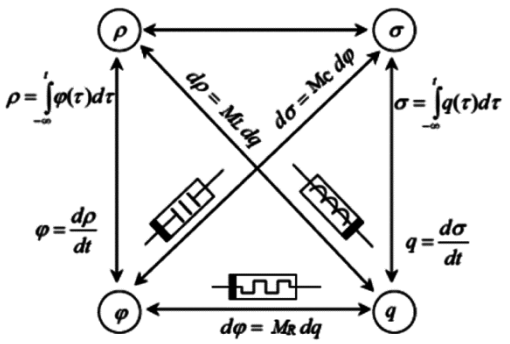

Fig. 1 — Relation between memelements

current conveyors, a single capacitor and a few resistors. A multiplier, two op-amps, a capacitor, and a few resistors have all been used to create a memristor emulator[25]. Next, it has been stated that two AD844s, a memristor and two passive elements (one capacitor and one resistor) can be used to create a meminductor and memcapacitor emulator. Memristor emulator used in the design of memcapacitor and meminductor has been produced employing two AD844s, two op-amps, capacitors and few resistors[26]. Babacan[27] developed a memcapacitor circuit with two capacitors and one transconductance amplifier (OTA) for simulating genuine elements. A mutator structure is not necessary for the operation of an OTA-based memcapacitor emulator. To acquire the memory behaviour of the memcapacitor, one of the OTA's outputs in this structure is connected to a capacitor. An analog implementation of a memcapacitor was introduced using a Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) with grounded passive circuit components[28]. Various techniques for simulating meminductors without utilizing actual memristors have been described in the literature. One approach involves a floating memristor-less meminductor emulator utilizing current-conveyors, resistors, capacitors, and a buffer[29]. Another method employs charge-controlled techniques with operational amplifiers, a multiplier, MOSFETs, inductors, and capacitors[30]. Mutator-based approaches have also been explored, utilizing operational amplifiers, multipliers, buffers, current sources, resistors, and capacitors[31]. A universal mutator has been developed using off-the-shelf active devices, resistors, and a capacitor to emulate memristor, memcapacitor, and meminductor behaviors[32]. Furthermore, other techniques involve floating memcapacitor emulators employing instrumentation amplifiers, binary capacitors, switches, and resistors, as well as meminductor emulators utilizing gyrators composed of operational amplifiers, memristors, resistors, and capacitors[33]. In 2020, a meminductor emulator employing second generation current conveyors (CCIIs), capacitors, and resistors was reported [34]. Subsequently, a proposal for a floating memcapacitor and meminductor emulator has been presented, utilizing voltage differencing current conveyor (VDCCs), a memristor, and a grounded capacitor[35].

Upon reviewing the existing literature, it is evident that most memcapacitor and meminductor mutator circuits incorporate memristors constructed with

active blocks and a significant number of active and passive components, resulting in complex circuits. This study addresses this complexity by designing memcapacitor and meminductor circuits with a simplified structure. It comprises only one active block, specifically a voltage differencing differential input buffered amplifier (VD-DIBA), a memristor created exclusively using transistors and a capacitor without the need of any matching condition.

2 Background and Blocks Used

2.1 CMOS based Memristors

CMOS-based memristors have emerged as a significant technology in the realm of electronics and computing due to their unique properties and versatile applications. These devices, implemented using complementary metal-oxide-semiconductor technology, exhibit non-volatile memory behavior, making them ideal for memory storage applications. With lower power consumption, CMOS-based memristors are energy-efficient and their compatibility with CMOS technology enables high integration on a single chip, facilitating compact and high-density memory solutions for various electronic systems.

A floating CMOS based memristor operating up to 13MHz designed using three NMOS, one DC current source and one capacitor was reported in[36]. In this configuration, 2 NMOS along with DC current source and capacitor acts as feedback circuit that produces a feedback voltage difference of magnitude ($V_0 = V_A - V_B$). V_A and V_B being the external voltage sources. The flow of current in 3rd NMOS causes a discharge in the capacitor and lets the memristor remember information even when not powered. In simpler terms, the memristor's resistance is based on how electricity flowed through it previously. A MOSFET based high-frequency floating memristor emulator was suggested in [37]. Three NMOS were utilized for the memristor design and an additional NMOS was employed for the implementation of grounded capacitor. This memristor can be used both in incremental and decremental modes. A simple CMOS memristor emulator without the need of an active element or multiplier circuit, consisting merely of four transistors and a grounded capacitor is used for the reported memcapacitor mutator circuit in[38]. Two different configurations: one for decremental configuration and one for incremental configuration; were reported in this study. Capacitor used in the circuit is responsible for the memory effect. A CMOS-based floating memristor circuit was reported in[39]. The implementation of this circuit employs a constant current source, an NMOS and a single PMOS. The circuit design leverages intrinsic parasitic capacitance to achieve memory-like characteristics. In a passive voltage controlled memristor deigned using only one MOSFET attached to an R–C tank circuit has been reported[40]. The suggested emulator works without any external bias with zero static power consumption. This memristor is capable of operating in both grounded and floating modes.

2.2 Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA)

VD-DIBA is an electronic circuit designed for amplifying the difference of voltages between the two input terminals. This amplifier configuration combines the benefits of differential input which enables amplification of signal's variation between two input voltages and a buffered amplifier architecture. The buffering stage serves to isolate the input from the output, preventing loading effects and maintaining signal integrity.

In Figs. 2 and 3, the symbol and the CMOS circuit diagram of the VD-DIBA are shown respectively. The VD-DIBA consists of a voltage source influenced by the differential voltage having a voltage gain of unity, and a current source influenced by the differential voltage having a transconductance of g_m. High impedance is exhibited at the V-, V+, and Z terminals of VD-DIBA. Internally, the terminal V- of the differential voltage buffer is connected to the terminal Z. The terminal V+ of this voltage buffer is monitored across port V. Consequently, the buffered differential voltage is directly delivered to port W, which is the output port.

The port equations describing the characteristics of VD-DIBA are given in Eq. (1) below:

$$\begin{pmatrix} I_+ \\ I_- \\ I_Z \\ I_V \\ V_W \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_Z \\ V_V \\ I_W \end{pmatrix} \quad \ldots (1)$$

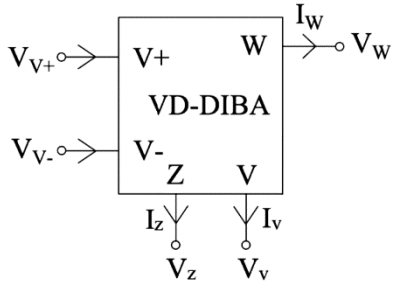

Fig. 2 — VD-DIBA symbol

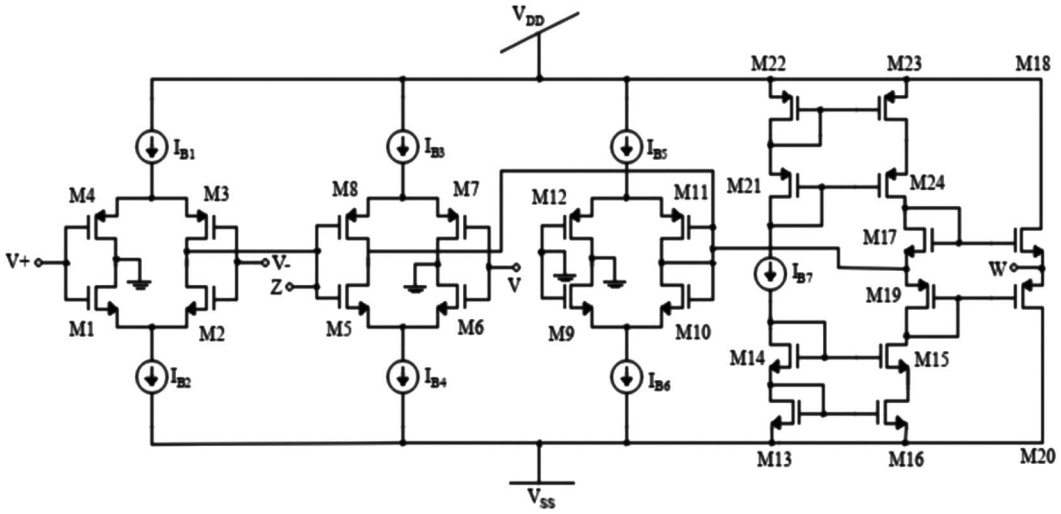

Fig. 3 — CMOS circuit of VD-DIBA

Here, current and voltage of different terminals are represented by suitable suffix with 'I' and 'V' respectively. g_m denotes the transconductance gain of VD-DIBA

3 Proposed Meminductor/Memcapacitor Mutator Configuration

The circuit for the proposed mutator configuration is shown in Fig. 4. This circuit employs a VD-DIBA block, a CMOS based memristor and a capacitor. This circuit behaves as memcapacitor or meminductor based on the characteristics of Z_1 and Z_2 elements.

The routine analysis of the circuit along with port relations shown in Equation (1) yields:

$$I_{in} = -I_W = \frac{V_{in}-V_W}{Z_1} = \frac{V_Z}{Z_1} \quad \ldots (2)$$

$$I_Z = g_m V_{in} \quad \ldots (3)$$

$$V_Z = Z_1 \cdot g_m V_{in} \quad \ldots (4)$$

3.1 Case 1 — Z_1 = Memristor and Z_2 = Capacitor

The suggested configuration behaves as meminductor when Z_1 is replaced by a memristor and Z_2 by a capacitor. For realizing floating memristor (Z_1), CMOS configuration reported by J. Vista and A. Ranjan in [36] has been used. The complete circuit of the suggested meminductor utilizing the stated floating memristor is shown in Fig. 5.

In Fig. 5, considering $Z_2 = C_2$ and using Eq. (4), voltage at Z terminal (V_Z) of VD-DIBA can be represented as:

$$V_Z = \frac{g_m}{C_2}\int V_{in}\,dt \quad \ldots (5)$$

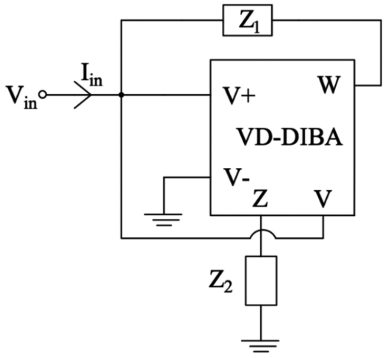

Fig. 4 — Basic circuit of proposed meminductor/memcapacitor mutator

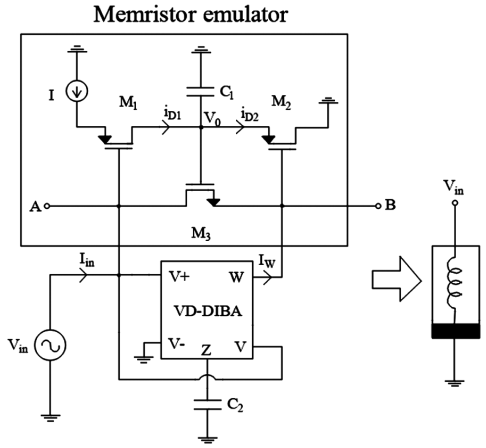

Fig. 5 — Proposed meminductor mutator circuit

Considering the fact that integration of input voltage (V_{in}) is defined as flux ($\varphi_{in}(t)$), Eq. (5) can be rewritten as:

$$V_Z = \frac{g_m}{C_2}\varphi_{in}(t) \quad \ldots (6)$$

Basic analysis of Fig. 5, combined with Eq. (2) yields:

$$I_{in} = \frac{V_Z}{M_R} \quad \ldots (7)$$

Combining Eqs. (6) and (7) yields:

$$I_{in} = \frac{g_m}{C_2 M_R}\varphi_{in}(t) \quad \ldots (8)$$

Considering the fact that meminductance is the relation between flux and current, from Eq. (8), the inverse meminductance of the proposed mutator can be deduced as:

$$M_L^{-1} = \frac{g_m}{C_2 M_R} \quad \ldots (9)$$

The time-dependent relation of M_R reported in [36], has been stated in Eq. (10).

$$M_R^{-1} = \beta[K_1 - K_2\varphi_{in}(t)] \quad \ldots (10)$$

Here, β is the transconductance of the MOSFET and K_1 and K_2 are real constants that depends on the parameters of the components constituting memristance in Fig. 4. Substituting the M_R value from Eq. (10) in Eq. (9), M_L^{-1} of proposed circuit can be expressed as:

$$M_L^{-1} = \frac{g_m\beta}{C_2}[K_1 - K_2\varphi_{in}(t)] \quad \ldots (11)$$

3.2 Case 2. Z_1 = Capacitor and Z_2 = Memristor

The suggested mutator configuration of Fig. 4 behaves as memcapacitor when Z_1 is replaced by a capacitor and Z_2 by a memristor. For realizing grounded memristor (Z_2), four transistor based tunable configurations reported by A. Yesil and Y. Babacan [38] have been used. The complete circuit of the suggested memcapacitor utilizing the stated grounded memristor is shown in Fig. 6. The mathematical analysis of this circuit is as follows

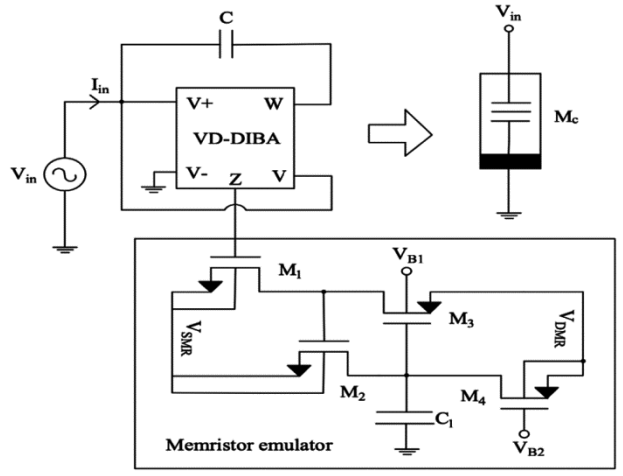

Fig. 6 — Proposed memcapacitor mutator circuit

Using Eq. (2), and considering $Z_1 = C_1$, I_{in} of VD-DIBA in Figure 6 can be represented as:

$$I_{in} = C\frac{dV_Z}{dt} = CM_R\frac{dI_Z}{dt} \quad \ldots (12)$$

Using port relation defined in Eq. (1), I_{in} can be expressed as:

$$I_{in} = CM_R g_m\frac{dV_{in}}{dt} \quad \ldots (13)$$

Mathematical rearrangement of Eq. (13) yields:

$$V_{in} = \frac{1}{CM_R g_m}\int I_{in}dt \quad \ldots (14)$$

Considering the fact that integration of input current gives charge ($q_{in}(t)$), Eq. (14) can be rewritten as:

$$V_{in} = \frac{1}{CM_R g_m}q_{in}(t) \quad \ldots (15)$$

Since, memcapacitance is the relation between flux and current, from Eq. (15), the reciprocal of the memcapacitance of the proposed mutator can be determined as:

$$M_C^{-1} = \frac{1}{CM_R g_m} \quad \ldots (16)$$

The relation of M_R for flux-controlled memristor reported in [38], has been stated in Eq. (17)

$$M_R^{-1} = P_1 - P_2\varphi_{in}(t) \quad \ldots (17)$$

Here, P_1 and P_2 are real constants that can be controlled with the help of parameter values of the components and bias used in M_R of Fig. 6. Substituting M_R value from Eq. (17) in Eq. (16), M_C^{-1} of proposed circuit can be expressed as:

$$M_C^{-1} = \frac{1}{Cg_m}[P_1 - P_2\varphi_{in}(t)] \quad \ldots (18)$$

Equations (11) and (18) represent the inverse meminductance and inverse memcapacitance of the proposed meminductor and memcapacitor respectively. These equations represent that both meminductance and memcapacitance consists of two terms one is fixed and other is variable. The constant term relies on the component parameters, while the variable term hinges on the input flux. These terms can be controlled by changing the component values of elements used in the respective designs.

4 Simulation Results and Analysis

The effectiveness of the proposed meminductor/ memcapacitor mutator circuit is validated through computer simulations utilizing LTSPICE tool with TSMC 180 nm CMOS technology parameters. In the construction of the active block VD-DIBA (Fig. 3), the MOSFETs are characterized by specific dimensions: the PMOS transistors feature a W/L ratio

of 16.6µm/0.36µm, and the NMOS transistors possess an aspect ratio of 3.6µm/0.36µm. The supply voltage used for simulating the circuits is ±1.2V, and the biasing currents (I_{B1}, I_{B2}, I_{B3}, I_{B4}, I_{B5}, and I_{B6}) are taken as 100µA, while I_{B7} is chosen to be 20µA.

The dimensions of all the MOSFETs used in the CMOS based floating memristor model utilized in the design of proposed meminductor mutator as shown in Fig. 5 are taken as $(W/L)_1 = (W/L)_2 = 1µ/1µ$ and $(W/L)_3 = 50µ/1µ$. The external current source is chosen as 10µA. The dimensions of the MOSFETs used in the CMOS based grounded memristor model utilized in the design of Fig. 6 are taken as $(W/L)_1$ = 1µm/50µm, $(W/L)_2$ = 10µm/0.54µm, $(W/L)_3$ = 25µm/0.18µm and $(W/L)_4$ = 50u/0.72u. Additionally, in all the simulations conducted for Fig. 6, the biasing voltages needed for memristor emulator are selected as: V_{B1} = 0V, V_{B2} = -0.676V and the power supplies for this element are chosen as: V_{DMR} = 0V and V_{SMR} = -0.7V.

4.1 Simulation Results of Proposed Meminductor Mutator

Simulations of the proposed VD-DIBA based meminductor mutator (Fig. 5) are conducted by providing a sinusoidal input voltage with an amplitude of 100 mV. In Fig. 7, transient analysis of the proposed meminductor mutator is shown at a frequency of 2 MHz. In this figure, the voltage at the Z terminal (V_Z) is represented instead of the flux ($\varphi_{in}(t)$) for ease of plotting, as it can be deduced from Eq. (6) that the flux of the proposed design is directly related to V_Z. To obtain pinched hysteresis loop for the proposed meminductor mutator, input current (I_{in}) is plotted against V_Z. The plots observed for various frequencies have been shown in Fig. 8. The curves for different frequencies have been achieved by adjusting the capacitance values (C_1 and C_2) accordingly.

The proposed meminductor mutator demonstrates satisfactory performance for a frequency range of 200Hz to 2MHz. Furthermore, from Figures 8(a–c), it is evident that as the frequency rises, the pinched hysteresis loop diminishes in size.

One notable property of a meminductor is its non-volatility, which refers to the ability to retain information without the need for a continuous power supply. This property is particularly advantageous in memory devices and storage applications. To validate the memory retaining property of the suggested meminductor, non-volatility test was conducted by applying an input pulse of amplitude 25mV with ON time = 2µs and time period =10µs and the waveforms observed are depicted in Fig. 9. Therefore, the proposed meminductor mutator verifies the non-volatility property.

4.2 Simulation Results of Proposed Memcapacitor Mutator

The simulations of the proposed VD-DIBA based memcapacitor mutator (Fig. 6) are carried out by applying a sinusoidal input voltage with an amplitude of 35mV. In Fig. 10, transient analysis of the proposed memcapacitor mutator is shown at a frequency of 2.5MHz. To obtain the pinched hysteresis loop, voltage across capacitor (V_{in} - V_W) which is proportional to

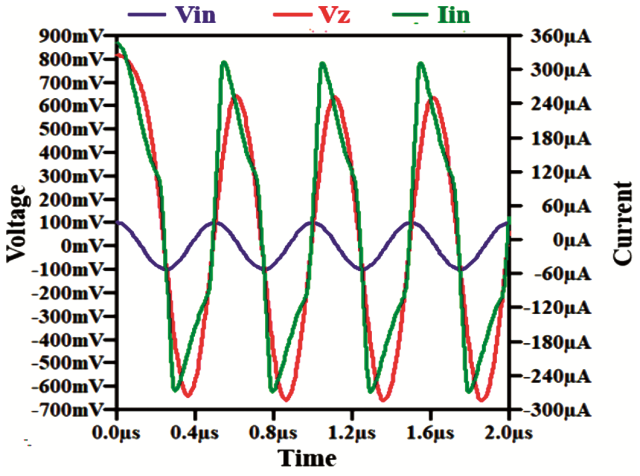

Fig. 7 — Transient analysis of the proposed meminductor mutator

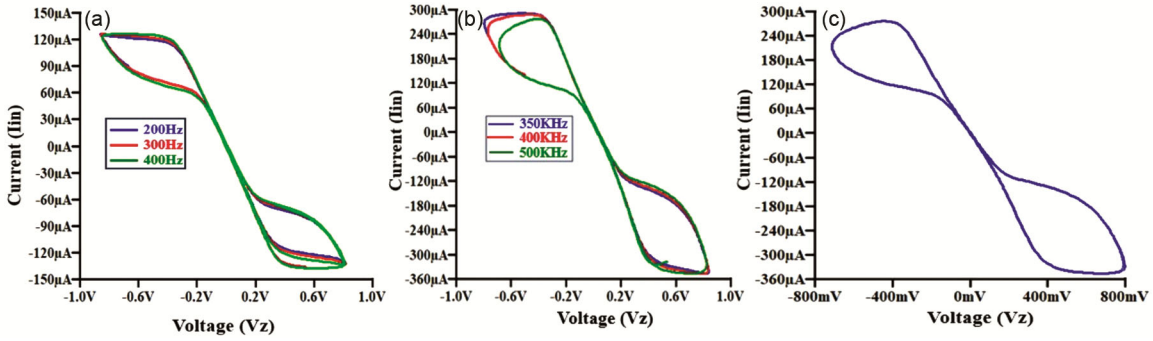

Fig. 8 — Pinched hysteresis loop for proposed meminductor at various frequencies (a) Hz (b) kHz, and (c) 2MHz

charge (q) is plotted against input voltage (V_{in}) of the proposed meminductor mutator.

The pinched hysteresis loops depicted in Fig. 11(a-c) are achieved by properly adjusting the capacitors' values (C and C_1). These curves depict that the proposed memcapacitor operates well for frequency range of 50Hz to 15MHz.

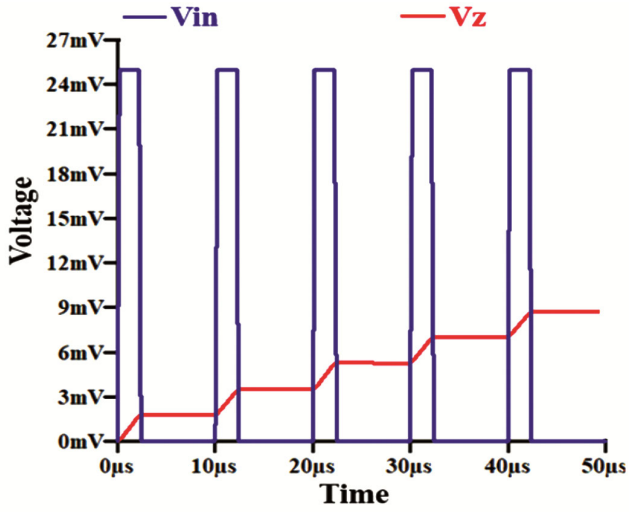

Fig. 9 — Proposed meminductor non volatility test

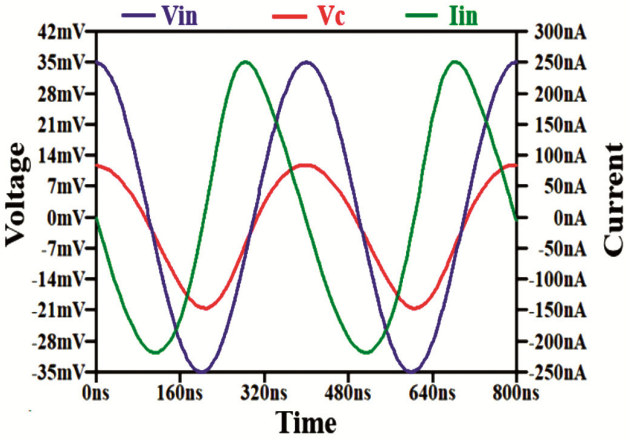

Fig. 10 — Transient analysis of proposed memcapacitor mutator

To validate the memory retaining property of the proposed memcapacitor, a non-volatility test was conducted by giving a input pulse of amplitude 1µA with ON time and time period of 3 ms and 8ms respectively as shown in Fig. 12.

4.3 Monte Carlo and Temperature Analysis of the proposed Mutators

To evaluate the robustness of the proposed mutators against environmental variations, their performance has been thoroughly analyzed under varying MOSFET parameters and temperature conditions. The circuits have been subjected to simulations with ±5% variations in two critical MOSFET parameters: threshold voltage (Vth) and aspect ratio (W/L). These variations were introduced to assess the impact of manufacturing tolerances and process variations on the circuit's behavior. Additionally, the circuits have been tested across a wide temperature range from -40°C to +85°C to examine their thermal stability and reliability under extreme environmental conditions.

To statistically analyze the impact of parameter variations, a Monte Carlo (MC) analysis has been

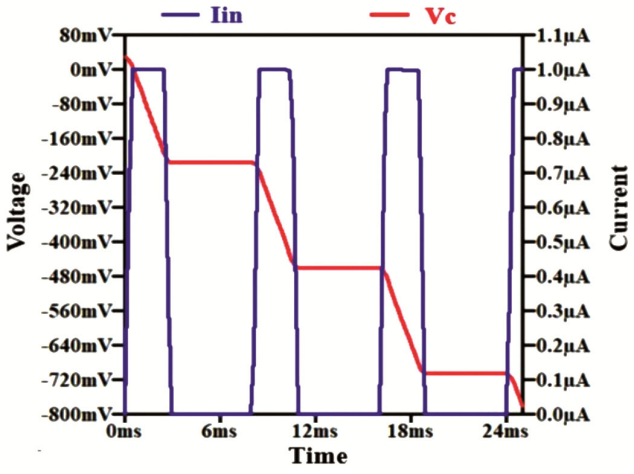

Fig. 12 — Proposed memcapacitor non-volatility test

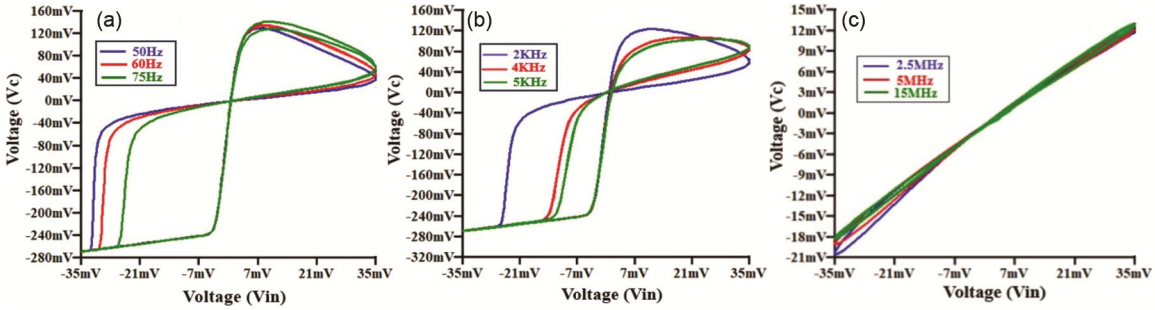

Fig. 11 — Pinched hysteresis loop for proposed memcapacitor at various frequencies (a) Hz (b) KHz (c) MHz

performed with 500 runs for each circuit. The MC simulations have been conducted using a 100 mV and 35mV peak-to-peak input signal with a frequency of 400 kHz and 2kHz for meminductor and memcapacitor respectively. The resulting PHL curves for the proposed meminductor and memcapacitor have been plotted and are presented in Figure 13 (a) and Figure 13 (b), respectively. These curves demonstrate the circuits' responses under the influence of random variations in MOSFET parameters, providing insights into their statistical behavior and tolerance to process-induced deviations.

Furthermore, the temperature analysis has been carried out to observe the effect of thermal variations on the circuits' performance. The PHL curves have been generated for the proposed meminductor and memcapacitor across the specified temperature range of -40°C to +85°C. The results of this analysis are illustrated in Fig. 14 (a) and Fig. 14 (b), respectively. These plots reveal the circuits' ability to maintain consistent performance despite significant temperature fluctuations.

The results from both the Monte Carlo and temperature analyses indicate that the proposed mutators exhibit minimal sensitivity to environmental and process variations. The PHL curves show only slight deviations under varying conditions, with no anomalous behavior observed. This confirms the robustness and reliability of the proposed meminductor and memcapacitor emulators, highlighting their suitability for practical applications where environmental stability is critical. The consistent performance across a wide range of conditions underscores the effectiveness of the proposed designs in mitigating the adverse effects of parameter and temperature variations.

5 Comparison of Proposed Mutators with Existing Literature

To demonstrate the efficacy of the proposed design, it undergoes a comparison with existing emulators detailed in the literature. This comparison, outlined in Table 1, focuses on key parameters such as maximum operating frequency and the count of active and passive elements employed. From this table it can be analyzed that the proposed mutators offer very high frequency range while being free from the requirement of any complex circuit like multiplier, integrator, differentiator, diode etc. Moreover, the proposed circuits can be realized as integrated circuits using CMOS technology.

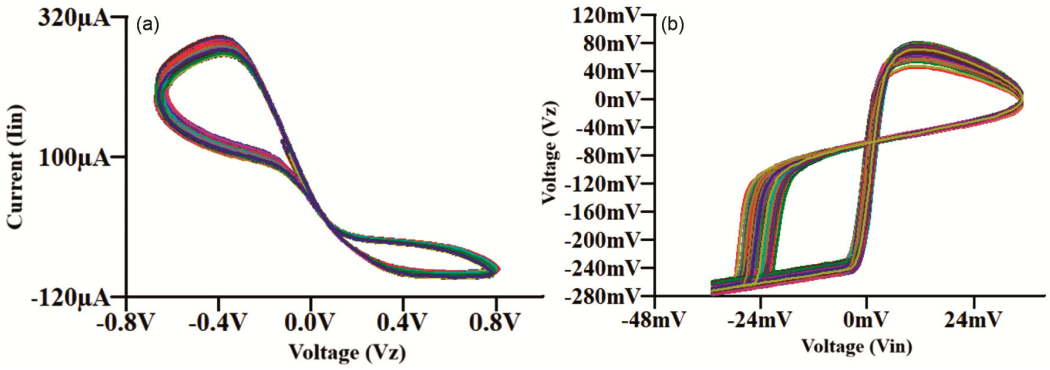

Fig. 13 — PHL curves for 500 runs of MC analysis for (a) Proposed meminductor, and (b) Proposed memcapacitor

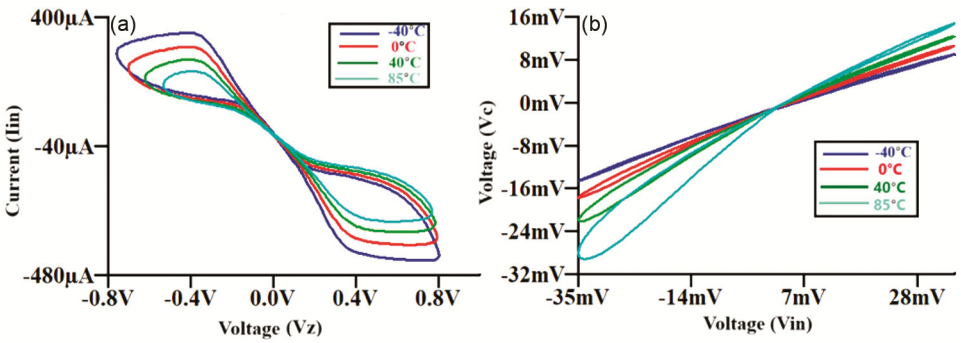

Fig. 14 — PHL curves for temperature analysis for range of -40ºC to +85ºC for (a) Proposed meminductor, and (b) Proposed memcapacitor

Table 1 —

Ref	YOP	Active Blocks Used	Use of Multiplier	Additional Components	Max Freq	MI/MC/ Both	Supply Voltage
[20]	2009	1 Op-amp	NO	1MR, 1C, 1R	8 Hz	Both	-
[22]	2012	2 Op-amp	YES	2R, 2C, buffer, inverting amplifier	10 Hz	MC	-
[23]	2012	3 Op-amp, 2AD844, 1 Diode	YES	13R, 2C, 1 LDR	10 Hz	MC	-
[24]	2013	2 CFOAs*	YES	1MR, 1R, 1C	900 Hz	MC	-
[25]	2103	4 AD844	NO	1MR, 2R, 1C	86.6Hz	MC	±15V
[26]	2014	2 CCII, 2 Op-amp, 3 Multiplier	YES	1R,1C	24.1 Hz	Both	±15V
[30]	2014	3 Op-amp, 1 Multiplier, 1 Voltage Differentiator	YES	2C,2R,1L	300 Hz	MI	±5V
[31]	2014	2 CCII, 1 Buffer	NO	1MR, 1R, 1C	800 Hz	MI	±5V
[34]	2021	2CCII Or 1 CCII and 1 OTA	YES	3C and 1R or 3C	2 kHz	MC	±20V
[35]	2021	1 VDCC	NO	1MR, 1C	0.7 MHz	Both	±0.9V
[41]	2020	1 CBTA	YES	1MR, 1C	250 kHz	Both	-
[42]	2021	1 Op-amp	NO	2C, 3R, 1MR or 2MR, 2C, 2R,	107 kHz-126 kHz	MI	±15V
[43]	2023	2 Op-amp	NO	1MR,	550 kHz	MI	-
[44]	2022	1 VDTA	NO	1MR, 1C	500 Hz		±0.9V
[45]	2024	1 DXCCDITA	NO	2C, 2R	1.5MHz	MI	±1.25V
[46]	2024	2 CCII+, 1 OTA	NO	2C, 2R or 2C, 1R	300kHz	MC	±1.2V
[47]	2024	1 VDCC	NO	4 MOSFETs	110kHz	MC	±0.9V
Proposed	-	1 VD-DIBA	NO	Memcapacitor: 2 MOS, 2C Meminductor: 4 MOS, 2C	Memcapacitor:15MHz Meminductor: 2MHz	Both	±1.2V

*CFOA: Current Feedback Operational Amplifier

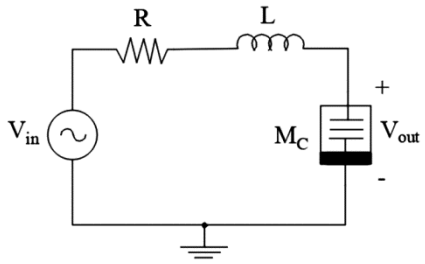

Fig. 15 — Adaptive learning circuit employing Proposed memcapacitor mutator

6 Adaptive Learning Circuit using Proposed Memcapacitor Mutator

Adaptive learning is a powerful application that imitates the behaviour of amoeba. Adaptive learning circuits that make use of the proposed memcapacitor mutator design is shown in Fig. 15. This circuit replicates how an amoeba reacts to changes in its surroundings. The applied input voltage (V_{in}) indicates variations in temperature in the amoeba's surroundings and the output voltage (V_{out1}) indicates equivalent changes in the amoeba's activity. The circuit is tested through a pulse signal of -500mV amplitude. Initially 3 consecutive pulses at an interval of 0.04µs are applied and then a 4th pulse is applied after a gap of 15µs.

Lastly another pulse of -500mV is applied after a long gap of 3.09µs. From the response plotted in Fig. 16, it

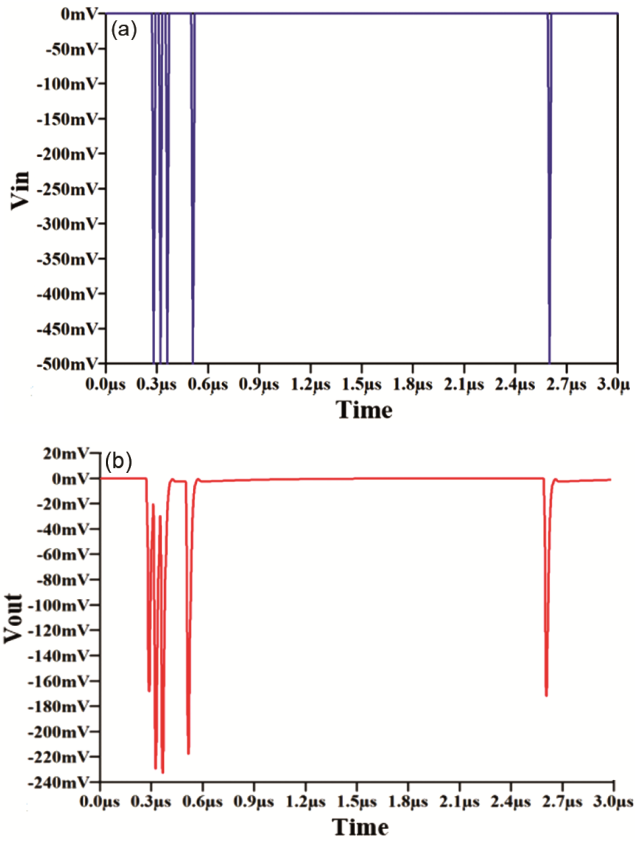

Fig. 16 — Responses of adaptive learning circuit employing (a) Input voltages (V_{in}), and (b) output voltages (V_{out})

can be analyzed that the circuit's initial response is low (around -160 mV). However, after training with 3 consecutive pulses applied at equal intervals, the response strengthens (around -210 mV).

Over time, the circuit begins to "forget", and its response strength diminishes, returning to the original value. The adaptive learning circuit's tuning with the input voltage signal (V_{in}) is due to change in memcapacitance value as the input signal value changes.

Table 1 illustrates that most existing meminductor and memcapacitor designs rely on multiple active blocks, numerous passive components, and often require additional elements such as memristors or multipliers. In contrast, our proposed circuits stand out by utilizing only a single active block, a few MOSFETs, and two capacitors.

Furthermore, our proposed design surpasses others by offering both meminductor and memcapacitor outputs through a slight reconfiguration — a feature rarely found in existing architectures, which typically provide only one of the two outputs. Additionally, our circuits operate at remarkably high frequencies in the MHz range—performance levels that are generally not attainable in conventional designs.

7 Conclusion

This study introduces meminductor and memcapacitor mutator circuits employing a VD-DIBA, in combination with a memristor and a single capacitor. The design includes memristor implemented using CMOS technology. The resulting pinched hysteresis loops showcase the functionality of the proposed circuit across different frequencies. To verify performance, adaptive learning circuits are developed and assessed, affirming the effectiveness of the proposed emulators. In conclusion, the study suggests that the proposed design provides a straightforward and efficient solution compared to existing alternatives in literature.

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