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Design and characterization of a low-leakage, high-stability SRAM cell for IoT applications

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The typical memory for very large-scale integrated (VLSI) circuits has traditionally been static random-access memory (SRAM) because it has offered faster speeds compared to other alternatives. However, SRAM has been associated with a high-power consumption rate. Researchers have recognized the importance of lowering the power consumption of SRAM cells due to their critical role in memory architecture. This literature review has aimed to provide innovative and effective strategies for designing low-power SRAM cells. Several circuit topologies and methodologies have been introduced to compute stability, leakage current, delay, and power, and novel techniques for designing SRAM cells based on eight transistors (8T) have been proposed. SRAM has frequently been chosen over dynamic random-access memory (DRAM) because it has demonstrated faster speeds and lower power consumption. It has been named "static" because no modification or action, such as refreshing, has been required to maintain data intact. However, leakage current in SRAM has often increased and impaired its performance as technology nodes have been scaled down. Voltage scaling has been adopted as a solution to this issue, although it has also affected the stability and latency of SRAM. A separate (isolated) read port has been employed to enhance read stability, while a negative bit-line (NBL) write-aid circuit has been implemented to improve write capability. The suggested design has been compared to state-of-the-art work in terms of write static noise margin (WSNM), write latency, read static noise margin (RSNM), and other metrics. Future research has been directed toward exploring novel circuit topologies and methodologies to further enhance stability, reduce leakage current, and minimizes delay and power consumption. Researchers have also investigated the performance of SRAM cells at smaller technology nodes to develop new techniques for maintaining stability and performance at these scales. Additional efforts have been made to explore new approaches to voltage scaling and to develop methods that improve the read and write capabilities of SRAM cells.

Keywords: SRAM, Stability, Energy efficient, Power, High speed and low-power VLSI applications, IoT applications

1 Introduction

More than five decades have passed since the scaling of semiconductor process technology began. The catalyst that has been propelling the semiconductor industry is advancements in process technology. In response to growing customer demand for enhanced performance and functionality at reduced cost, a new process technology generation has been introduced by the semiconductor industry every two to three years during the past four decades[1]. All electrical systems, including mainframes, microcomputers, mobile phones, and other devices, heavily rely on memory. Energy-efficient CPUs are becoming essential due to the rising demand for portable battery-operated systems. The dimensions, weight, and battery life of these gadgets have an impact on their performance. The IC design community has been actively seeking out new approaches and methodologies that result in more power-efficient designs, which means significant reductions in power consumption for the same level of performance, as a result of serious reliability issues, rising design costs, and battery-operated applications. Every system design includes memory circuits, which greatly increase system-level power consumption as Dynamic RAMs, Static RAMs, Ferroelectric RAMs, ROMs, or Flash Memories.

System performance, reliability, and costs may all be considerably increased by reducing the power dissipation of memory. Due to the rise in popularity of notebooks, laptops, hand-held communication devices, and IC memory cards in recent years, RAMs have developed extremely quickly in terms of low-power, low-voltage memory architecture. To decrease power dissipation, a number of strategies are used, including power gating, the sleepy technique, and the

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design of circuits with power supply voltage scaling. A lower power supply voltage quadratically and exponentially lowers dynamic power and leakage power, respectively. However, scaling of the power supply reduces the noise margin. A lot of SRAM arrays are built around lowering the swing voltage and active capacitance. Gate leakage and sub threshold leakage current are the major causes of leakage currents in the sub-100 nm area. Technology with high dielectric constant gates reduces gate leakage current. To lessen sub threshold leakage current, dual Vt approaches and forward body biassing are employed. The operational current in sub threshold SRAMs is the sub threshold leakage current since the power supply voltage (VDD) is lower than the transistor threshold voltage $(Vt)^2$. Computer data storage, often called storage or memory, refers to computer components and recording media that retain digital data used for computing for some interval of time.

The main purpose of storage is that without a significant amount of memory, a computer would merely be able to perform fixed operations and immediately output the result[3]. There are two types of memories: volatile and non-volatile. In the storage array or core, the straightforward cell circuits are stacked in horizontal rows and columns to share connections. Word-lines are the horizontal lines that are exclusively driven from the external storage array, while bit-lines are the vertical lines that carry data into and out of the cells. For reading or writing, access is made to the row and column that have been specifically chosen in a cell. Either "0" or "1" can be stored in each cell. Read-Write Random-Access Memory (RW RAM) refers to the storage of data in flip-flop circuits or simply as charge on capacitors (RAM). Because the data is volatile, there is about an equivalent delay while reading or writing it. Read-Write memories store data in an active circuit, meaning that if the power source is stopped, the recorded data will be lost. Since Read-Write Random-Access Memory is frequently referred to as RAM, RWM is the obvious shorthand for this type of memory. This research proposes a novel SRAM cell with differential write and single-ended read capabilities for IoT applications. For enhanced stability and rail to rail voltage swing, the transmission gate is employed as an access transistor. The suggested SRAM cell's analysis of leakage power and stability at supply voltages ranging from 0.9V to 0.5V is contrasted with that of the current 5T and 6T SRAM bit cells at 32nm technology. The transistor stacking effect is employed to reduce the SRAM cell's leakage current. By separating the read line from the node that is responsible for the read disturbance problem, stability is increased[4]. This article explains the low-power 8T SRAM cell memory cell suggested design. In the suggested method, two PMOS transistors are used, one of which is linked to the node voltage Q and the other to the Qbar. the bit and bit bar lines' swing voltage must be eliminated. The swing voltage is reduced when the cell is operating, which lowers the dynamic power dissipation. A sequence of leakage current decreases occurs when the transistors go from being inactive to being active and vice versa thanks to the pre-charge voltage level approach, which uses an NMOS transistor as a resister and a PMOS transistor as a switch. The comparison's results demonstrate that the proposed 8T SRAM cell's read, write, and hold mode operation is superior to that of the 6T SRAM cell. This occurs regularly as a result of the increased static noise margins produced, which guarantee good bit cell write ability[5].

Several schemes have been proposed about the improved stability as well as energy efficient for SRAMs in present-day low power analysis. Following is a discussion about the work done in improved stability and energy efficient SRAMs. Since the speed of early days electronic system was very slow, because the speed of memory was not comparable to the processor speed. Hence the cache memory is used for enhancing the speed of overall system. Currently, on static random-access memory, the cache memory is built. SRAM cell count on a single chip for a domain-specific architecture (DSA) is reaching to hundreds of megabits. This is resulted in two crucial challenges. The first challenge is the increasing inefficiency in SRAM array size with the newest CMOS technologies while the second challenge is the static power dissipation due to various leakage current which flows from the higher power supply through the SRAM cell to the lower power supply[6].This necessitates the need to design SRAM with minimal leakage since this reduces static power dissipation significantly. One of the suggested solutions to the power dissipation problem is to scale back the power supply, but the reliability of the SRAM cell poses another challenge in this. Besides this, issues like data

stability, delay and high sensitivity to process variation[10] also contributes to overall performance of SRAM. Besides this, issues like data stability, delay and high sensitivity to process variation[10] also contributes to overall performance of SRAM.

Figure1 depicts the conventional 6T SRAM cell consisting of four NMOS (NM_4, NM_5, NM_6 and NM_7) and two PMOS (PM_3 and PM_4) transistors. At the scaled cell supply voltage, the 6T SRAM cell encounters several issues like stability, delay, high sensitivity to process variationetc.[11]. The SRAM cell stability is mainly affected by the strength of transistors which form internal latch and access transistors. Hence, the weak pull-up transistor of the internal latch and strong access transistor are required for maintaining the write ability, while a strong pull-down transistor of the internal latch and weak access transistor is required for read stability[12].During the write operation in the SRAM cell, the conventional 6T SRAM cell provides a poor write ability due to disturbance in the node voltage at the down scaled cell supply voltage[13].Several write assist techniques are known in the literature currently in use to improve the write capabilities of SRAM cells. Among them the popular ones are negative bit line, V_{DD} collapse, boosted V_{SS}, word-line boosting etc.[14]. The negative bit-line write assist circuit technique has been proposed by Y. H. Chen, *et al*.[15]. When the bit lines of SRAM cells are used with a negative voltage rather than with ground, the gate to source voltage (VGS) of the access transistors is increased as a result. Therefore, increasing the voltage increases the SRAM cell's access transistors' driving capacity without affecting the inside latch. However, in this technique, the bit-line capacitance has been increased by boosted capacitor which eventually increases the access time[16]. On the contrary, in V_{DD} collapse technique, proposed by E. Karl, *et al*. [17], the weakening of the internal latch during a write operation is performed for improving the write ability, but the reduction in cell supply voltage in the technique disturbs the stored node voltage, thereby resulting in data loss during read or hold operation. In boosted word-line write assist technique[18], the word-line voltage is increased which also increases the gate to source voltage of access transistors, thereby increasing the static power dissipation. As a result, this method is likewise not appropriate for low voltage operation. In addition to this, attempts were also made by B. Wang, *et al*. [19] proposing ultra-low voltage 9T SRAM cell (9T UV SRAM), M. H. Tu, *et al*. [20], A. Banerjee, S. Kamineni and B. H. Calhoun [21] etc. to reduce the static power dissipation and for improvement of read/write operation. However, the results obtained are not promising.

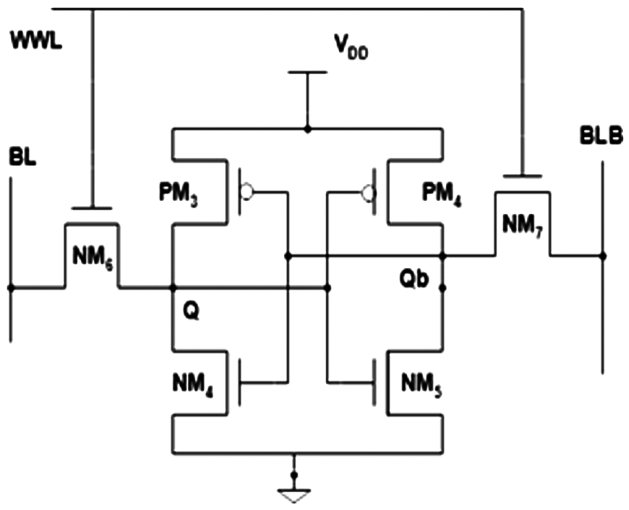

Fig. 1 — Conventional 6T SRAM cell.

a. To address stability and delay difficulties in SRAM, a unique negative bit-line (NBL) circuit is proposed then put into action using an 8T SRAM cell.
b. In the recommended architecture, one of the bit lines produces a negative voltage during the write operation (due to the NBL circuit), which enhances the access transistors' driving capacity and, as a result, the writing ability.
c. To increase the cell's stability during read operation, a separate or isolated read port is employed.
d. As a consequence, the suggested improvement has improved SRAM's stability and decreased its latency.

The recent literature review on designing low-leakage, high-stability SRAM cells for IoT applications focuses on the challenges associated with scaling down SRAM technology nodes. The study identifies leakage current and voltage scaling as the major concerns that need to be addressed to reduce power consumption in SRAM cells. The literature review also highlights the importance of designing SRAM cells that have high stability, low latency, and low power dissipation. Several circuit topologies and methodologies have been proposed in recent literature to address the challenges of reducing power consumption in SRAM cells. One such methodology

is the use of negative bit-line (NBL) write aid circuit to improve write capability. This methodology has been found to increase write stability and reduce write latency. Another proposed topology is the use of a separate (isolated) read port to increase read stability. This approach has been found to improve read stability and reduce read latency. The literature review also highlights the importance of considering multiple factors such as static noise margin, read and write latency, and power dissipation while designing low-power SRAM cells. The study suggests that the choice of which factor to optimize depends on the specific application and requirements of the SRAM cell.

2 Materials and Methods

2.1 Proposed 8T SRAM Cell

The following is a description of the proposed design:

2.1.1 Negative bit-line generator circuit(NBL)

The problem being addressed in this study is the high-power consumption and degradation of performance of SRAM cells due to the rising leakage current as technology nodes are scaled down. Voltage scaling has been proposed as a solution to this problem, but it can also impact the stability and latency of SRAM. Therefore, the goal of this study is to design and characterize a low-leakage, high-stability SRAM cell for IoT applications. The specific challenges include reducing leakage current, minimizing delay and power consumption, and improving read and write capabilities of the SRAM cell.

Mathematical Approach: This study employs circuit topologies and methodologies to compute stability, leakage current, delay, and power consumption. The design of the SRAM cell is based on eight transistors (8T), and performance metrics such as write static noise margin (WSNM), write latency, and read static noise margin (RSNM) are used to evaluate the effectiveness of the proposed design. A separate (isolated) read port is used to increase read stability, while a negative bit-line (NBL) write aid circuit is employed to improve write capability. The performance of the proposed design is compared to state-of-the-art work in terms of these metrics. Applying a negative voltage to one of the bit lines (BL or BLB) of the SRAM cell decreases the gate to source voltage (VGS) of the access transistor in the proposed circuit. The major function of the NBL circuit is to deliver a negative voltage instead of 0 V at the BL/BLB of an SRAM cell, depending on the operating conditions.

The suggested NBL generator circuit is depicted in Fig. 2 and is constructed utilizing four NMOS, three PMOS, and two NOR gates. The NOR gate's inputs in the NBL circuit are the Din, Dinb, and WR signals, while the NOR gate's output is connected to the inputs of the NMOS and PMOS transistors.

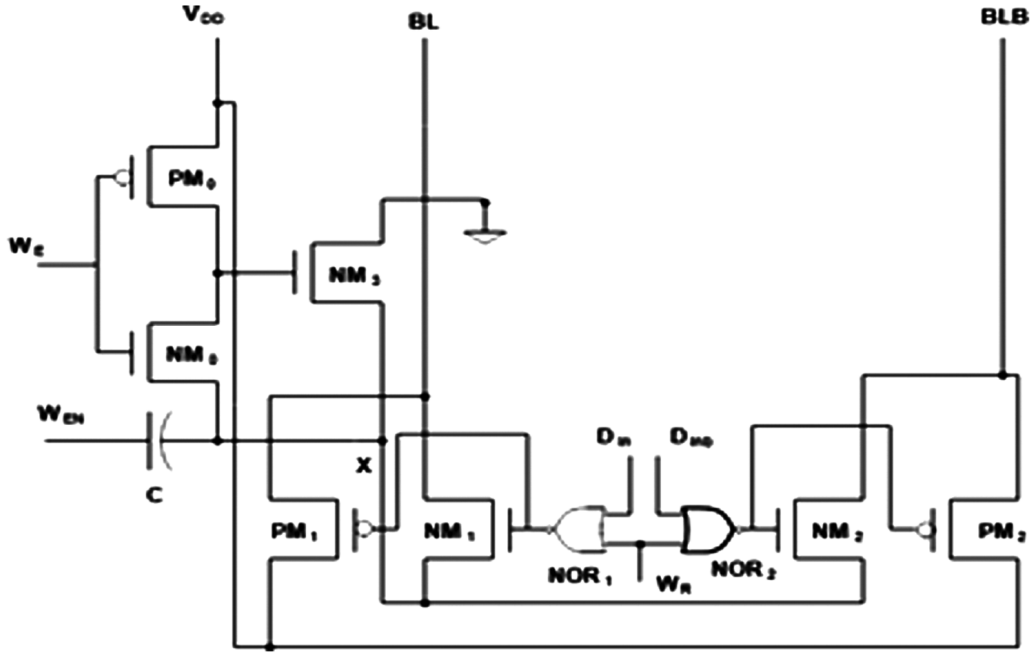

Fig. 2 — Circuit of negative bitline generator (NBL)[22].

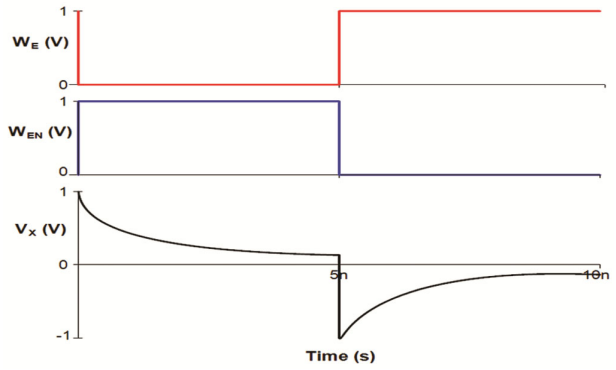

Fig. 3 — Output voltage at nodeX (NBL)[22].

The NBL circuit performs the following operations:

Case 1: NBL circuit in write mode when logic "1" is used. While applying logic levels "1" and "0" respectively, to the Din and Dinb signals, logic level "0" is applied to WR in a write logic "1" operation. Inverted Din and Dinb signals are always the NOR gate's output signals. As a result, NOR1 and NOR2 output "0" and "1" respectively. Transistor NM1 would turn to an OFF state, and NM2 would go into an ON state. Transistor PM1 would also be ON and PM2 would be OFF in addition to this. As a result, the bit-line (BL) would change to logic high (VDD), and the bit-line bar's (BLB) state would rely on two additional scenarios related to the status of the WE and WEN sign

Case A: The WEN signal's counterpart logic "1" is applied when the WE signal is at logic "0" as shown in Fig. 3. As a result, the transistor NM0 is turned off by the WE signal, and the transistor PM0 is turned on, which then turns on the transistor NM3. The triode region in which the ON transistor NM3 works provides a resistance across it. The RC network is made up of a capacitor (C) and the transistor NM3 (RON) resistance (the circuit works as a RC differentiator).Because the WEN signal (at the starting point) is a rising pulse and the slope at the positive edge is particularly large, the capacitor acts as a short circuit, the input voltage (the voltage of the WEN signal) and the voltage at node X (the voltage across the RON or VX) are equal at this point. When the WEN signal reaches logic "1" after the positive edge, the capacitor starts to charge through resistance RON. As a result, until the capacitor is fully charged, the voltage at node X or VX quickly decreases as shown in Fig. 3.charging of capacitor depends on time constant RONC. As a result, in this circumstance, the voltage at BLB and VX are equal.

Case B**:** The WEN signal's counterpart, logic "0" is applied when the WE signal is at logic "1" As a result, the transistor PM0 is turned off by the WE signal, while the transistor NM0 and NM3 are turned on (because capacitor does not allow the sudden change in voltage thus the gate of NM3 is connected to node X through NM0 transistor). An RC network is created in a manner similar to scenario A. The negative edge of the WEN signal has a very steep slope, and since the WEN signal is a falling pulse, the capacitor does not react well to steep slopes. As a result, a negative spike develops at this point. The capacitor discharges when the WEN signal reaches logic "0" following a negative edge. As the capacitor drains, the voltage at node X or VX increases exponentiallyas seen in Fig. 3. discharging of capacitor also depends on time constant RONC. As a result, in this instance, the voltage at BLB is also equal to the negative voltage, or VX voltage.

Case II: When writing logic "0" the NBL circuit. The Din and Dinb signals are respectively, at logic levels "0" and "1" the logic "0" is applied to WR in order to perform a write logic "0" operation. The output signals of the NOR1 and NOR2 gates are, respectively, at logic "1" and "0" Transistor NM1 would go to the ON state, whereas NM2 would go into the OFF state. Additionally, transistors PM1 and PM2 would be ON and OFF respectively. As a result, the bit-line bar (BLB) would change to logic high (VDD), and the bit-line (BL) state would likewise rely on the WE and WEN signal states for the additional two instances A and B as mentioned for scenario I. As a result, when WEN is set to logic "0" the bit-line (BL) receives a negative voltage.

Case III**:** The NOR gate would always produce a zero output during a read and hold operation, which would then activate the PMOS (PM1 and PM2) and deactivate the NMOS (NM1 and NM2) transistors. The WR signal is always at logic "1" during a read and hold operation, hence the NOR gate would always output zero regardless of Din and Dinb values. The PMOS (PM1 and PM2) transistors are used to link the BL or BLB and VDD. The aforementioned Cases A and B have no impact on the read and hold operation since the NMOS (NM1 and NM2) transistors are in the OFF state and the node X disconnects from the bit-lines (BL/BLB). Since the bit-lines (BL/BLB) are switched to VDD during read

and hold operations, the proposed NBL circuit provides a negative voltage at one of the bit-lines (BL/BLB) during the write operation.

2.1.2 Proposed design (NBL circuit with 8T SRAM cell)

The proposed design (PD), which implements an NBL circuit with an 8T SRAM cell, is shown in Fig. 4. There are eight transistors in an 8T SRAM cell. The SRAM's internal latch, where the data is kept, is built using the transistors NM4, NM5, PM3, and PM4. The separate read port for accessing data from the SRAM cell is formed by transistors NM8 and NM9. The data-storing nodes of an SRAM cell are node Q and node Qb. While transistor NM9 functions as an access transistor during read operation and is triggered by the read word line (RWL) signal, transistors NM6 and NM7 function as write access transistors. The read bit line (RBL) functions as an input/output line under read operation, whereas the bit lines (BL/BLB) function as an input for write operation.

The following is a discussion of the different operations of the proposed design:

2.1.2.1 Write operation

Figure 5 shows the circuit's behavior during write operations. In this instance, a dotted line represents an OFF transistor. The WWL signal is given the write operation logic "1" which activates the access transistors NM6 and NM7. Write logic "1" for at node Q. The nodes Qb and Q, respectively, are initially where logic "1" and "0" are stored.

1. At the nodes Qb and Q, respectively, logic "1" and "0" are initially stored.
2. BL and BLB are given the logic values "1" and "0" respectively.

In the suggested architecture, the NBL circuit is linked to the bit-lines. The WR signal is at logic "0" for write operation in the NBL circuit, whereas the Din and Dinb signals are at logic "1" and "0" respectively. As a result, the BLB is driven at negative potential while the BL is driven at VDD as discussed in section 3.1

The negative voltage at the BLB causes the gate to source voltage (VGS) of the access transistor (NM7) to rise, which in turn raises NM7's driving capacity. Due to node Qb being forced to discharge quickly and acquire 0V as a result of transistor NM7 acting much faster than transistor NM6 in Fig. 5, transistor PM3 is turned ON and transistor NM4 is turned OFF.

Thus, transistor PM3 connects the storing node Q to the supply voltage (VDD), whereupon the logic "1" is afterwards stored.

2.1.2.2 Read operation

Figure 6 shows the circuit behavior of the proposed design (with the OFF transistor shown by the dotted line) during a read operation.

The output of the NOR gate would always be at a low voltage, activating the PMOS, because the WR

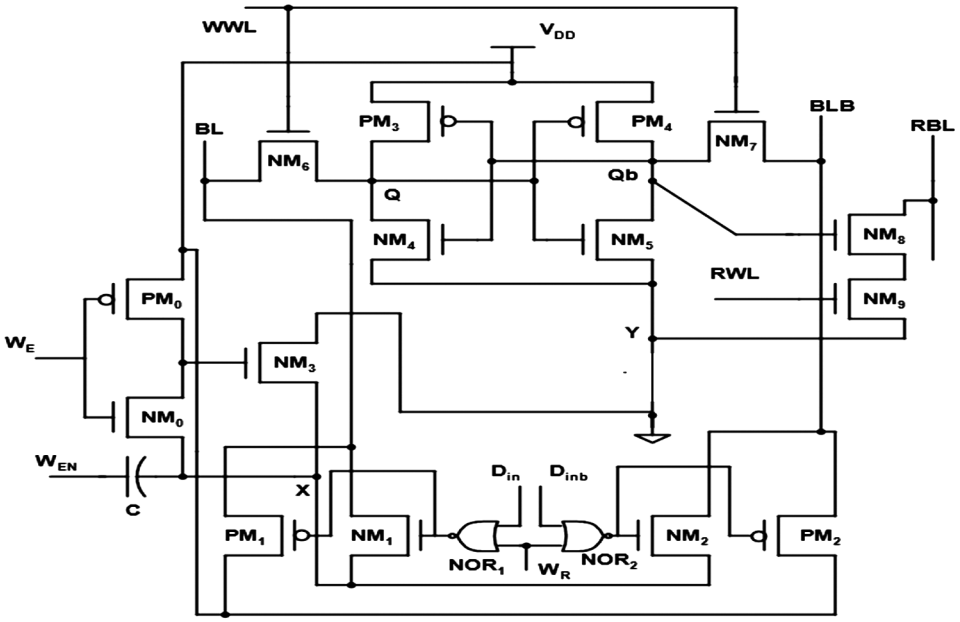

Fig. 4 — Proposed 8T SRAM cell Design with NBL.

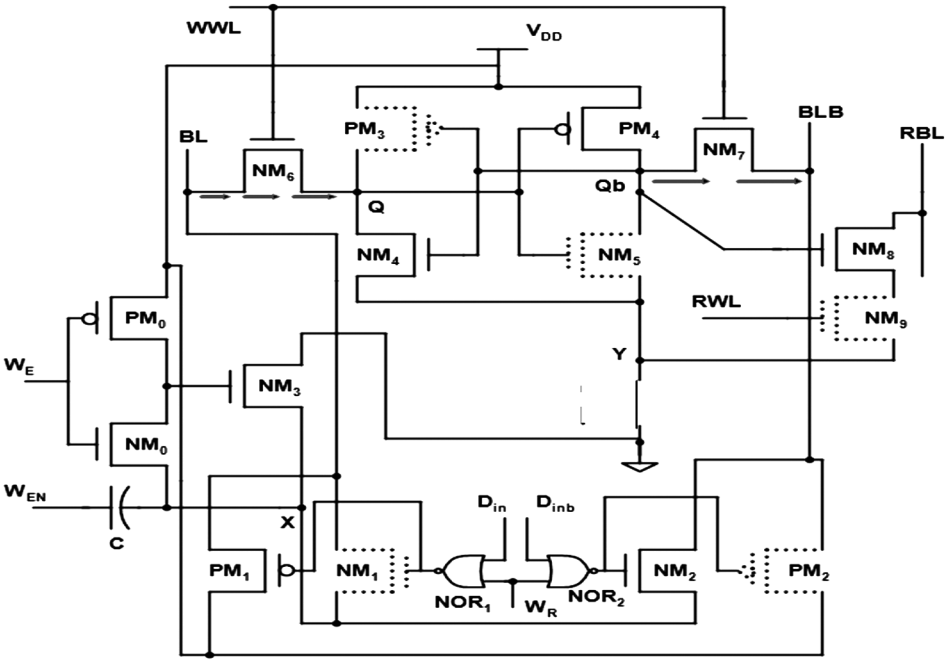

Fig. 5 — Proposed 8T SRAM cell design with NBL during a write operation.

must always be at logic "1" in order to read data from the SRAM cell. As a result, the bit lines (BL or BLB) have always been set to logic "1". During a read operation, RBL is pre-charged at logic "1" the WWL signal is at logic "0" RWL is at logic "1" and so on. Assume initially that nodes Q and Qb are where logic level "0" and "1" are kept for read logic "0" operations. The transistor NM8 turns ON owing to logic "1" stored at node Qb, which is coupled to the transistor NM8's gateas illustrated in Fig.6. With the help of transistors NM8, and NM9, a route depicted by an arrow is created between RBL and ground. Thus, as seen in Fig. 6, the RBL is discharged to 0 V. The read logic "0" operation has therefore been carried out.

2.1.2.3 Hold operation

The access transistors NM6, NM7, and NM9 are turned off as a result of the RWL and WWL being maintained at logic "0" during the hold operation. The BL, BLB, and RBL are constantly at logic "1" because the WR in the NBL circuit is always at logic "1" The internal latch of the SRAM cell is disconnected from the bit-lines in hold mode of operation, preserving the data stored inside. A large amount of static power was also lost by the SRAM cell during the hold mode due to leakage current, mostly sub-threshold leakage current because the bulk of the transistors are still in the OFF state. Consequently, the suggested design reduces static power dissipation. The NM9 transistor Y node generates a positive voltage as a result of self-reverse biassing. This positive voltage lowers the drain to source (VDS) and gate to source (VGS) voltages of OFF transistors (NM5 and NM9) while raising their threshold voltages (NM5 and NM9).

3 Results and Discussion

The performance of the given design has been predicted using the cadence virtuoso tool for circuit design and simulation utilizing the UMC 28 nm CMOS technology node. The following are the simulated findings for the proposed design's different performance parameters:

3.1 Write ability

The stability of the SRAM cell is defined as the greatest noise voltage that cannot flip the state of the storing node in the SRAM cell. Write static noise margin (WSNM), which is acquired via a sweeping approach, serves to define the SRAM's write capability. This technique sweeps the voltage at one node (Q) from zero to the supply voltage (VDD), then plots it against the analogous voltage at another node (Qb) to get the voltage transfer characteristic curve (VTC).

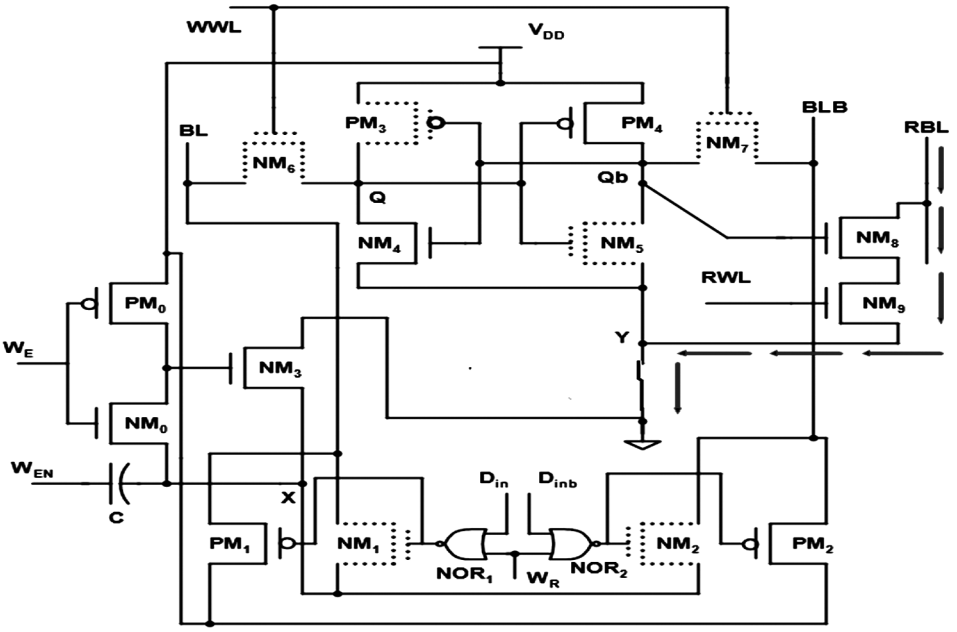

Fig. 6 — Proposed 8T SRAM cell design with NBL during a read operation.

The process is then repeated, but this time to generate a comparable graph to the analogical VTC at node Q, the voltage at node Qb is swept from 0 V to the maximum supply voltage (VDD). Last but not least, the two VTC curves are blended into a graphic called a butterfly plot. The butterfly plot, in which a square is produced and the longest vertical side is taken into account as the WSNM value, determines the WSNM[24]. Figure 7 illustrates the butterfly curve of the suggested design for calculating the write-operational WSNM value at 1 V cell supply voltage and 27°C temperature with TT corner.[24] When compared to an 8T SRAM cell without an NBL circuit, the suggested design's WSNM is 490 mV. Since the 8T SRAM cell with the NBL circuit improves the WSNM value by 1.53x over the SRAM cell without the NBL circuit, it is preferable to have this feature included.

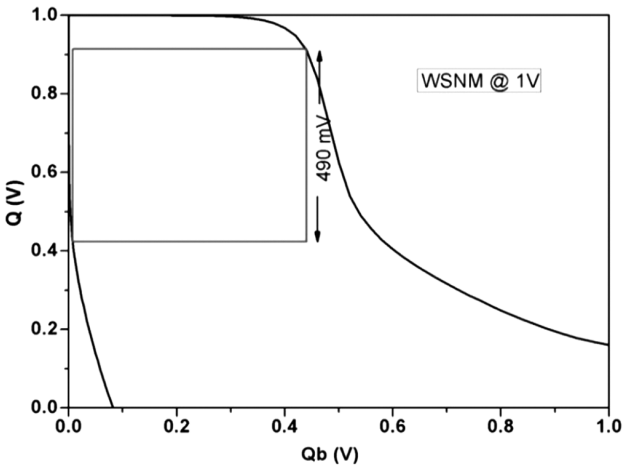

Fig. 7 — Butterfly curve for write stability.

Figure 8 shows the comparison of the proposed design with the standard 6T SRAM cell, the VDD collapse write assist approach, the NBL write help technique, and the 9T UV SRAM cell at various cell supply voltages. Because there is a significant likelihood of flipping the data of SRAM cells at lower supply voltages, it has been shown that WSNM rises with supply voltage. As a result, the cell is less stable at lower supply voltages than it is at higher supply voltages. Additionally, when developed at 1 V supply voltage using the same technology node, the WSNM of the suggested design is improved by 48%, 11%, 19%, and 32.4% over basic 6T SRAM cell, NBL, VDD collapse, and 9T UV SRAM, respectively. This increase was made possible by a negative bit-increased line's ability to boost the access transistor's VGS.

The WSNM of the suggested design is shown in Fig. 9 at various temperatures. When the temperature rises from -40°C to 120°C at 1V supply voltage, it can be shown that the WSNM value of the suggested design falls from 580 mV to 430 mV. This is due to the threshold voltage decreasing with temperature. As a result, the SRAM cell's data values deteriorate. So, at high temperatures, the SRAM cell is less stable. Comparing the suggested design to the basic 6T and

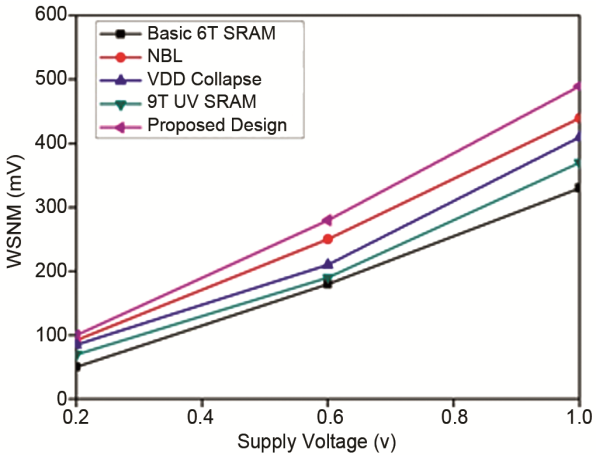

Fig. 8 — Variation in WSNM versus supply voltage.

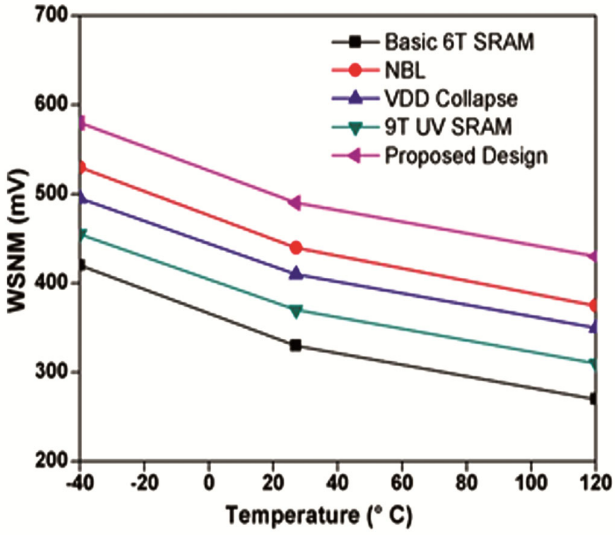

Fig. 9 — Variation of WSNM versus temperature.

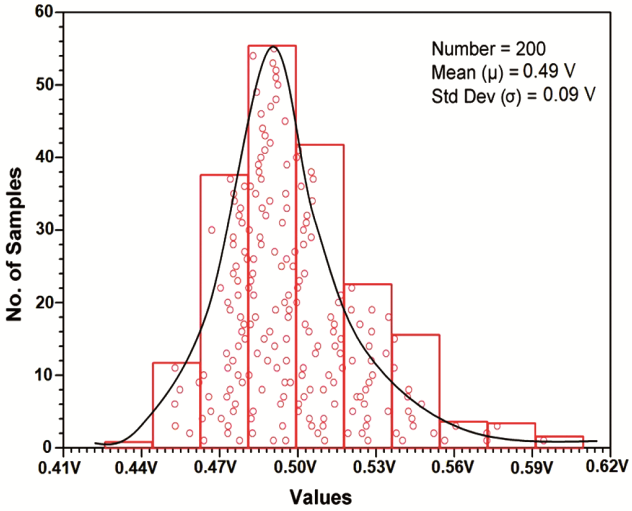

Fig. 10 — Monte Carlo of WSNM for proposed design.

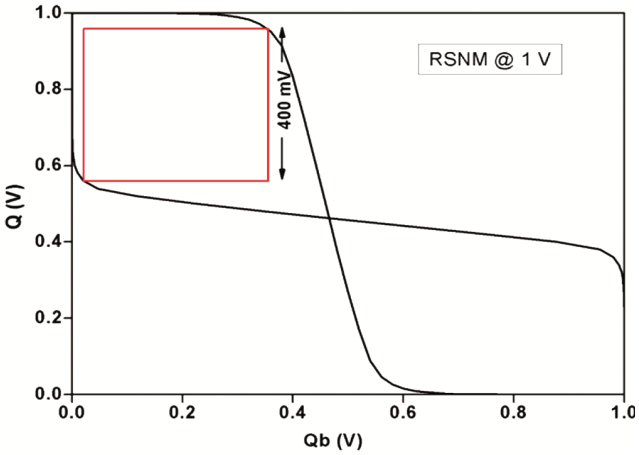

Fig. 11 — Butterfly curve for the read stability.

other current designs, as shown in Figure 9, the proposed design exhibits nominal performance in terms of WSNM even with the increase in temperature.

The yield of the suggested design has been determined and validated using a Monte Carlo simulation for process variation and mismatch. For transistor parameters that are normally distributed and uncorrelated, the Monte Carlo simulation approach replaces the fixed Gaussian distribution with a random value. The simulation result for WSNM demonstrates that the proposed design is lesser sensitive to mismatching and process variations as standard deviation (σ) is only 0.09V as depicted in Fig. 10 when 200 number of samples have been considered for the analysis. The mean value (μ) of proposed design is 490 mV whereas the variability (σ/μ) is 0.18.

3.2 Read stability

The read stability of the SRAM cell is defined through the read static noise margin (RSNM), which is also obtained using the butterfly plot [26]. The butterfly curve for the read stability in the read operation is shown in Fig. 11. The greatest side length of the square produced inside the smaller lobe of the butterfly curve is used to evaluate the proposed design's RSNM value. It should be noted that the suggested design's RSNM value is 400 mV at 1 V for the cell supply voltage. The fluctuation in RSNM values for the proposed design and prior published studies at various cell supply voltages are shown in Fig. 12. The RSNM is very low at the lower supply voltage, and as the voltage rises, the RSNM likewise rises. It can be noticed that there is an enhancement in RSNM of proposed design by 81%, 42%, 29%, over

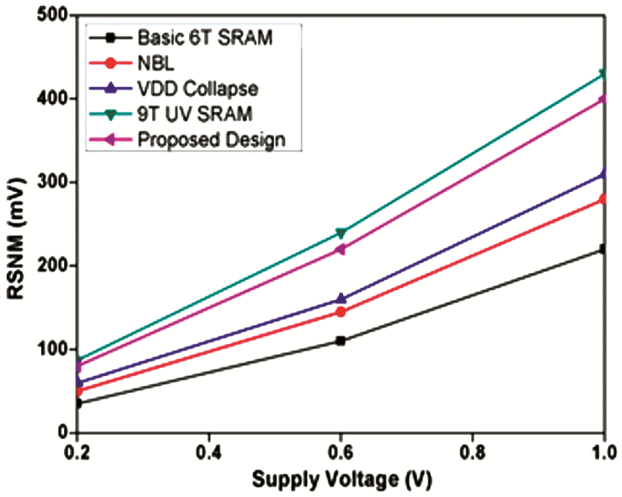

Fig. 12 — RSNM versus supply voltage.

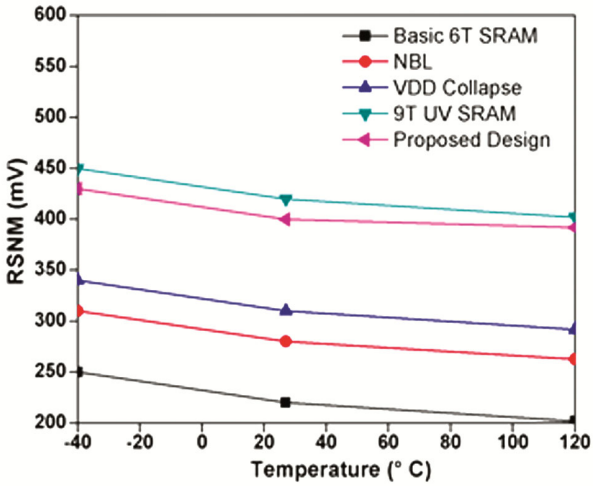

Fig. 13 — Variation of RSNM versus temperature.

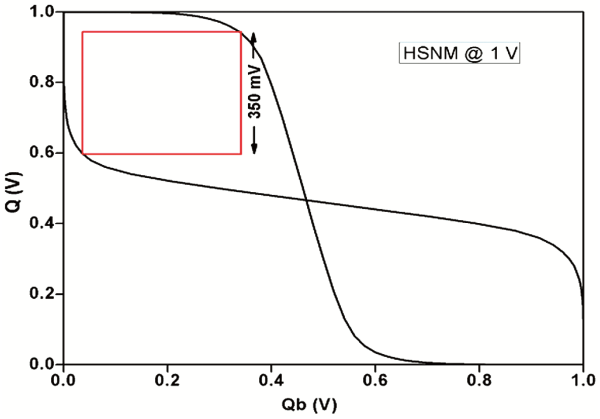

Fig. 14 — HSNM of proposed design.

basic 6T SRAM cell, NBL, V_{DD} collapse respectively, whereas decrement by 4.8% over 9T UV SRAM when designed at 1 V supply voltage using same

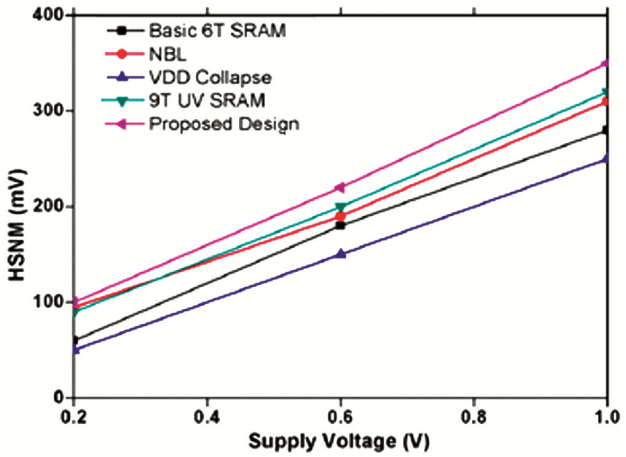

Fig. 15 — Variation of HSNM versus supply voltage.

technology node. In the suggested architecture, a dedicated or isolated read port is used to accomplish this increase in RSNM. The WWL signal is at logic "0" during the read operation, isolating the storage nodes from the bit-lines (BL/BLB). As a result, there has been no disruption or degradation of the data held in nodes (Q/Qb). As a result, the suggested design is quite stable when being read. The RSNM value of the suggested design is shown in Fig. 13 at various temperatures. Due to the lower threshold voltage of transistors when temperature rises, the suggested design's RSNM value lowers. Additionally, Fig.13 compares the suggested architecture to different SRAM designs. It is clear that the suggested design delivers the best results for read operation at a specific temperature.

3.3 Hold Stability

Hold static noise margin is used to measure the SRAM cell's stability in hold mode (HSNM). This is possible using the butterfly plot, as seen in Fig. 14, it has also been highlighted that the HSNM value of the proposed design is 350 mV at 1 V for the cell supply voltage. At various cell supply voltages, Fig. 15, compares the HSNM value of the proposed design to that of other current designs. In the hold mode of the proposed architecture, the internal latch is isolated from the bitlines. As a result, there is no data loss and the SRAM cell is more stable in hold mode. Also, it can be noticed that there is an enhancement in HSNM of proposed design by 28%, 13%, 40%, and 8.5% over basic 6T SRAM cell, NBL, V_{DD} collapse and 9T UV SRAM respectively when designed at 1 V supply voltage using similar technology node. The HSNM of the suggested design is shown in Fig.16, at various

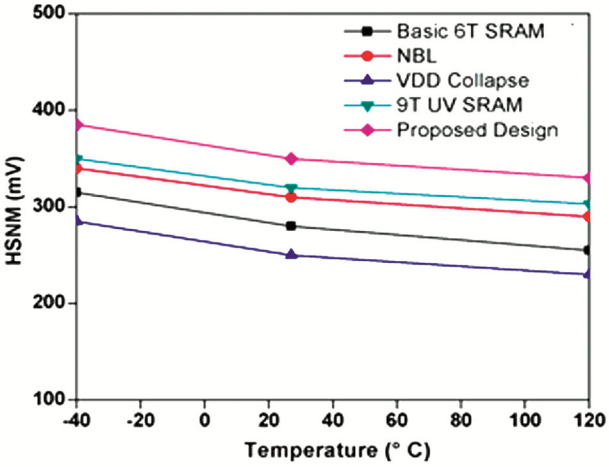

Fig. 16 — Variation of HSNM versus temperature.

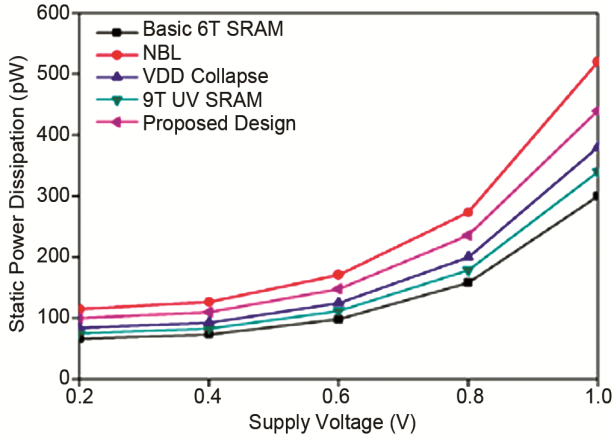

Fig. 17 — Static power dissipation at various cell supply voltage.

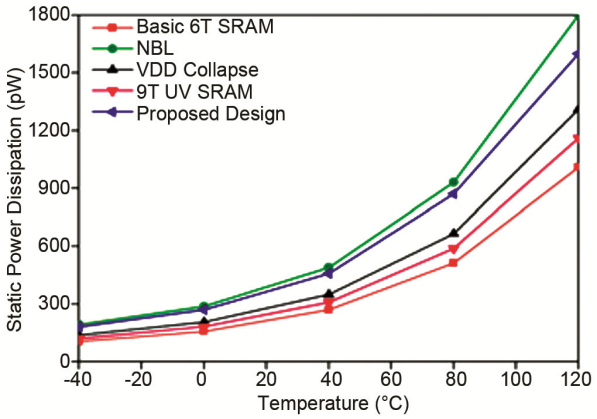

Fig. 18 — Variation of static power dissipation versus temperature.

temperatures. It has been noted that the HSNM value of the suggested design, when operating at 1V cell supply voltage, reduces when temperature increases from -40°C to 120°C. Additionally, a comparison of the suggested architecture with a standard 6T SRAM cell and other cutting-edge work is shown. This may be used to show that the proposed design's HSNM performs better than alternative designs at different temperatures.

3.4 Static power dissipation

At lower technology node SRAM cell also faces the issue of static power dissipation. The numerous leakage currents in a circuit are the major cause of static power dissipation. The leakage current includes sub-threshold leakage current, junction leakage current, gate leakage current, and so on [27]. Figure 17, displays the dynamic power dissipation of the proposed architecture at different cell supply voltages. The static power dissipates more when the cell power supply is increased. The recommended design's static power dissipation is 430 pW at a cell power supply of 1 V. (190 pW by an 8T SRAM cell and 240 pW by an NBL circuit). The suggested design has been compared to other state-of-the-art work as well as a simple 6T SRAM cell. This can be noticed that the proposed design consumes 30%, 11% and 20% more power than 6T SRAM cell, V_{DD} collapse and 9T UV SRAM respectively while 17% less than NBL, at 1V cell supply voltage. Due to the NBL circuit's usage of just one SRAM cell, the suggested design has a little higher static power dissipation than usual. However, by combining a single NBL circuit to several SRAM cells, static power can be reduced. The fluctuation in static power dissipation at various temperatures is seen in Fig. 18, Because the sub-threshold leakage current exponentially relies on the temperature and threshold voltage, the suggested device loses power as the temperature rises. As the temperature rises, the threshold voltage falls, increasing the sub-threshold leakage current. As a result, the suggested design loses more static power.

3.5 Write delay

The amount of time needed to write data at storage nodes (Q/Qb) is computed as the time interval starting when the WWL signal reaches 50% of its highest value during the write operation. At a 1 V cell power supply, the suggested design's write latency is 140 ps. The write delay of the suggested design at various cell supply voltages is shown in Fig. 19, along with a comparison to other existing SRAM. This can be detected that the write delay of proposed design is reduced by 33%, 39%, 48%, and 22% when compared to 6T SRAM cell, NBL, V_{DD} collapse and 9T UV SRAM respectively at 1 V supply voltage.

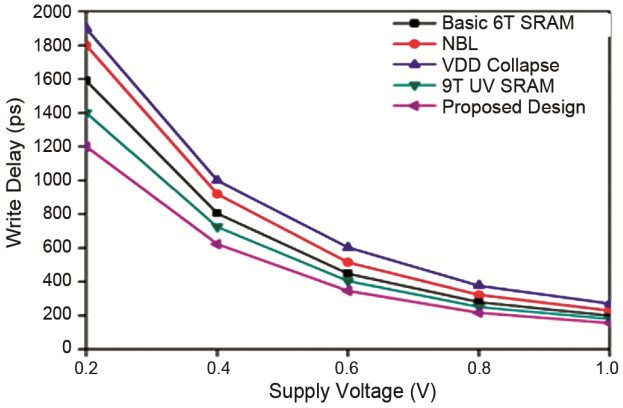

Fig. 19 — Variation of write delay versus supply voltage.

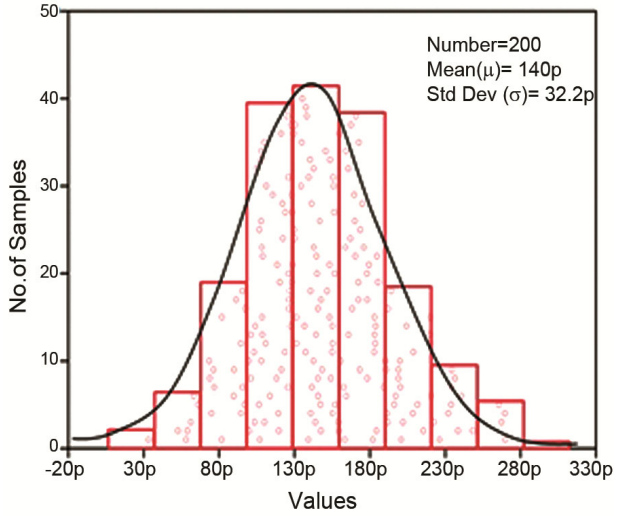

Fig. 20 — Monte Carlo of write delay for proposed design.

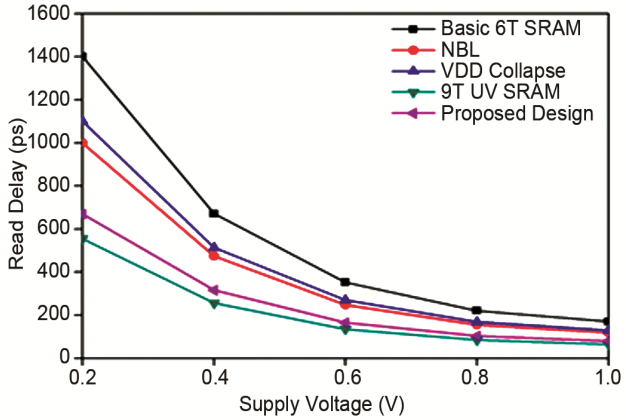

Fig. 21 — Variation of read delay versus supply voltage.

Since the source of the access transistor is at a negative voltage during a write operation, the write latency is reduced thanks to the high driving capabilities of the access transistor. The cross coupled inverter state is flipped as a result of the node storing logic "1" discharging relatively quickly, making it simple to send data to the storage nodes. Additionally, a Monte Carlo study of the suggested design's write latency was completed and is shown in Fig. 20, For 200 samples, the standard deviation and mean write delay values are 32.2 and 140 ps, respectively, with a variability of 0.26.

Table 1 — Read and write power at different supply voltages.

Supply Voltage (V)	Read Power	Write Power
0.2	59 nW	278 nW
0.4	505 nW	1.39 uW
0.6	2.16 uW	4.22 uW
0.8	6.4 uW	11.82 uW

3.6 Read Delay

The period of time between the RWL signal being triggered and the RBL signal discharging to 50% of its highest value is known as the calculated read delay. At a 1 V cell power source, the suggested design's read latency is 80 ps. The read latency of the suggested design at various voltages is shown in Fig. 21. This can

be detected that the read delay of proposed design is reduced by 52%, 33%, and 38% while increased by 18% when compared to basic 6T SRAM cell, NBL, V_{DD} collapse and 9T UV SRAM respectively. Using an isolated read port for read operation allows for this decrease in read t

3.7 Dynamic power dissipation

The SRAM cell's dynamic power dissipation may be measured while it is used in write and read mode. The suggested design's write power is raised due to the NBL circuit's rise in gate to source transistor voltage, which causes access and pull-down transistor current to increase. The proposed design's read power, however, is minimal. Table 1, displays the dynamic power dissipation of the proposed architecture, including parasitic components, during read and write operations at various cell supply voltages.

Table 1 shows the read and write power of the SRAM cell at different supply voltages. As the supply voltage increases, both the read and write power also increase. At a supply voltage of 0.2V, the read power is 59nW and the write power is 278nW. At a supply voltage of 1.0V, the read power is 12.5uW and the write power is 26.3uW. It

is important to note that the write power is higher than the read power at all supply voltages, indicating that write operations consume more power than read operations.

4 Conclusion and Future Scope

Since low power integrated circuits are widely used in portable electronic devices, their necessity is well understood. Static Random Access Memory (SRAM) on the SoC (System on Chip) controls both the speed and power consumption of the device. Therefore, having low power SRAMs is crucial. We have been reducing the size of CMOS devices for more than 50 years in order to make them portable, small, and to achieve superior performance in terms of access time, power consumption, latency, etc. As a result, there is a greater need for memory that is small and low-powered. Working on low supply voltage and energy leakage has become a top priority since there is a lot of room for power consumption reduction. The oxide thickness and operating voltage continue to drop as IC manufacturing technology scales. Lower operating voltage will reduce the SRAM cell's stability, resulting in a lower static noise margin value. Certain essential factors, including static noise margin, read and write latency, static power dissipation, etc., regulate the SRAM cell. Designing an SRAM cell that performs better while taking into account all of the aforementioned characteristics at once is difficult. The designers have always had to make concessions in order to improve certain criteria at the expense of others. The necessity and application of the SRAM will determine which characteristics must be increased and which parameters can be compromised. This study offers a negative bit-line (NBL) write assist circuit for increasing the write stability of SRAM cells and a separate (isolated) read port for improving the read stability in order to increase stability and speed. In terms of write static noise margin (WSNM), write latency, read static noise margin (RSNM), and other factors, the suggested design has been compared to previous state-of-the-art work. When designed with a 1 V cell supply voltage, it has been shown that the WSNM has improved by 48, 11%, 19%, and 32.4%, while the write latency has decreased by 33%, 39%, 48%, and 22% when compared to standard 6T SRAM cell, NBL, VDD collapse, and 9T UV SRAM, respectively. In conclusion, the design and characterization of a low-leakage, high-stability SRAM cell for IoT applications is crucial for the development of portable electronic devices. This study proposes a negative bit-line (NBL) write assist circuit and a separate (isolated) read port to improve the write and read stability of the SRAM cell, respectively. The suggested design has been compared to previous state-of-the-art work, and it has been shown that the WSNM has improved significantly, while the write latency has decreased. The future scope of this study includes further optimization of the proposed design to achieve even better results in terms of power consumption, stability, and performance.

5 Conflicts of Interest

There are no material financial or non-financial interests to report for the authors.

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