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Design and characteristics exploration of an InAs-source-based electrostatic doped vertical nanowire TFET

Anjana Bhardwaj[a], Amit Das[b]*, Shivani Yadav[c] & Yuvika Dhillon [d]

[a]Department of ECE, GLA University, Mathura 281406, Uttar Pradesh, India

[b]Department of ECE, Indian Institute of Information Technology Guwahati, Guwahati 781015, Assam, India

[c]Department of Electronics and Communication Engineering, Krishna Institute of Engineering & Technology (KIET), Ghaziabad 201 206, Uttar Pradesh, India

[d]Department of Electronics and Communication Engineering, School of Engineering and Technology, CGC University, Mohali 140307, Punjab, India

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In this manuscript, the nanotube structure with vertical architecture and an indium arsenide-based source has been proposed. In the proposed device, the electrostatic doping (ED) has been applied to eliminate the doping ambiguities like expensive thermal budget (ETB) and random dopant fluctuation (RDF). RF and analogue metrics, including transconductance (g_m), drain current (I_D), output conductance (g_d), output characteristics (I_D–V_{DS}), cut-off frequency (f_T), and gate capacitance (C_{GG}), have been utilized to analyze the device characteristics. The structural parameters of the device, like energy band, electric field, potential, and carrier concentration,have also been investigated. The InAs-based source electrostatic-doped VNW-TFET (InAs-S-ED-VNW-TFET) has shown better performance than the conventional or Si-based source VNW-TFET (Si-S-ED-VNW-TFET) due to its higher mobility, lower bandgap, and lower effective mass, resulting in a higher tunneling rate. With the inclusion of electrostatic doping, uniform doping has been achieved throughout the device. The device has been optimized by achieving a steeper subthreshold slope of 19.8 mV/Dec., higher ON current 8.99μA/μm, and higher ON/OFF current ratio of 1.23×10^{13}.

Keywords: Dopingless transistor, InAs/Si interface, Indium arsenide source, Nanowire transistor, Silvaco TCAD, VNW-TFET

1 Introduction

Due to their inherent advantages over traditional CMOS devices[1], tunnel FETs (TFETs)[2,3] have gained popularity in recent years. MOSFETs[4] operate based on thermionic emission[5], whereas the PIN architecture of TFETs facilitates band-to-band tunneling (BTBT)[6], making them advantageous for the application of low-power[7]. This phenomenon allows TFETs to achieve a high I_{ON}/I_{OFF} ratio. The device InAs-S-ED-VNW-TFET (InAs-based source electrostatic doped vertical nanowire TFET) has been proposed in this paper[8,9]. It has been observed that the subthreshold slope average (AV_{SS}) of a conventional TFET is less than 60 mV/decade[10], the limitation imposed on conventional MOSFETs. However, the ON-current of TFETs is used to decrease as compared to FET devices due tothe inefficiency of tunneling. Performance-enhancing techniques, such as using low-bandgap materials like Ge and InAs on the source side[11], employing high-k dielectric materials[10–12], and dual-material gates[13,14], may help improve performance. Additionally, uniform doping remains a challenge during the fabrication process. The electrostatic doping approach can be used to address this issue[2,15]. In this method, the voltage is applied at the drain and source metal (used for the purpose of doping) to introduce the doping in the substrate. By the use of this technology, a reconfigurable doping can be achieved. Due to enhanced inversion of the surface, which enhances the drive current, the nanotube with a gate all around (GAA) structure provides a better ability to control the charge carriers. Furthermore, the device's overall area is smaller than that of conventional TFETs. The InAs-S-ED-VNW-TFET combines the advantages of the low-bandgap material InAs with the nanotube structure of the device[16,17]. The objective is to overcome the limitations of conventional and dopingless TFETs by achieving improved characteristics, such as a higher BTBT rate, a lower threshold voltage (V_t), and an enhanced ON-current (I_{ON}).

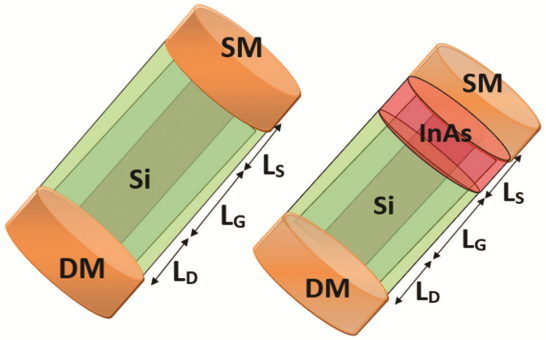
*Corresponding author (E-mail: amitofficial7492@gmail.com)

2 Materials and Methods

Figures 1 (a & b) show the three-dimensional structures of both the conventional Si-S-ED-VNW-TFET and the proposed device,InAs-S-ED-VNW-TFET. The channeland drain regions are formed from an intrinsic material of Si, which is 10 nm thick (diameter). The ED technique has been employed to create the region of drain and source in these dopingless devices. One of the devices, a Si source is used, while in the second device, material Si is being changed by the narrow-bandgap material InAs, with the drain side identical in both devices to achieve a low I_{OFF}.

Two extra metals are used in the device, one for drain-2 and another for source-2. To achieve the doping, a positive voltage (+1V) is supplied to drain-2, and a negative voltage (-1V) is connected to source-2. By this approach, a cloud of electrons is formed near drain-2 metal, and a cloud of holes is formed near source-2 metal. This technique also allows the doping in the device to be varied during operation, which is why it is also known as a reconfigurable device. In both architectures, the thickness of the gate oxide is kept at 1 nm. For optimized performance, the channel length for both configurations is 20 nm, and the oxide thickness, composed of SiO_2, between the intrinsic body and the metal contact is 1.5 nm. All parameter values are identical in the three-dimensional structures of both devices. The drain, source, and gate electrodes are made with aluminum having a work function WF of 4.2eV. A layer of SiO_2 surrounds these electrodes. Silvaco TCAD is used to simulate both devices. The spatial tunneling of charge carriersisutilized using the nonlocal BTBT model. Quantum models were also employed.

Since the InAs-source-based structure is showing better performance as compared to the Si-based structure, Fig. 1 (c) describes the steps required in the fabrication process[3,18,19]. To design the base of the nanowire, vertical cylindrical annulus etching is the first step in the creation of an InAs-S-ED-VNW-



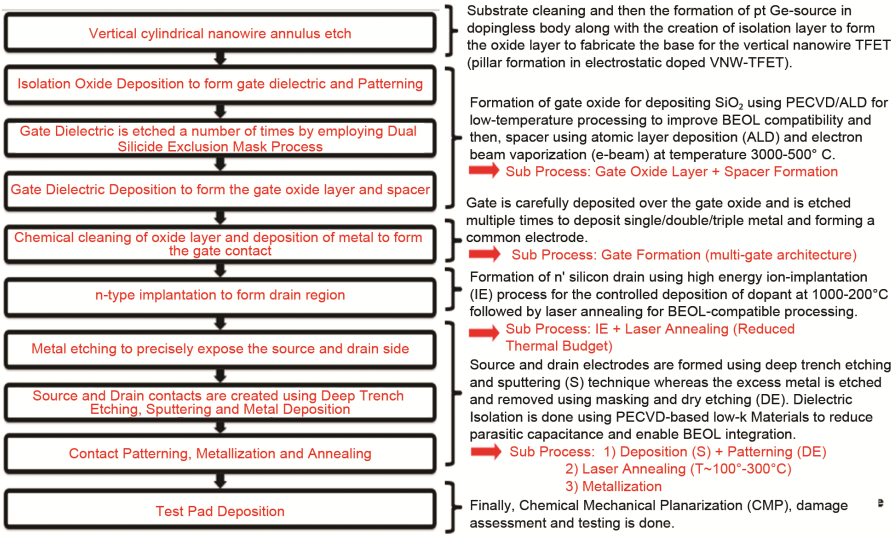


Fig. 1 — 3D structure of (a) Si-S-ED-VNW-TFET, and (b) InAs-S-ED-VNW-TFET, and (c) Fabrication flow chart of InAs-S-ED-VNW-TFET [3,18,19].

TFET structure. In order to increase BEOL (back-end-of-line) compatibility, isolation oxide is formed and patterned to build the dielectric gate using PECVD (plasma-enhanced chemical vapour deposition)/ALD (atomic layer deposition) for low-temperature processing. BEOL-compatible processing and a lower thermal budget are achieved through laser annealing. Thereafter, a dual silicide exclusion mask method is used to etch the gate dielectric repeatedly. Metal is deposited for the gate contact following chemical cleaning, and the source and drain sides are precisely etched. Metal deposition, sputtering, and deep trench etching are used to build source and drain connections. Although BEOL integration can be achieved using low-temperature processing. The device is mainly designed for FEOL (front-end-of-line) applications.

3 Results and Discussion

In this section, the analysis of the proposed device is done for the analogous and structural parameters. This section contains two parts. In the first part, the performance of the proposed device, InAs-S-ED-VNW-TFET, is compared with that of Si-S-ED-VNW-TFET, and in the second part, optimization is done for the proposed device for the carrier concentration by changing the doping level with the help of applied electrostatic voltage. The device's performance has been investigated in this study. The WKB approximation elaborates that the energy band gap in InAs-S-ED-VNW-TFET can be reduced by lowering the effective-mass of the charge carriers, which will increase the tunneling-probability of the device, as shown by T_{WKB} as given in equation (1), to increase[20].

$$T_{WKB} = \exp\left(-\frac{4\lambda\sqrt{2m*}\sqrt{E_g{}^3}}{3qh(E_g+\triangle\phi)}\right) \quad \ldots (1)$$

where, $E_g$represents the bandgap energy, a decrease in E_g will increase the probability of tunnelling.

m*= effective mass,

$\triangle\,\phi$ = possible distinction between the conduction band of the channel and the valence band of the source

λ = screening length given by equation (2) as,

$$\lambda = \sqrt{\frac{\varepsilon_{Si}t_{Si}t_{OX}}{\varepsilon_{OX}}} \quad \ldots (2)$$

where "λ" can be reduced by the introduction of a high dielectric constant material as the gate-oxide material[20] which will result in the creation of channel bands with strong modulation.

Figure 2(a) illustrates the energy band diagrams for both the Si-S-ED-VNW-TFET and the InAs-S-ED-VNW-TFET in the OFF state (drain voltage is 1V and gate voltage is 0V) and the ON state (drain voltage is 1V and gate voltage is 1V). As the band gap of the material decreases in the tunnel width, the resistance of tunneling also decreases. The same can be seen in Fig. 2(a), where the tunneling width for InAs-S-ED-VNW-TFET reduces as compared to that of Si-S-ED-VNW-TFET. In Fig. 2(b), the tunneling gap or width is reduced so that the charge carriers may tunnel easily. Furthermore, the electron-tunneling rate of the InAs-S-ED-VNW-TFET is higher than that of the device Si-S-ED-VNW-TFET because the tunneling probability of the InAs-S-ED-VNW-TFET is higher. The tunneling rate in the InAs-S-ED-VNW-TFET has a greater value than its counterpart in the Si-S-ED-VNW-TFET. The surface penitential for both devices is shown in Fig. 2(c). The band gap is narrower in the source due to the InAs material, so the surface potential of the proposed InAs-S-ED-VNW-TFET is higher than that of the Si-S-ED-VNW-TFET. In the rest of the device, the surface potential for both devices is the same. Figure 2(d) shows the electric field for both the devices Si-S-ED-VNW-TFET and InAs-S-ED-VNW-TFET. Figure 2(d) shows that the device with the InAs source has a higher electric field on the source side than the device with the Si source. The presence of InAs, a low-bandgap material, at the source side causes this behaviour. Since the drain material is the same for both devices, this pattern persists until the curve approaches the drain area. As a result, the devices' electric field values are nearly equal on the drain side.

Figures 2(e) & (f) shows the carrier concentration of e^- and $h^+$for both the devices Si-S-ED-VNW-TFET and InAs-S-ED-VNW-TFET. From Fig. 2(e) & (f), it can be observed that for the device InAs-S-ED-VNW-TFET, the e^- as well as h^+concentration is higher than for the device Si-S-ED-VNW-TFET. This occurrence is caused by the use of low bandgap material InAs as compared to Si material. The quasi-Fermi-level (QFL) is the energy level that describes the distribution of electrons or holes when the system is not in thermal equilibrium. In thermal equilibrium, there's only one Fermi level[21,22] E_F, and both electrons and holes follow

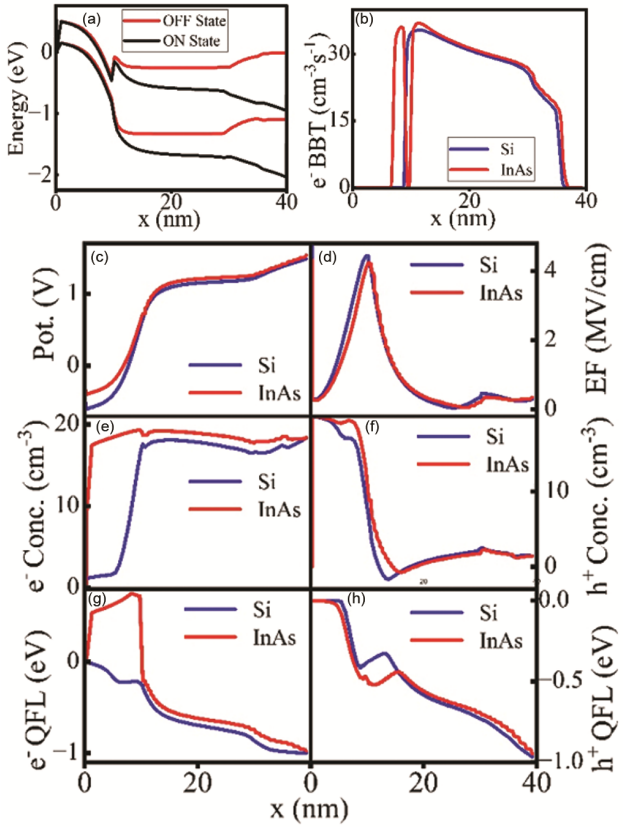


Fig. 2 — (a) Energy-band diagramfor InAs-S-ED-VNW-TFET, (b) BBT rate, (c) Surface potential distribution, (d) Electric field profile, (e) e^-conc., (f) h^+ conc., (g) e^-QFL, and (h) h^+QFL for Si-S-ED-VNW-TFET and InAs-S-ED-VNW-TFET.

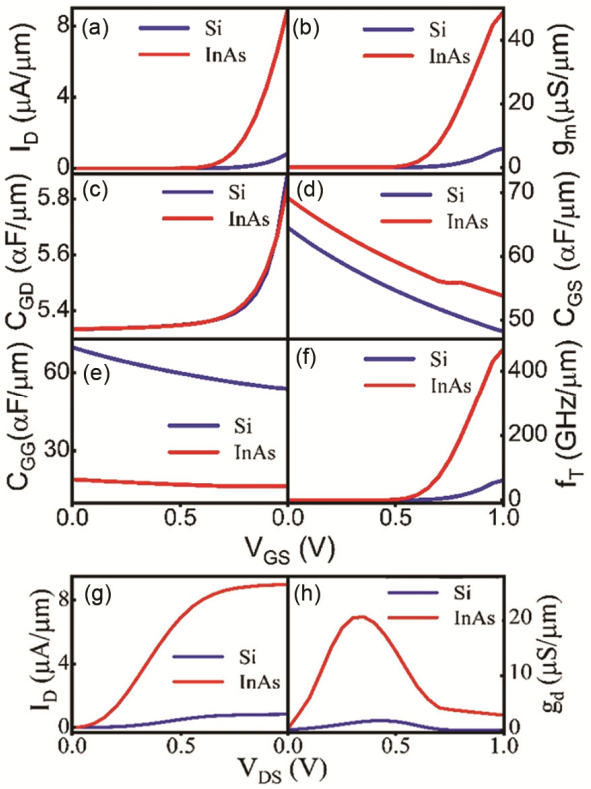


Fig. 3 — (a) Drain current, (b) g_m, (c) C_{GD}, (d) C_{GD}, (e) C_{GG}, (f) f_T with respect to gate voltage, (g) I_D, and (h)g_d with respect to drain voltage for Si-S-ED-VNW-TFET and InAs-S-ED-VNW-TFET.

it. But in non-equilibrium conditions (e.g., under illumination or electrical injection), the distributions of electrons and holes deviate from equilibrium. The QFL for electrons and holes is shown in Fig. 2 (e & h). In InAs-based devices, the quasi-Fermi levels for electrons and holes respond differently to carrier injection compared to a Si-based device, as the InAs has a much smaller direct bandgap (~0.36 eV) and extremely high electron mobility. Under non-equilibrium conditions, E_{Fn} shifts closer to the conduction band and E_{Fp} toward the valence band, with a greater separation between them than in silicon for the same injection level. This is because InAs has a higher intrinsic carrier concentration and allows easier population of conduction and valence bands. However, effects like Fermi level pinning at surfaces can also influence QFL positions in nanoscale InAs devices. Figure 2(g) illustrates that for InAs-S-ED-VNW-TFET, in the source region, the electron QFL has higher values, while in the drain and channel region, it is similar for both devices.

The transfer characteristic of both the devices, Si-S-ED-VNW-TFET and InAs-S-ED-VNW-TFET, is shown in Fig. 3(a). From Fig. 3(a), it is proven that the drain current of InAs-S-ED-VNW-TFET is higher than that of Si-S-ED-VNW-TFET, because the InAs material has a lower band gap and a higher tunneling rate of charge carriers. The transconductance g_m is calculated by the I_D and V_{GS} as shown in equation (3). As the drain current for the device InAs-S-ED-VNW-TFET is higher, similarly, the g_m is also higher for the same, as illustrated in Fig. 2(b). The capacitances C_{GD} and C_{GS} of the device are illustrated in Fig. 3(c) and (d). Both types of capacitances are showing higher values for the device InAs-S-ED-VNW-TFET than those of Si-S-ED-VNW-TFET. C_{GG} is calculated by the sum of both C_{GD} and C_{GS}. Therefore, it is also exhibiting the higher values for the device InAs-S-ED-VNW-TFET as illustrated in Fig. 3(e). Figure 3(f) shows the frequency f_T for both structures, InAs-S-ED-VNW-TFET and Si-S-ED-VNW-TFET. The maximum frequency at which a given device can amplify a signal is denoted as f_T . The physical formula for f_T is given by equation (4)[15,23]. As f_T is

Table 1 — Comparative analysis of performance parameters.

Device	SS (mV/Dec)	I_{ON} (A/μm)	I_{ON}/I_{OFF}
Ref [21]	62.6	~10^{-6}	~10^{+7}
Ref [22]	-	-	~10^{+7}
Ref [23]	160	6 x 10^{-6}	~10^{+6}
Ref [24]	-	~10^{-8}	~10^{+10}
Ref [25]	370	5 x 10^{-6}	-
Ref [26]	51	~1 x 10^{-7}	~10^{+11}
Si-S-VNW-TFET	26.2	4.13 $_X$ 10^{-6}	1.70 x 10^{+12}
Proposed InAs-S-VNW-TFET	19.08	8.99 $_X$ 10^{-6}	1.23 x 10^{+13}

dependent on the device's transconductance (g_m), leading g_m increases f_T as well. Consequently, the f_T value of the device InAs-S-ED-VNW-TFET should be higher than that of the device Si-S-ED-VNW-TFET. While the channel resistance depends on its carrier concentration, V_{DS} also contributes the creation of width, which influences tunnel-resistance[14,24,25]. As evident from Fig. 3(g), the ED-VNW-TFET with an InAs source has a narrower tunneling width than the Si-S-ED-VNW-TFET. As a result, I_D increases due to a reduction in tunnel resistance caused by the narrower tunnel width of InAs-S-ED-VNW-TFET. As a result, the I_D-V_{DS} curve of the InAs- source structure has a higher value than that of the Si-S-ED-VNW-TFET, as shown in Fig. 3(g). The g_d of the devices under study is represented by the change in I_D-V_{DS} of the device, keeping V_{GS} constant. The g_d is determined using the formula given in equation (5)[15,26], which is a crucial parameter since it affects the device's intrinsic gain. While V_{GS} remains constant, g_d depends on I_D and increases as I_D increases. Figure 3(h) illustrates g_d versus drain voltage V_{DS} while keeping V_{GS} constant.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad \ldots (3)$$

$$f_T = \frac{g_m}{2\pi C_{GG}} \quad \ldots (4)$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \quad \ldots (5)$$

Table 1 compares the observations from this investigation with those from other proposed works. The proposed device, InAs-S-ED-VNW-TFET, has the lowest subthreshold slope (19.08mV/Dec) and gives better switching. Other advantages of the InAs-S-ED-VNW-TFET above the other devices include the high ON current of 8.99×10^{-6} and the I_{ON}/I_{OFF} ratio of 1.23×10^{13}. They both can therefore function effectively and reduce the leakage power and low leakage power.

4 Conclusion

The designs of both the ED-VNW-TFET structures, with silicon and InAs sources, proposed and analyzed in this article using their RF and analog characteristics. Since silicon on the source side is replaced with the low-bandgap material InAs, the InAs-S-ED-VNW-TFET has been observed to exhibit improved characteristics compared to the Si-S-ED-VNW-TFET. Due to their doping-free nature, both devices are simpler to manufacture, and their reconfigurable nature allows doping to be varied during operation. Additionally, the superior RF performance of the InAs-S-ED-VNW-TFET makes it a strong candidate for next-generation communication technologies. The proposed InAs-S-ED-VNW-TFET exhibits improvements of 117.6% in I_{ON}, while the $I_{OFF}$and SS is reduced by 69.91% and 27.2%, respectively, as compared to its conventional counterpart. Future research can focus on optimizing material properties and device architecture to further enhance efficiency. These advancements could contribute significantly to the development of innovative applications in nanoelectronics and energy-efficient semiconductor technology.

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