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Design and analysis of PV fed single-stage AC-DC bi-fold converter for onboard charging applications

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Traditional electric vehicle (EV) chargers typically employ a dual-stage configuration to achieve a significant step-down in voltage, which results in discontinuous input current and compromised efficiency. This paper has proposed a single-stage, single-phase high step-down bifold converter featuring synchronous rectification and ripple mitigation to address these challenges. By regulating the intermediate bus voltage (IBV) to provide only half of the output voltage, the converter ensures continuous input current with a near-unity power factor. A highly efficient 1.55KW prototype, converting from 230V AC and PV panel to 48V DC, has been developed, simulated and analyzed using MATLAB. The charger's performance has been rigorously analyzed and harmonic compensator has been introduced to eliminate ripple components causing improvements in efficiency and reduction in THD along with operational stability.

Keywords: EV charger, Parasitic element, Ripple mitigator, Single stage high step down AC-DC converter

1 Introduction

For more than a century, the operation of vehicles powered by internal combustion engines has permanently altered the climate. Due to the exhaustion of fossil fuel supplies and rise in environmental pollutants, research has switched to electric vehicles. Electric vehicles includes following features; efficient electric drivetrains, storage systems, and charging infrastructure. Apart from several groupings based on charging capacity and AC/DC types, SAEJ1772 separated EV chargers into categories for on-board and off-board (independent) chargers. While onboard chargers must be extremely energy dense, light, and efficient, off board chargers, which are installed outside the car, are not limited by size or weight.

It is usually advised to use Level 1 chargers for devices that can operate on single phase energy (in the range of 3.3kW for battery voltages of 48V, 72V, or 96V which is less than 100V). Thus, there is a need for a power-dense, single-stage EV charger that can only charge a battery at 48V for as long as it is connected to a single-phase grid.

Single stage converters[1-10], employing a bridge less architecture, have been introduced to markedly mitigate conduction losses by enabling current flow through a minimal switch configuration contrasting to conventional PFC circuits. The proposed architectures not only diminishes the semiconductor device count but also curtails the system's overall mass and spatial footprint relative to the traditional unfolding bridge structures.

Buck PFC converter-basedchargers[11–15] are suggested in CCM and DCM to replace boost PFC interfaces for extremely low power level applications since they offer lower output voltage and comparatively greater efficiency. They do not comply with IEC 61000-3-2 as they have a substantially lower power factor due to the formation of dead zones, which appears when the input voltage drops below the corresponding DC bus voltage resulting in low power factor and heavy input current harmonics. According to reports, two stageschargers[16–21] can be used to eliminate dead zones in buck converters. However, a second stage cascaded DC-DC must be added or present in order to supply the step-down voltage. This adds weight and volume to the device and results in higher losses, less efficiency, higher prices, and less power density.

Other alternative is single stage converters[22] uses isolated converter affecting efficiency of system. Literature mentioned inliterature[23] presents a streamlined single-phase bridgeless Cuk-derived DC-DC converter for flexible V2V and grid-to-vehicle EV charging. Utilizing a single power stage and

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discontinuous conduction mode, it minimizes control demands and component count, achieving high efficiency with compact, cost-effective design. DC-DC stage, increasing the number of stages and component count.

When operating in grid-to-vehicle mode, an additional AC-DC converter is required before the a single-stage grid-to-vehicle charger to streamline the process and enhance efficiency.while[24–25]describes a high-efficiency, single-stage on-board charger for AC-to-battery EV charging, using a bridgeless converter. It achieves power factor correction (PFC), component stress reduction, and precise charging control with constant current and voltage but contains 100Hz harmonics component PFC chargers often add a significant 100 Hz frequency component to the output, which is replicated at the DC side as well and results in additional harmonics showing up at the output. Active power decoupling[26] circuit is used to eliminate the need of bulky DC link capacitor. However it charges a battery of 300V dc from 110V rms grid voltage leaving behind the need of single stage EV charger with active ripple compensation. ACHR[27–28] technique is used which employs a sophisticated multilevel filter design to effectively attenuate third order and high frequency harmonic distortions prior to their transmission through the current control loop. This optimization not only enhances the robustness of the closed-loop system but also preserves the integrity of the fundamental harmonic characteristics but leaving behind need of compensator which compensated 2nd order harmonics. Thus, further research on AC-DC converters for battery charging applications is required.

For low voltage EV applications such as charging batteries for UPS, e-rickshaws, e-scooters, and e-bikes, it is recommended to utilize proposed single stage bi-folding converter (SSBC) with synchronous rectification and a ripple mitigator as shown in Fig. 1. Additionally solar energy is utilized to charge battery in the proposed system using buck-boost converter and modified MPPT method is used to extract maximum power fromPV Panel[29–30]. A comparative analysis between the proposed converter with existing other topologies is mentioned in Table 1.

The key features of the proposed single stage bifold converter (SSBFC) for EV charging are mentioned below:

- Modeling and control has been done including parasitics.
- Common mode current compensation has been done.
- Sinusoidal input current is achieved through single-stage conversion, circumventing the emergence of dead zones.
- Voltage stress of components are reduced due to bifolding switching cells(BSC) to mitigate voltage stress.
- Nearly unity power factor along with high efficiency is achieved.
- Active ripple compensation reducing THD has been done using full-bridge topology.

Furthermore, a thorough analysis, design, and streamlined control of the circuit are presented,

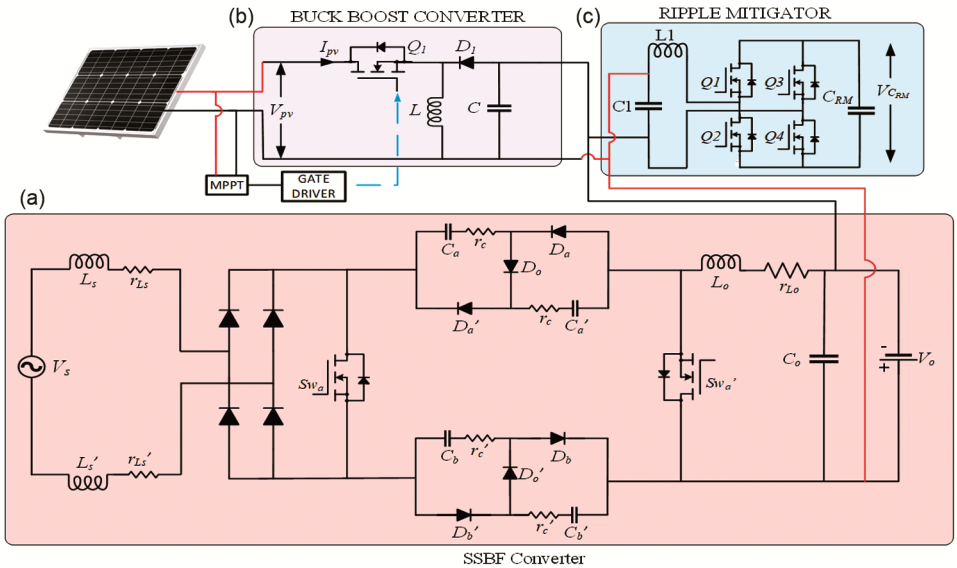

Fig. 1 — (a) Single stage PV fed AC-DC bifold converter, (b) Buck boost converter and (c) Ripple mitigator.

Table 1 — Comparison of existing topologies with the proposed SSBF PV fed converter.

Feature / Metric	Proposed Converter	[17] Two-Stage MPC with Reduced Cap	[24]Bridgeless Cuk V2V Converter	[26] Interleaved Buck-Boost PFC + LLC Charger	[21] MUT-MPC with DFF	[18] High-Gain Buck-Boost + Cuk DC–DC
Stage Count	Single-stage	Two-stage	Single-stage	Two-stage	Two-stage	Two-stage
AC–DC Topology	Diode bridge + switched capacitor	2-leg boost PFC front-end	Bridgeless Cuk-derived	Interleaved bridgeless buck-boost	2-leg boost PFC with predictive control	High-gain buck-boost PFC + isolated Cuk DC–DC
Output Voltage	48 V	200 V DC-link → DC–DC stage regulates battery	Variable low-voltage (supports V2V)	48–72 V battery range	48–72 V battery	Designed for 48 V battery
Efficiency (%)	94%	~91%	High, but not quantified	93% peak	~91% peak	~90% peak
Power Factor (PF)	Unity PF	~0.99	Not specified	Unity (DICM operation)	~0.99	0.97
THD (%)	2.25%	~3.2% (varies with capacitance)	Not reported	2.08%	~3.5%	~3.2%
DC-Link Capacitance	Not needed (single-stage)	Reduced capacitance with DFF	Not applicable	Normal size DC-link	Reduced capacitance using MPC+MUT	Medium filtered by passive LCL + DC–DC isolation
100 Hz Ripple Control	Active Ripple Mitigation at battery current	Feed forward + DFF to reduce ripple	Not addressed	Only passive filtering	DFF method used	Only output capacitor smoothing
Support for PV Input	Yes, acts as hybrid PV-EV charger	No	No	No	No	No

corroborated by empirical findings demonstrated within a MATLAB environment. The control and operation of the active ripple compensator are also comprehensively addressed and illustrated.

2 Material and Methods

The proposed SSBF converter is fed by single AC phase supply and solar energy through a diode bridge and connected in conjunction to a bifold buck phase switching cells (modified Cuk converter) and synchronous rectification switch (Fig 1). Second harmonic compensator is utilized having current control mode after this stage.

In addition to offering a very minimal region of dead zones, the bi-folding stage of a single stage eV charger permits parallel discharging and series charging of storage capacitors in both directions to provide better buck potential of the circuit. The circuit's inherent bi-folding capability enables intermediate bus voltage (IBV) to spill evenly into each capacitor (as connected in series), keeping the output voltage simply low while the capacitors' stored power is seamlessly transferred to the output by discharging them parallelly in duplets, which limits voltage ripple.

2.1 Operation of SSBFC

Mode1: When switch S_{wa} *is ON and switch* S_{wa}' *is OFF*

Due to the forward biasing of diodes D_a,D_a',D_b and $D_b'$and the reverse biasing of diodes D_O and D_O', Switch S_{wa} is triggered to charge grid side inductors L_S and L_S' in tandem. In order to charge the output inductor, capacitors are operated in parallel and discharge through the switchS_{wa}, keeping switch S_{wa}', in the off position is shown in Fig. 2.

Mode2: When switchS_{wa} *is OFF and switch* S_{wa}' *is ON*

As soon as switch S_{wa} is switched off and switch S_{wa}' is switched on, allowing transfer of power from the AC side to the capacitors connected in series via inductors. This becomes possible due to the forward biasing of diodesD_O and D_O' along with diode connected in antiparallel with S_{wa}'.The switch S_{wa}'possesses synchronous rectification at this stage, as indicated in Fig. 3.

2.2 Operation of proposed single stage AC-DC bifold converter

This section represents the steady state analysis and state space modelling of SSBFC. The relationship between input and output voltage are developed

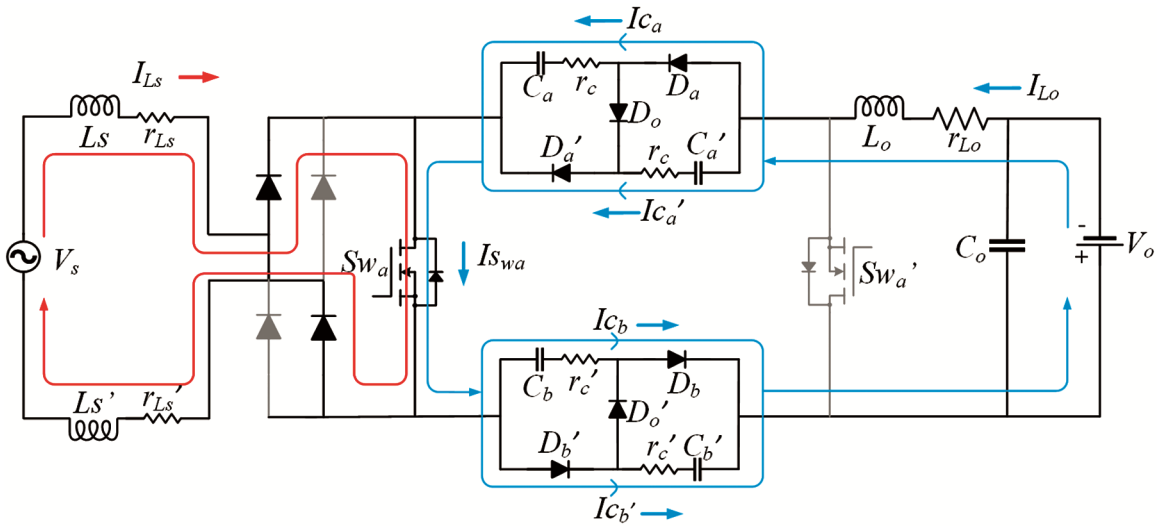

Fig. 2 — Mode 1: when switch S_{wa} is ON.

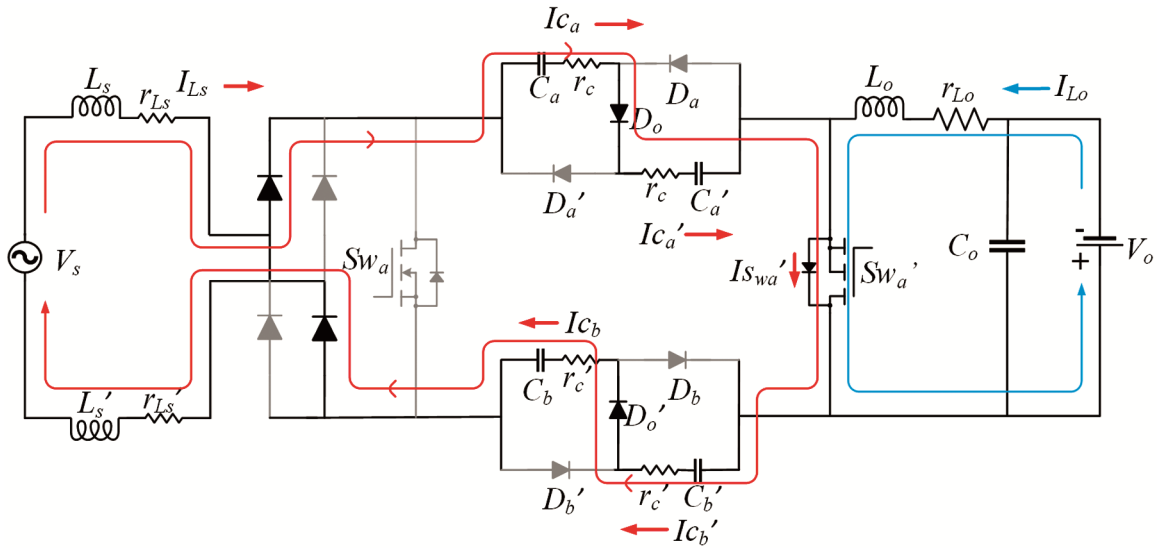

Fig. 3 — Mode 2: when switch S_{wa}' is ON.

according to the current balance equations for C_a and C_b. As the circuit imitates the features of Cuk converter, duty cycle for switch S_{wa} under fifty percent leads to buck behavior which is needed for high step down in one stage.

2.2.1 Steady state analysis

In the event that switch S_{wa} is closed, it is assumed that all of the capacitors linked to the switching cell have the same value.

$$I_{Ca}=I_{Ca}{}'=I_{Ca}=I_{Ca}{}' \quad \ldots (1)$$

$$I_{LO}=I_O=2I_{Ca}=2I_{Ca}{}'=2I_{Cb}=2I_{Cb}{}' \quad \ldots (2)$$

$$I_{s_{wa}}=I_{LS}+I_{LO} \quad \ldots (3)$$

$$I_{LS}=I_S \quad \ldots (4)$$

Furthermore, when S_{wa}' switch is turned on and S_{wa} is turned off:

$$I_{LS}=I_S \quad \ldots (5)$$

$$I_{LS}=I_{Ca}=I_{Ca}{}'=I_{Cb}=I_{Cb}{}' \quad \ldots (6)$$

$$I_{LO}=I_O \quad \ldots (7)$$

$$I_{s_{wa}}{}'=I_{LO}+I_{LS} \quad \ldots (8)$$

Since equal currents pass through each capacitor, the current balance equation among capacitors C_a, C_a', C_b, and C_b' is the same. Below is an overview of the steady state study for one capacitor (C_a).

$\frac{I_{LO(DT)}}{2} + I_{LS}(1\text{-}dT) = 0$ … (9)

$\frac{I_{LS}}{I_{LO}} = \frac{\text{-}D}{2(1\text{-}D)}$ … (10)

Since input power P_S and output power P_O are equivalent in a lossless system, the voltage gain is as follows:

$P_O = \text{-}V_O\, I_{LO},\ P_S = V_S\, I_{LS}$ ... (11)

$\frac{V_O}{V_S} = \frac{\text{-}I_{LS}}{I_{LO}}$ … (12)

$\frac{V_O}{V_S} = \frac{\text{-}D}{2(1\text{-}D)}$ … (13)

b. State Space Modelling Of Converter:

When switch is on:

$-V_S + V_{LS} = 0$ ... (14)

$-V_O + V_{LO} + -2V_{Ca} = 0$ … (15)

$I_{LO} - 2I_{Ca} = 0$ … (16)

$I_{LO} = I_{CO} + {}^{V_O}/_{R}$ … (17)

When switch is off:

$-V_s + V_{Ls} + 4V_{Ca} = 0$ ... (18)

$V_O + V_{LO} = 0$ … (19)

$I_{Ls} + I_{Ca} = 0$ … (20)

$I_{LO} = I_{CO} + {}^{V_O}/_{R}$ … (21)

Voltage across Inductor and capacitor are as follows:

$V_{Ls} = V_s D + (V_s - 4V_{Ca})(1 - D)$ … (22)

$V_{Ls} = V_s - 4V_{Ca}(1 - D)$ … (23)

$V_{Ca} = V_S/4(1 - D)$ … (24)

2.2.2. Small signal modelling

To derive the transfer function in terms of small-signal perturbations, model is linearized around steady-state operating point. This involves perturbing both the input voltage V_S the output voltage V_o and the duty cycle D with small variations as follows:

$V_S = V_S + v_S(t)$ … (25)

$V_{Ca} = V_{Ca} + v_{Ca}(t)$ … (26)

$I_{LS} = I_{LS} + i_{LS}(\mathrm{t})$ … (27)

$I_{LO} = I_{LO} + i_{LO}(\mathrm{t})$ … (28)

$D = D + d(t)$ … (29)

Considering only perturbed values and taking Laplace transform, following expressions came:

$(L_S s + r_{LS} + 4r_C(1-d))I_{LS}(s) = V_{IN}(s) - 4V_{C1}(s)(1-d) + 4V_{C1}d(s)$ (30)

$(L_o s + r_{LO})I_{LO}(s) = 2V_{Ca}\, d(s) + 2dV_{Ca}(s) - V_O(s)$ … (31)

$C_a s V_{Ca}(s) = (\frac{I_{LO}}{2} + I_{LS})\ \ d(s) - (1-s)I_{LS}(s) + \frac{D}{2}I_{LO}(s)$ ... (32)

$C_O s V_O(s) = I_{LO}\ \ (s)\frac{1}{R}V_O(s)$ ... (33)

*The small-signal transfer fu*nction relates the perturbation in the output voltage V_O to the perturbation in the control input d ignoring parasitic elements is shown in equation (21) below

And with Parasitics the transfer function is mentioned in equation (22)

Where $Z_1 = L_s S + r_1 + 4r_c(1-d)$

$Z_2 = C_O s + \frac{1}{R}$

$Z_3 = L_O s + r_{Lo}$

The small-signal transfer function relating the perturbation in the output voltage V_O to the perturbation in the input voltage V_{in} is shown in equation (23) below. Considering parasitic elements, transfer function obtained is shown in equation (24) below.

$$\begin{bmatrix} \frac{d\hat{\imath}_{L_1}}{dt} \\ \frac{d\hat{\imath}_w}{dt} \\ \frac{d\hat{V}_c}{dt} \\ \frac{d\hat{V}_w}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-4(1-d)}{L_1} & 0 \\ 0 & 0 & \frac{2d}{L_o} & \frac{-1}{L_o} \\ \frac{1-d}{c} & \frac{-d}{2c} & 0 & 0 \\ 0 & \frac{-1}{C_o} & 0 & \frac{-1}{C_o R} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_o} \\ V_c \\ V_{C_o} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{4V_c}{L_1} \\ 0 & \frac{2V_c}{L_o} \\ 0 & \frac{-1}{C}\left(\frac{IL_o}{2} + IL_1\right) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{V}_{in} \\ \hat{d} \end{bmatrix}$$

$\dot{X} = AX + BU$

$$V_{dc} = [0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} iL_1 \\ iL_o \\ V_c \\ VC_o \end{bmatrix} + [0 \quad 0] \begin{bmatrix} \hat{V}_{in} \\ \hat{d} \end{bmatrix}$$

$Y = CX + DU$

$\frac{V_o(s)}{d(s)} =$

$\frac{R(2V_{Ca}L_S C_a s^2 + (I_{LO}L_S d + 2I_{LS}L_S d)s - 8V_{Ca}(1-d)}{L_S C_a L_O C_O R s^4 + L_O C_a L_S s^3 + (L_S C_a R - d^2 L_O C_O R - 4L_O C_O R(1-d)^2)s^2 - (4L_O(1-d)^2 + d^2 L_S)s - 4R(1-d)^2}$ … (34)

$\frac{V_o(s)}{d(s)} =$

$\frac{2C_a s V_{ca} Z_1 Z_3 + 8dZ_3 V_{ca}(1-d)^2 + 2d^2 Z_1 V_{ca} + dZ_1 Z_3 (I_{LO} + 2I_{L1} - 8dZ_3 V_{ca}(1-d) + d^2 Z_1 V_{ca}}{C_a s(1 + Z_2 Z_3) Z_1 Z_3 - 2Z_3(1-d)^2(1 + Z_2 Z_3) - d^2 Z_1(1 + Z_2 Z_3) + d^2 Z_1}$ … (35)

$\frac{V_O(s)}{V_{IN}\ (s)} =$

$\frac{R(2V_{Ca}L_S C_a s^2 + (I_{LO}L_S d + 2I_{LS}L_S d)s - 8V_{Ca}(1-d)}{L_S C_a L_O C_O R s^4 + L_O C_a L_S s^3 + (L_1 C_a R - D^2 L_O C_O R - 4L_O C_O R(1-D)^2)s^2 - (4L_O(1-d)^2 + d^2 L_S)s - 4R(1-d)^2}$ … (36)

$\frac{V_o(s)}{V_{IN}\ (s)} =$

$\frac{2DR(1-D)}{\{(r_{Lo}C_o sR + r_{Lo} + L_O C_O R s^2 + L_O s + R)(4(1-d^2) - L_S C_a s^2 - ZC_a s)\} + d^2(L_S C_O R s^2 + C_O R s Z + L_S s + Z)}$ … (37)

Table 2 — Parameters used and their values.

S. No.	Components	Values
1.	L_s	3mH
2.	L_O	220µH
3.	$C_a = C_a'$	22µF
4.	C_b=C_b'	22µF
5.	C_O	470µF
6.	L_1	220µH
7.	C_1	0.1µF
8.	C_{RM}	2200µF
9.	V_F	0.7V
10.	r_{ds}	0.099
11.	r_{LS}	0.303
12.	r_{Qds}	0.004
13.	r_a	0.1
14.	r_c	0.1
15.	r_{Lo}	0.044
16.	f_s	100KHz
17.	C_{OM}	32pF
18.	r_{L1}	0.02
19.	r_{C1}	0.02
20.	r_{Crm}	0.02

Table 3 — Simulated values for system.

S. No.	Components	Values
1	V_s	230V
2	I_S	10A peak
3	I_{srms}	10.8A
4	I_{Da}	4.25A
5	I_{DM}	10A peak
6	I_{LS}	10A peak
7	I_{ca}	8.5A
8	I_{cb}	8.5A
9	I_{L1}	21.2A
10	I_B	28.9A
11	V_B	51.8V
12	V_{SM}	400V Peak

Where Z= $r_{LS} + 4r_C(1 - D)$

2.3 Computation of proposed converter

The design parameters for the proposed SSBC are computed and chosen values are shown in Table 2 & Table 3. The on-board solar PV array used for extracting solar energy as and when required. It may reduce the burden on the system for battery charging while solar energy is available.

Let proposed SSBC input supply is$V_S(t)$ =$V_m$sin wt and IBV is 207.4V. Here passive and active components are designed for rated power of 1550W. Considering battery voltage as 48V and maximum value of batter y current is set at 24.8A following design equations are estimated as follows;

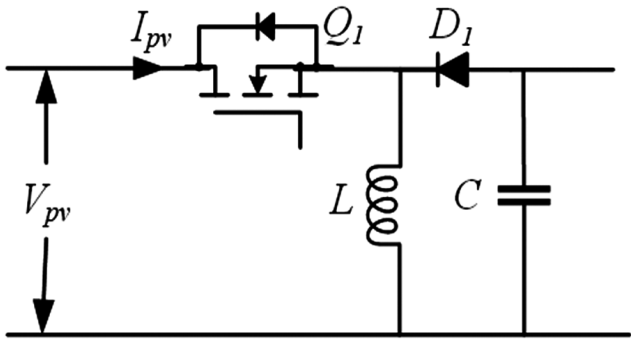

Fig. 4 — Buck boost converter.

$$D = \frac{2V_O}{(2V_O + IBV)} = \frac{2 * 48}{(2 * 48 + 207.4)} = 0.316$$

(i) Designing Input inductor L_S:

$$L_S = \frac{0.03\ IBV^2}{\omega\ P_s}$$

The calculated value is coming very large but SSBFC is responding well for 2mH value.

(ii) Designing Intermediate capacitor:

$$C_a = \frac{DI_O}{\Delta V_{Ca} f_{SW}}$$

For output current 28.9 A and switching frequency of 100 kHz, C_a is taken as 22µF.

(iii) Designing Output side capacitor:

$$C_O = \frac{I_O}{2\ \omega(\Delta V_O)}$$

Its really important to absorb the second harmonic pulsations at the output and requires large capacitor. Various methods are used to reduce its size. As ripple compensator is used, it eliminates need of using high value of output side capacitor. Thus 220 µF capacitor is used for simulation purpose.

2.3.1 On-boad solar PV charging

The on-board solar PV with improved MPPT controller is utilized for the battery charging operation with or without SSBF converter. The buck-boost converter as shown in Fig 4, with improved MPPT controller is used with solar PV array ratings mentioned inLiterature[29−30].

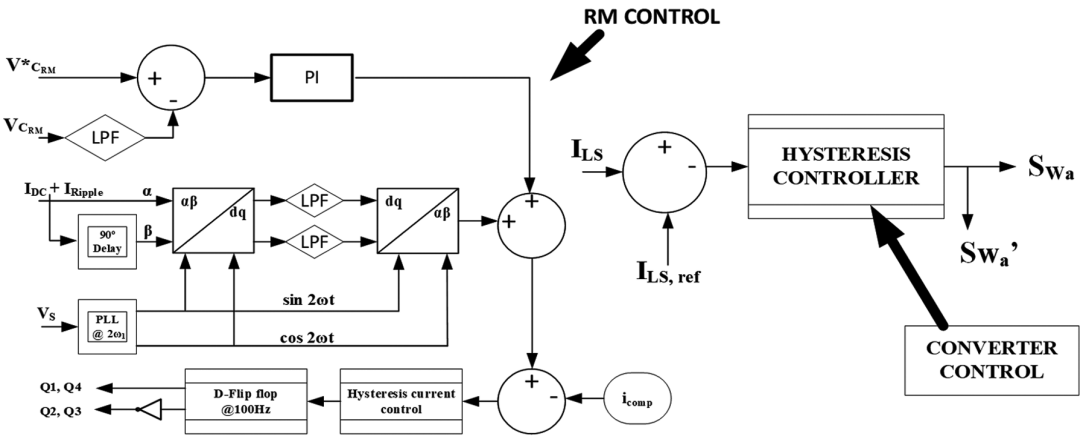

Fig. 5 — Control description of SSBFC and ripple mitigator.

2.4 Control scheme of SSBF converter

2.4.1 Control for AC-DC converter

The suggested EV charger's comprehensive control mechanism is depicted in Fig. 5. The reference current, which is created using the grid voltage unit template, compared with input current in hysteresis current controller. The produced switching pulses are given to switch S_{wa}' and its complementary pulses are given to switch S_{wa}. A D-flip flop is used to limit the maximum switching frequency of the produced pulses to 100kHz. Switches S_{wa} and S_{wa}'have little switching losses during turn off due to very low voltage during turn off. This significantly improves the efficiency of the proposed converter.

2.4.2 Full bridge ripple mitigation technique

The PFC operation causes second harmonic ripple to be formed at the intermediate bus. This ripple is then carried to the converter's output side, where it disrupts the charging current. Such current must be neutralized using the active cancellation method. To mitigate the ripples of the second order harmonic, full bridge ripple mitigationis integrated as illustrated in Fig. 1and Parameters detailed description with values is mentioned in Appendix - A, Table. 4. This paper presents a novel approach where the output current is refined through a low-pass filter after compensating for 100 Hz harmonics via a full-bridge ripple mitigation circuit, thereby attenuating the 100 Hz component. Apart from the DC currentI_{DC}, the AC-DC conversion also generates an output current I_{ripple} with a frequency component of $2\omega_S$. By utilizing an SRF $decomposer$[28], the $2\omega_S$ ripple element Irippple is obtained from the output current I_{DC}+I_{ripple}.

In order to mitigate the ripple from the current entering into the battery, the necessary compensation current I_{comp} is extracted which is set to be inopposition with the 2nd harmonic component of the current I_{ripple}.

The frequency components, aside from $2\omega_s$ and the DC component, are separated sequentially by delaying the I_{DC} + I_{ripple}. by 90 degrees at $2\omega_s$. This is achieved using a Park transformation with a PLL tuned to the $2\omega_s$ frequency. A moving average, serving as a low-pass filter, is implemented to detect transient deviations within a half-cycle. The DC values of the d and q components are then transformed back into the αβ frame to extract the positive sequence $2\omega_s$ component.

Figure 5 discusses the detailed control approach of the proposed system. Measuring the filtered voltage at C_{RM}[28]. provides an estimation of the active energy needed to counteract the losses in the full bridge circuit. In order to regulate the dc bus voltage and estimate the inverter losses, the PI controller responds on the difference between the filtered V_{CRM} and V_{Ref}. DC voltage filtering which provides power transmission between the inverter's DC bus and supply is solely caused by DC current, not by harmonic frequency. The difference between the reference current generated by SRF decomposition and the current needed for DC bus control is compared with the actual current. By adjusting the MOSFETs in RM in accordance with the switching sequences generated by the control scheme, the reference current acquired from SRF decomposition and the current needed for DC bus regulation are compared with the actual

Table 4 — Power loss anaysis in detail for four cases.

Cases	I/P Power	O/P Power	Power Loss	Efficiency	PF	THD
Case 1 Without Parasitic and with Compensator	1550W	$V_B I_B = 51.78 * 27.6 = 1429.12W$	$P_{loss} = 121W$ $P_{sw} = f_s C_{OM} {V_{sm}}^2$ $= 100 * 10^3 * 33 * 10^{-12} * \left({}^{400}/_{\sqrt{2}}\right)^2$ $= 0.264W$ $P_{rds} = r_{ds} {I_{srms}}^2 = 0.099(10.8)^2 = 11.54W$ $P_{Da} = V_F I_{Da} = 0.7 * 4.25 = 2.975W$ $= As four\ diodes\ in\ conduction\ 4 * 2.975$ $= 11.9W$ $P_{DM} = V_F I_{DM} = 0.7 * 7.07 = 4.95$ $= 4.95 * 2 = 10W$ $P_{QSW} = 100 * 10^3 * 33 * 10^{-12} * 100^2$ $= 0.033$ $P_{Qrds} = 0.004 * \left({}^{30}/_{\sqrt{2}}\right)^2 = 1.8W$ $2P_Q = 3.67W$ $P_{misc.} = P_{co} + P_{LS} + P_{LO} + P_{C1} + P_{L1} + P_{crm}$ $= 83.62W$ $I_{RM} = 30A\ Peak$ $I_{RM} = 21.21Arms$	0.92	0.99995	2.27%
Case 2 Without Parasitic and without Compensator	1550W	$V_B I_B = 51.8 * 28.65 = 1484W$	$P_{loss} = 66W$ $P_{sw} = f_s C_{OM} {V_{sm}}^2$ $= 100 * 10^3 * 33 * 10^{-12} * \left({}^{400}/_{\sqrt{2}}\right)^2$ $= 0.264W$ $P_{rds} = r_{ds} {I_{srms}}^2 = 0.099(10.8)^2 = 11.54W$ $P_{Da} = V_F I_{Da} = 0.7 * 4.25 = 2.975$ $= 4 * 2.975 = 11.9W$ $P_{DM} = V_F I_{DM} = 0.7 * 7.07 = 4.95$ $= 4.95 * 2 = 10W$ $P_{misc.} = P_{co} + P_{L1} + P_{LO} = 32.3W$	0.94	0.9999	2.25%
Case 3 With Parasitic and without Compensator	1550W	$V_B I_B = 51.75 * 25.88 = 1339W$	$P_{loss} = 211W$ $P_{sw} = f_s C_{OM} {V_{sm}}^2$ $= 100 * 10^3 * 33 * 10^{-12} * \left({}^{400}/_{\sqrt{2}}\right)^2$ $= 0.264W$ $P_{rds} = r_{ds} {I_{srms}}^2 = 0.099(10.8)^2 = 11.54W$ $P_{Da} = V_F I_{Da} = 0.7 * 4.25 = 2.975W$ $= As four\ diodes\ in\ conduction\ 4 * 2.975$ $= 11.9W$ $P_{DM} = V_F I_{DM} = 0.7 * 7.07 = 4.95$ $= 4.95 * 2 = 10W$ $P_{rLS} = r_{LS} {I_{LS}}^2 = 0.303\left({}^{10}/_{\sqrt{2}}\right)^2 = 18.05W$ $P_{ca} = r_a {I_{ca}}^2 = 0.1(I_{ca})^2 = 12.34W$ $P_{cb} = r_c {I_{cb}}^2 = 0.1(I_{cb})^2 = 12.34W$ $P_{rLo} = r_{Lo} {I_{Lo}}^2 = 0.044 * 28.9 * 28.9$ $= 36.74W$ $P_{misc.} = 97.82W$	0.854	0.9998	2.35%

(*Contd.*)

Table 4 — Power loss anaysis in detail for four cases. (*Contd.*)

Cases	I/P Power	O/P Power	Power Loss	Efficiency	PF	THD
Case 4 With Parasitic and with Compensator	1550W	$V_B I_B = 51.7 * 24.8 = 1289W$	$P_{loss} = 261W$ $P_{sw} = f_s C_{OM} {V_{sm}}^2$ $= 100 * 10^3 * 33 * 10^{-12} * \left({}^{400}/_{\sqrt{2}}\right)^2$ $= 0.264W$ $P_{rds} = r_{ds} {I_{srms}}^2 = 0.099(10.8)^2 = 11.54W$ $P_{Da} = V_F I_{Da} = 0.7 * 4.25 = 2.975W$ $= As four\ diodes\ in\ conduction\ 4 * 2.975$ $= 11.9W$ $P_{DM} = V_F I_{DM} = 0.7 * 7.07 = 4.95$ $= 4.95 * 2 = 10W$ $P_{rLS} = r_{LS} {I_{LS}}^2 = 0.303\left({}^{10}/_{\sqrt{2}}\right)^2 = 18.05W$ $P_{ca} = r_a {I_{ca}}^2 = 0.1(I_{ca})^2 = 12.34W$ $P_{cb} = r_c {I_{cb}}^2 = 0.1(I_{cb})^2 = 12.34W$ $P_{rLo} = r_{Lo} {I_{Lo}}^2 = 36.74W$ $P_{QSW} = 100 * 10^3 * 33 * 10^{-12} * 100^2$ $= 0.033$ $P_{Qrds} = 0.004 * \left({}^{30}/_{\sqrt{2}}\right)^2 = 1.8W$ $Two\ switches = 2 * (1.8 + 0.033)$ $= 3.67W$ $P_{misc.} = P_{co} + P_{L1} + P_{LO} = 126.15W$ $P_{rL1} = r_{L1} {I_{L1}}^2 = 0.02(21.21)^2 = 9W$ $P_{rC1} = r_{C1} {I_{C1}}^2 = 0.02(6.602e^3)^2$ $= 6.34e^{-10}$ $P_{rCrm} = r_{crm} {I_{Crm}}^2 = 0.02(21.21)^2 = 9W$	0.825	0.99998	2.35%

current I_{Comp} fed into the DC bus to compensate for I_{Ripple}.

3 Results and Discussion

Comprehensive simulation analyses aredone to elucidate the operational efficacy of the proposed 1550W converter, both with and without active ripple compensation. Figure 6 shows the input Voltage and input current from grid for different power rating ranging from 500W to 1550W system.

Active power and reactive power for different power ratings of 500, 750, 1150 and 1550W is shown in Fig. 7.

The voltage across C_{RM} and compensation current which is required to for mitigation of 100Hz ripple is shown in Fig. 8.

3.1 Effect of parasitic and ripple compensator on battery performance

In the performance assessment of a converter used to charge a 48V battery, it is important to analyze various configurations with and without parasitic elements and compensators. This detailed analysis focuses on four distinct cases, assessing their impact on key parameters such as battery state of charge (SOC), current, and voltage. The compensator is designed to improve converter performance by mitigating oscillations and stabilizing voltage and current.

3.1.1 Converter without parasitics and with compensator

This case represents an improvement on the first scenario by introducing a compensator. The compensator is typically a feedback control loop designed to regulate the converter output and ensure stability, preventing any overshoot, oscillation, or current/voltage spikes during operation.

The compensator smooths out the current profile, ensuring that the current delivered to the battery is stable and consistent. Any minor fluctuations due to switching events or load changes are mitigated. As a result, the current is precisely controlled according to the charging algorithm Fig. 9.

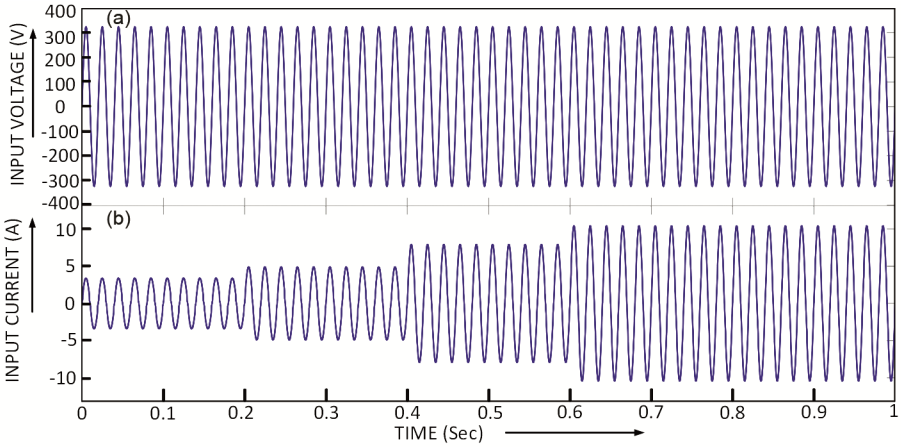

Fig. 6 — (a) Input voltage and (b) Input current for different power ratings.

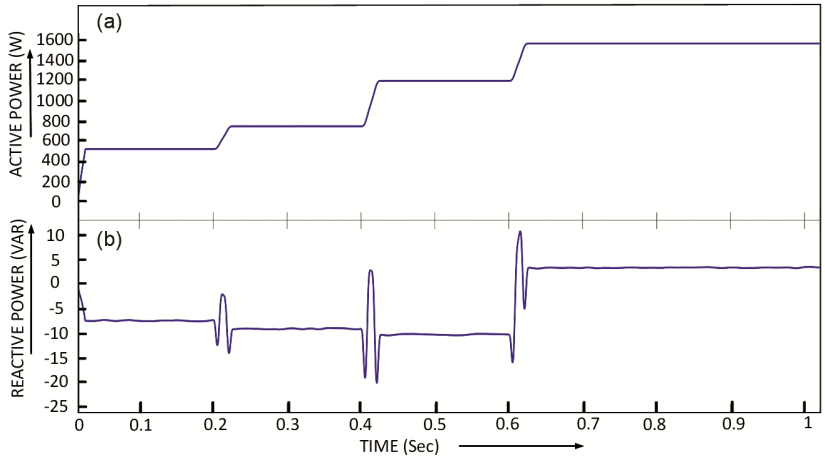

Fig. 7 — (a) Active power (W) and (b) Reactive power (W) for different power ratings.

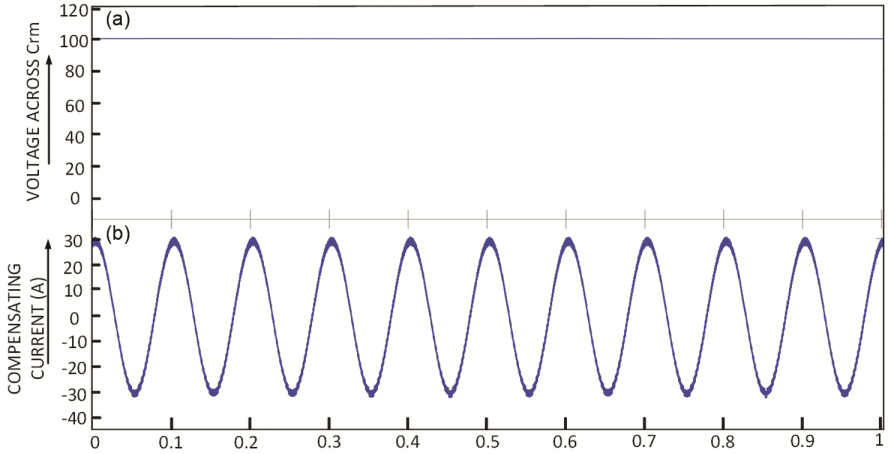

Fig. 8 — (a) Voltage across C_{RM} and (b) Compensation current from RM.

The SOC increases predictably and remains linear, much like in case 1. However, the addition of the compensator may slightly extend charging time due to the more regulated and controlled current profile, avoiding excessive current spikes.

Stability: The key advantage in this case is the enhanced stability provided by the compensator. Voltage and current are regulated more tightly, minimizing the risk of overshooting or voltage ripple, which could potentially harm battery life or cause inefficient charging.

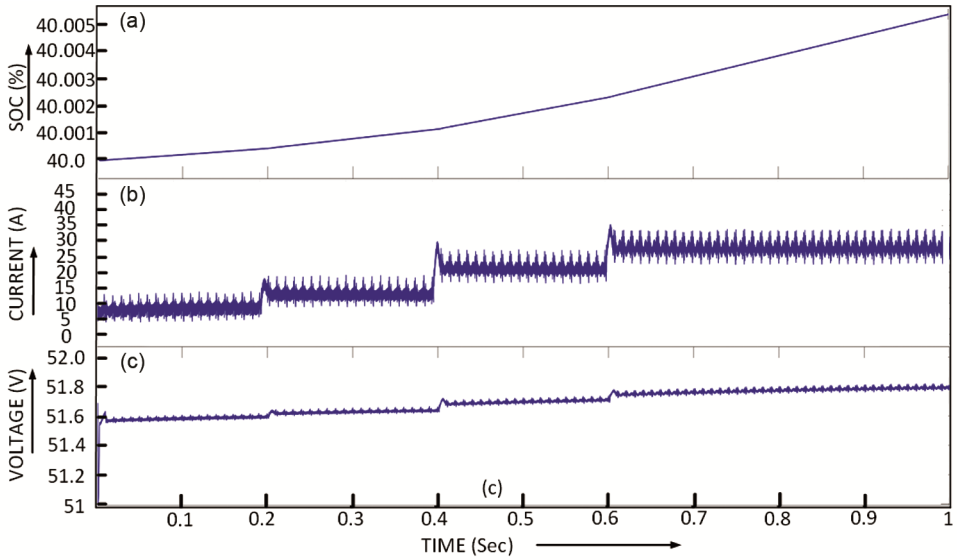

Fig. 9 — 1 (a) SOC (%), (b) Battery current and (c) Output voltage.

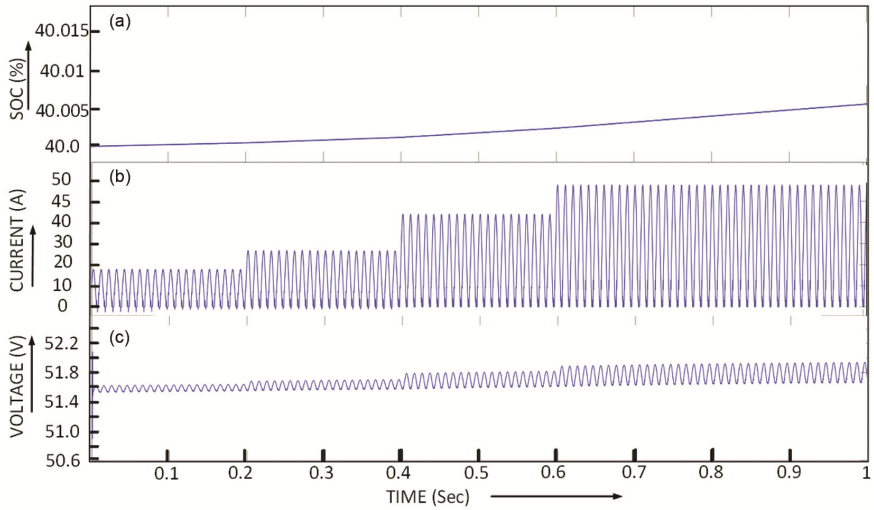

Fig. 10 —2 (a) SOC (%) , (b) Battery current, and (c) Output voltage.

3.1.2 Converter without parasitics and without compensator

In this case, the converter is free from parasitic elements such as parasitic resistance, inductance, and capacitance. Additionally, no compensator is employed to regulate or stabilize the converter output. This represents a baseline scenario to evaluate the intrinsic behavior of the system under ideal conditions.

Since there are no parasitic losses, the converter operates at maximum efficiency, delivering a stable current to the battery. The current follows the expected charging profile dictated by the converter's settings, such as constant current or constant voltage charging modes Fig. 10.

The SOC increases in a linear and predictable manner, corresponding to the designed charging algorithm. With no parasitics, the charging time will be at its theoretical minimum, as all the converter's output is directed towards charging the battery without losses.

However, without a compensator, there may be minor fluctuations in voltage and current during switching events, though these fluctuations are typically minimal in the absence of parasitics.

3.1.3 Converter with parasitics and without compensator

In this case, parasitic elements (resistances, inductances, and capacitances) are present in the converter. These parasitics introduce energy losses and undesirable dynamic effects into the system, and no compensator is in place to regulate the converter's output.

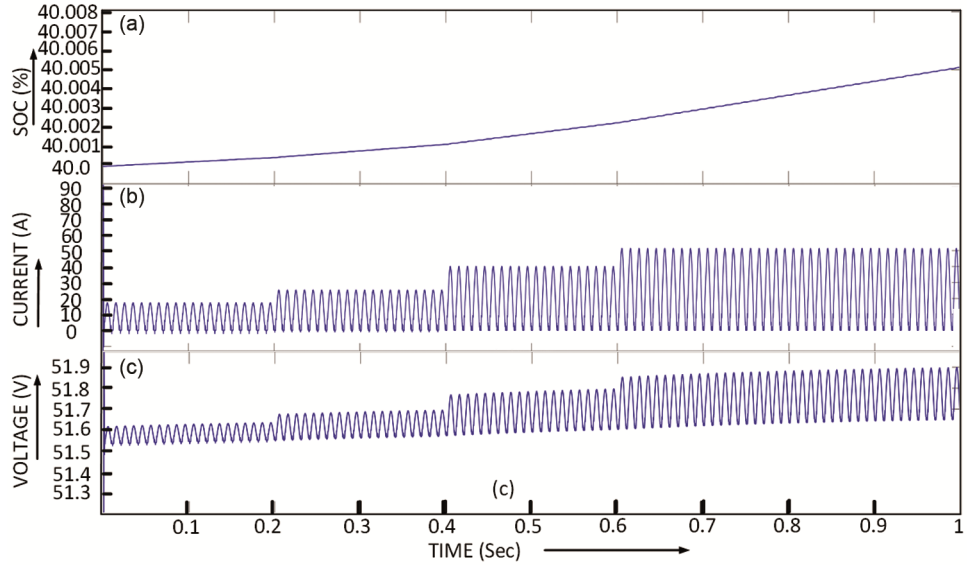

Fig. 11 — Case 3 (a) SOC (%) ,(b) Battery current and (c) Output Voltage.

Parasitic elements cause significant fluctuations in the current profile. Parasitic resistance increases the overall losses, leading to increased heat and causing the converter to draw more current from the battery. Parasitic inductance and capacitance lead to oscillations and spikes in the current waveform, further increasing the current demand from the battery as shown in Fig.11.

Due to the increased current draw and energy losses caused by parasitics, the battery's SOC decreases more rapidly. This occurs because more current is required to maintain the desired output, and the energy losses translate to less efficient charging. The SOC curve becomes nonlinear, as irregular current spikes and oscillations cause unpredictable charging behavior.

Without a compensator, the parasitic elements exacerbate the instability in the converter's operation.

Current and voltage oscillations are more pronounced, and the system is prone to overshoot or excessive ripple, negatively affecting battery health over time.

3.1.4 Converter with parasitics and with compensator

This case introduces a compensator to the system that already includes parasitic elements. The compensator is tasked with regulating and stabilizing the converter output, reducing the adverse effects of parasitics on the charging process.

With the compensator in place, the system's performance improves significantly despite the presence of parasitics. The compensator actively mitigates the oscillations and spikes caused by parasitic inductance and capacitance. The result is a smoother current profile, though the current may be lower than in the previous cases due to compensator action designed to avoid overcurrent conditions as shown in Fig. 12.

The SOC increases in a more controlled and predictable manner compared to case 3. The compensator reduces the effects of current ripple and overshoot, resulting in a more stable charging process. However, the overall charging time may be extended slightly as the compensator limits current spikes and fluctuations to protect the battery.

Figure 13 shows the variation of power factor with power rating for four different cases. Similarly, Figure 14 shows the effect of power rating on THD for different cases as explained earlier in section 3.1.

3.2 Effect of charging rate on battery charging dynamics

When charging a 100Ah, 48V battery with a 500W to 1550W charger, the charging rate varies from C/13 to C/3.5 results in noticeable shifts in both battery current and voltage, which reflect the battery's response to the increasing charge rates shown in Fig. 15 for case 1 and Fig. 16 for case 4.

At the initial charging rate, the current is relatively low (C/13), providing a gentle charge with minimal impact on the battery's internal resistance and temperature. The voltage is at 51.57V, showing the beginning of the charge cycle. This low current minimizes stress on the battery, preserving its life and allowing balanced charging of all cells. With a slight

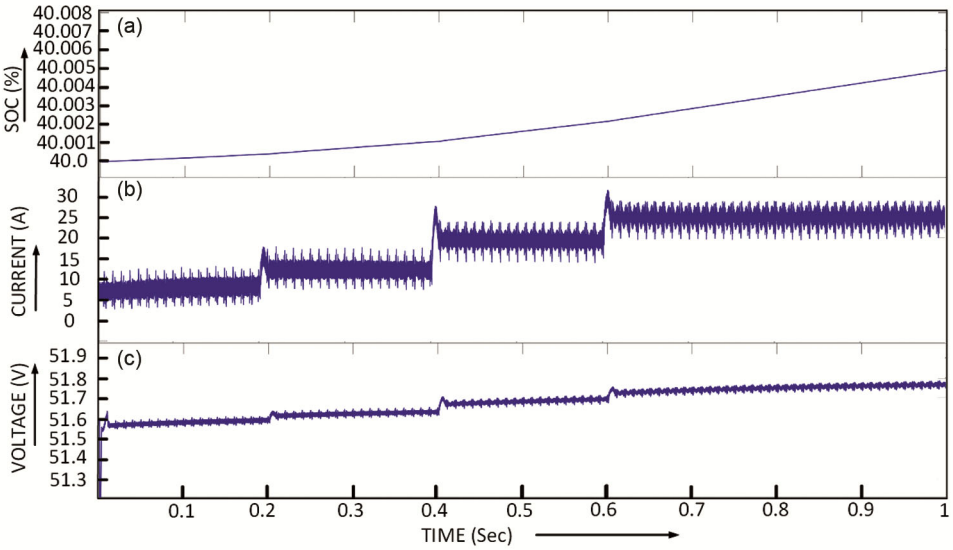

Fig. 12 — 4 (a) SOC (%), (b) Battery current and (c) Output voltage.

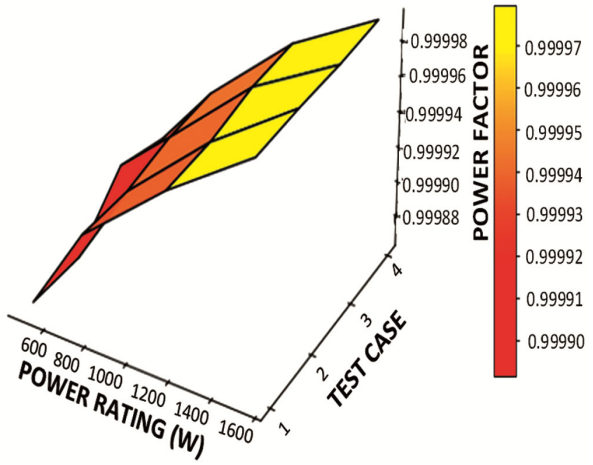

Fig. 13 — Converter power factor for all four cases (3.1.1-3.1.4).

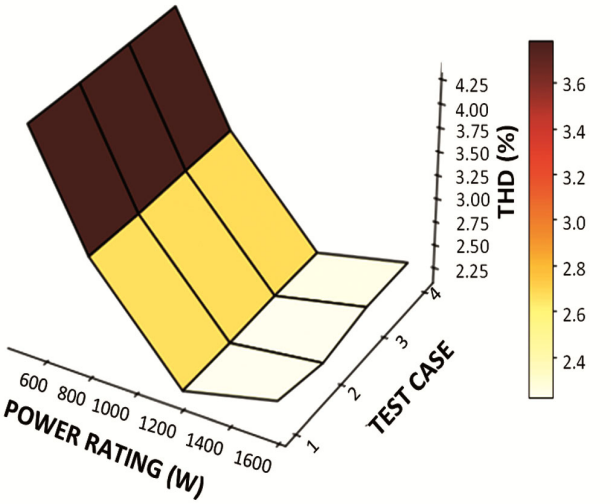

Fig. 14 — Converter THD for all four cases (3.1.1-3.1.4).

increase in the charging current i.e.8.5A for 750W system, the battery voltage rises slightly to 51.6V. The charger responds to this moderate current increase by supplying a slightly higher power level. The higher current input gradually builds up surface charge on the battery cells, which causes a small increase in voltage. This step-in current does not heavily strain the battery, maintaining a stable voltage with minimal heating.

As the charging rate increases to C/7.7, there's a more noticeable increase in the battery current, pushing it to around 13 A for 750W system. The battery voltage rises to 51.65V, showing a stronger response to the higher current flow. At this stage, the charger provides more power, accelerating the charging process, and the battery begins to experience a bit more internal heating. The gradual increase in voltage is a sign of surface charge accumulation. When the charging rate reaches C/5, the battery current surges to 20 A, leading to a further voltage increase to 51.7V. This higher charging rate introduces more heat within the battery as current flow intensifies. The charger works harder to maintain this power level, and at this stage, it's crucial for the charging algorithm to monitor for any significant temperature rise to avoid stressing the battery. At the C/3.5 charging rate, the battery current is now at 28.57 A, and the battery voltage has risen to 51.75V. This is a relatively high charging rate, and the battery voltage shows a slight increase compared to lower charging rates, reflecting increased internal resistance and temperature within the cells.

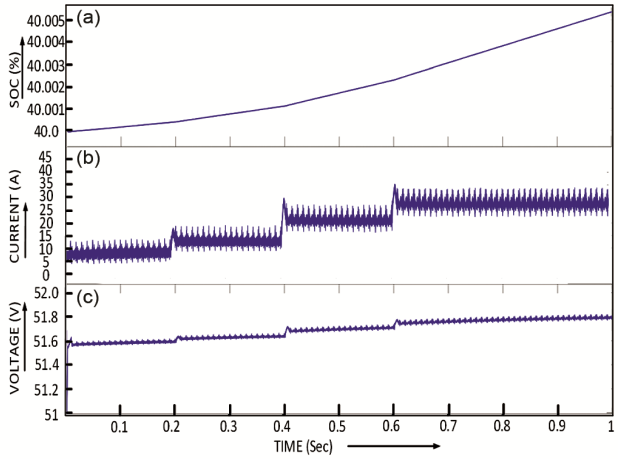

Fig. 15 — Battery dynamics (a) SOC%, (b) Battery current (A), and (c) Battery voltage.

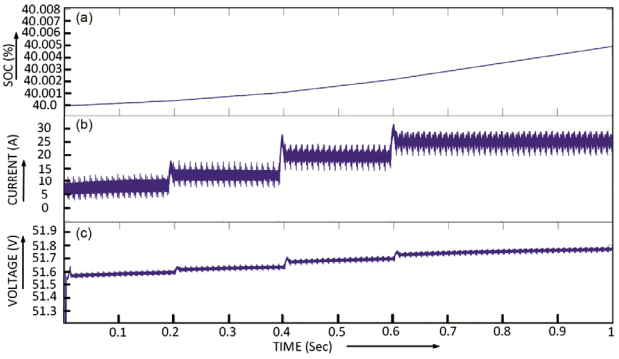

Fig. 16 — Battery dynamics (a) SOC%, (b) Battery Current (A), (c) Battery Voltage.

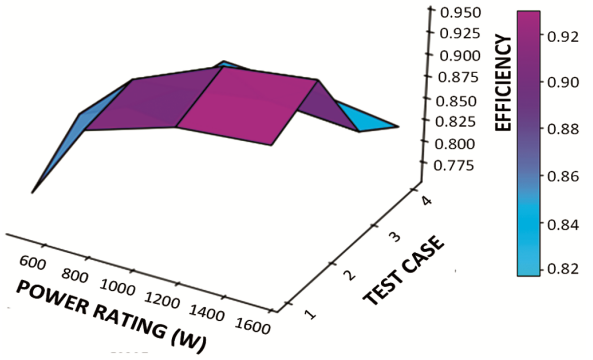

Fig. 17 — Converter efficiency for all 4 cases (3.1.1-3.1.4).

The overall performance of the converter during this process demonstrates its ability to adapt to changing charging rates while keeping the voltage stable. The gradual rise from C/10 to C/5 helps optimize the charging process, ensuring the battery is charged efficiently without causing excessive voltage spikes or stressing the battery. This staged increment in charging rate ensures that the voltage rise at the battery terminals remains controlled and minimal, maintaining system stability and protecting the battery. Figure 13 and 14 show the battery dynamics for proposed system with and without parasitics.

3.3 Power loss analysis of SSBFC

Figure 17 provides proposed converter's loss analysis for all four cases. The switches S_{wa} and $S_{wa}'$are turned on alternatively, reduces switching loss. Power losses caused during the conduction times of switches, diodes, inductor, and capacitor are included in the power loss analysis of the converter and Ripple mitigator.

When analyzing the performance of converters, the impact of parasitic elements—such as stray inductance, parasitic capacitance, and resistance—plays a critical role in determining their overall efficiency and stability. Without parasitic elements, converter is expected to exhibit optimal performance, with negligible losses and perfect switching dynamics, resulting in high efficiency i.e. 94% shown in Fig.16. However, in real-world conditions, parasitic elements introduce losses and oscillations that degrade performance. Detailed analysis of converter for four cases is explained in Table 4.

To evaluate the switching losses associated with the Switches S_{wa} (IPP60R099P7) and S_{wa}' (IPP040N06N) in the converter utilizing the DiodesD_a,D_o, $D_a'$and D_o', as well as the corresponding inductor L_S + L_S, using Powder core 77074 and 77616 for L_o and capacitor C_a, C_O components, it is essential to employ precise mathematical formulations.

The comparison between converter with and without parasitic elements reveals a significant drop in efficiency and increased thermal stress in converters with parasitics, necessitating design considerations like snubber circuits and layout optimization to mitigate their effects. Thus, accounting for parasitic elements in the design and analysis of converters is crucial for enhancing their real-world performance which is explained in Table 4.

4 Conclusion

The proposed single-stage high step-down current-controlled AC-DC converter with synchronous rectification has been successfully simulated in MATLAB, demonstrating robust performance with flexible charging rates and active ripple compensation. The system achieved an efficient output power for 750W to 1550W system and exhibit

minimum power losses, even under hard-switching conditions, resulting in a high efficiency of 94%. The input current closely tracks the input voltage, maintaining near unity power factor and complying with the IEC 61000-3-2 standard. The simulated results confirm that active ripple compensation effectively minimizes current ripple, making the converter ideal for battery charging applications.

This paper has presented an in-depth analysis of the converter system's dynamic behavior through the exploration of four distinct cases, each examining the effects of parasitic elements and the presence or absence of compensators. The study highlights the profound impact these factors have on the converter's performance, particularly in terms of the battery's State of Charge (SOC), current, and voltage regulation. The comparative analysis across the above mentioned four cases underscores the critical role of compensators in achieving optimal converter performance, particularly in systems where parasitic effects are non-negligible. The findings also highlight the need for minimizing parasitic components to ensure both efficiency and stability in power converter systems.

Furthermore, the converter's ability to charge a battery flexibly from C/10 to C/5 (10A to 20A) showcases its versatility and suitability for applications requiring high step-down capability. The modular and power-dense design makes the converter an excellent choice for onboard charging systems in small electric vehicles and microgrid environments.

References

1 Dadhaniya P, Maurya M & Vishwanath G M, *IEEE J Emerging and Selected Topics in Inds Electro*, 5 (2024) 553.

2 Le T T, Lee J &Choi S,*IEEE Transon Power Electronics*,39 (2024) 1060.

3 Belkamel H, Kim H& S. Choi*, IEEE Trans. Power Electron,* 36 (2021) 3486.

4 Naradhip A M, Kang S, Kim & Choi S, *Proc IEEE Appl Power Electron Conf Expo*, (2019) 757.

5 Kim H, Park J, Kim S, Hakim R M, Belkamel H, & Choi S, *IEEE Trans Power Electron*, 37(2022) 6780.

6 Choi W & Yoo J, *IEEE Trans. Power Electron,* 26 (2011)3884.

7 Le T T, Hakim R M, Park J& Choi S, *Proc. IEEE Energy Convers Congr Expo* (2021) 2208.

8 Le T T, Hakim R M, & Choi S*, IEEE Trans Power Electro*, 38 (2024) 4945.

9 Le T T, Lee J, and Choi S, *Proc IEEE Energy Convers Congr Expo*,2022, 1–5.

10 Li G, Xia L, Wang K, Deng Y, He X, & Wang Y, *IEEE J. Emerg. Sel. Topics Power Electron,* 8, (2020)1767.

11 Huber L, Liu G & Jovanovic M M,*IEEE Trans. Power Electron.,* 25, (2010) 85.

12 Endo H, Yamashita T & Sugiura T, *Proc. IEEE Power Electron. Spec. Conf,* 1992, pp 1071.

13 Yen-Wu L& King R J, *IEEE Trans. Power Electron.*, 10 (1995) 158.

14 Jang Y & Jovanovi´c M M, *IEEE Trans. Power Electron.,* 26(2011) 602.

15 Lin & Wang F, *IEEE Trans. Ind. Electron,* 65 (2018)7730.

16 Meng et al L, *IEEE Transactions on Industrial Electronics*, 67(2020)10366.

17 Zarkab Farooqi M, Singh B and Panighiri B K, *IEEE Trans on Inds Apps,* 59 (2023) 5739.

18 Singh A, Gupta J & Singh B, 2022, *IEEE 2nd Int Conf on Sustainable Energy and Future Electric Transp (SeFeT),* (2022) 1.

19 Lee J & Won J, IEEE J, *Emerging and Selected Topics in Power Electro,* 12 (2024) 283.

20 Tang Y, Zhu D, Jin C, Wang P & Blaabjerg F, *IEEE Transactions on Power Electronics*, 30(2025) 717.

21 Farooqi M Z, Singh B & Panigrahi B K, 2022 *IEEE Global Conf on Computing, Power and Comm Tech (GlobConPT),* 2022,1.

22 Prasanna U R, Singh A K & Rajashekara K, *IEEE Transactions on Transportation Electrification*, 3 (2017) 536.

23 Gupta J, Singh B, J. Inst. Eng. India Ser. B 105(2024) 27.

24 Dutta S, Rathore A K & Khadkikar V, *IEEE J Emerging and Selected Topics in Indus Electro,* 4 (2023)1170.

25 Sivaperumal N, Jothimani G, Electr Eng 106(2024) 4127.

26 Kumar G K N & Verma A K, IEEE Trans on Inds Apps, 59 (2023) 7163.

27 Kazemtarghi A, Chandwani A, Ishraq N & Mallik A, *IEEE Trans on Transportation Electrification*, 9 (2023) 1629.

28 Singh B & Verma V, IEEE Trans on Power Delivery, 23 (2008)792.

29 Singh A, Badonim and Mishra A K, Inter J Circuit Theory and Apps, Wliey, (2025)1.

30 Dubey R and Joshi D, *2012 IEEE 5th India International Conference on Power Electronics (IICPE)*, (2012)1