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Optimized meta-heuristic VCO-based ADC design and analysis

Sriram Sundar S[a*] & G. Mahendran[b]

[a]Department of Electronics and Communication Engineering, CARE College of Engineering, Tiruchirappalli, Tamil Nadu, India
[b]Department of Electronics and Communication Engineering, Syed Ammal Engineering College, Ramanathapuram, Tamil Nadu, India

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The ADC (Analog to Digital Converter) has become essential for interfacing analog signals with the digital domain, particularly in applications requiring high resolution and low voltage operations. Recent advancements in technology have led to reduced signal power and voltage through supply voltage scaling, which has posed significant challenges for ADC performance, including increased area, narrow input range, and process variation. To address these issues, this study has proposed a VCO (Voltage Controlled Oscillator)-based ADC integrated with an ACO-PSO (Ant Colony Optimization–Particle Swarm Optimization) algorithm, thereby enhancing stability, reliability, and effectiveness in chip design. The proposed system has utilized real-time input sources, specifically solar PV (Photo Voltaic) and wind energy, and has incorporated a SEPIC (Single-Ended Primary Inductance Converter) to deliver a controlled output voltage. The ACO-PSO algorithm has optimized the values obtained from the VCO-based ADC and has selected the best solutions to achieve improved performance. The efficiency of the framework has been assessed by measuring gain and delay through Verilog simulations, and the results have been obtained using MATLAB/Simulink. The circuit has occupied an area of 0.012 μm² and has achieved a Mean Square Error (MSE) of 0.2 and a Peak Signal-to-Noise Ratio (PSNR) of 52 dB, thereby demonstrating superior efficiency compared to conventional methods.

Keywords: Analog to digital converter, Ant colony optimization particle swarm optimization, SEPIC converter, Voltage controlled oscillator

1 Introduction

The ADC is an electronic circuit that accepts analog input signal and generates digital output, whereas DAC (Digital to Analog Converters) are used to convert the digital input into analog output. Generally, the ADC takes the input as a continuous time signals and then converts into a quantised data points or discrete output level. The ADC[1] inputs either current or voltage tends to fluctuate from a set of minimum value to a set of maximum value. This is performed to generate a valid digital output depiction of analog inputs. If both positive and negative analog inputs exceeds these limits, it can cause damage ADC and also saturates the outcome at either minimum or maximum digital output rate. An oscillator is considered as a circuit, which generates revolving waveform with constant repetitions and lacks in information. These oscillators tends to turn unidirectional current stream from a DC (Direct Current) source into its additional waveform with the ideal recurrence. Based on the advancements of updated and new IC (Integrated Circuits) technologies, the microprocessors and communicating systems works at gigahertz frequencies[2] . This helps the systems to process with efficient chip area, low cost and low power consumption and it needs an oscillator to generate stable periodic signal. The stable periodic signal is used to achieve some functions namely synchronisation clock and stable frequency signal for microprocessors in order to modulate or demodulate the information signals. Thus, VCO (Voltage Control Oscillator) are designed to produce high frequency periodic signals and accurate frequency. But the traditional VCO had a bad reputation on performance characteristics like distortion, non-linearity, robustness and noise. However, these problems can be tackled by using suitable circuit design and architectures. Thus, VCO based ADC systems are used in wide applications, to improve the efficiency and achieve enhanced performance[3] . Earlier studies of VCO where based on increased tuning range, low operating voltage, low power, lower phase noise and higher frequency [4] . However, these limitations has to be overcome by employing better algorithms, to provide effective communication systems.

Concurrently, the ADCs face design challenges when ported with smaller highly scaled technology nodes. The traditional ADC circuits mostly rely on the

*Corresponding author
(E-mail: subramanian.sriramsundar@gmail.com)

manual re-spins and design iterations in order to meet the desired performance specifications. So, the considered paper[5] has introduced NeuADC (Neural Network based ADC), to synthesis the analog to digital interface that approximates the desirable quantisation function. This is done by using NN (Neural Network) with a single hidden layer. Along with the model, mixed signal RRAM (Resistive Random Access Memory) crossbar structure, to develop a dual path configuration for operating basic NN in circuit level. From the outcomes, it is predicted that the study has quantify the impacts of ADC quantisation quality from hidden neurons, area, power, design trade-off between speed, PVT (Process, Voltage and Temperature) variations and RRAM resistance imprecision. Apart from solar (PV), wind energy can also be employed as input. Therefore, the intimated study[6] , employed wind speed estimation, this method has employed to accomplish the DFIG and MPPT under varying wind speed at diverse circumstances. From the experimental outcome, it has been identified that simulated curve represents the good agreement between the empirical outcomes and simulation outcomes at different wind speed. The suggested study[7] , employed an amalgam AC and DC method and MO-UOPF (Multi-Objective Unified Optimal Power Flow) has also been employed. The MO-UOPF converter employed in the recommended study [8] employed a VSC – HVDC (Voltage Source Converter – High Voltage Direct Current). Here, the major objectives of the study includes reducing the total generation cost, enhancing the stability of the voltage, reduction of unwanted gases, AC/DC transmission line of losses and so on. In order to enhance the voltage output, a boost converter termed as SEPIC (Single-Ended Primary-Inductance Converter) can be used. Hence, the considered study [9] emphasized on incorporating a SEPIC converter in hybrid energy generation system. Apart from SEPIC, BESS (Battery Energy Storage System) and DG Set (Diesel Generator Set) are also employed to ensure the dependability of the energy generation system. The SEPIC converter is connected to the boost converter which helps in lowering the cost and helps in decreasing the total harmonic distortion and it also helps in overcoming issues like balancing of the load, regulation of voltage etc. performance of the model can be evaluated using MATLAB/Simulink.

Even though there are various advantages of employing the existing studies, there are some disadvantages, which needs to be addressed such as efficiency and stability of converters and power systems. So, the proposed study aims to overcome the issues and pitfalls of these exiting studies by employing hybrid form of two real-time input sources such as solar PV panel and wind. Initially, the power is generated from the solar and wind panels are directed to AC-DC converter, where the input AC is transformed into DC source. Here, the ACO-PSO optimisation algorithm is employed to generate effective ADC converter. The signal is then operated with PWM (Pulse Width Modulation) generator, where the signal comprises of trained pulses. These trained pulses are in the form of square waves and the output signal is in a "high" state. As PWM possess the ability of providing low power loss and better efficiency they tend to precisely control the power. Then the output from PWM is fed into VCO, which controls the voltage developed inside the circuit. A VCO based ADC that process the analog information tends to decrease the power consumption and better operating voltage. It is then implemented in Verilog platform to calculate the efficacy of the proposed model and the performance of the proposed approach is measured based on metrics namely power, delay, gain, area of the voltage. The main contributions of the present work are as: To design an improved VCO-based ADC, to convert analog real-time input sources into digital sources and further enhance the performance and energy efficiency, to perform PWM generation using ACO-PSO (Ant Colony Optimization and Particle Swarm Optimization) algorithm, to optimise best solution for VCO and to improve the area, delay, power and gain of the voltage using Verilog and compare the results procured by the model with existing approaches.

Different techniques involved in analog to digital converters and studies related to proposed work are analysed and reviewed in this section with problem identification.

In recent days, the world's data is propagating within the optical fibres supporting both throughput and high channel rates. But the bottleneck of a network is found to be the throughput and power consumption arising from the interfaces and connections at its input and output. Additionally, the digital sensors or systems requires an ADC or EO (Electronic to optical), DAC and ADC are considered to be power consuming elements in high speed data link. So, the suggested study[10] has implied coherent

parallel photonic DAC combined with an experimental prototype. This prototype has been providing ability of performing DAC, in which the optic-electric-optic domain crossing is not applied. The communication systems, radar imaging are operated in a broad bandwidths and high operational frequencies that requires ADC's. These ADCs should be with sufficient accuracy, broadband coverage and high sampling rate for efficient transmission. Hence, the intimated study[11] has implemented photonic ADC structure, to overcome the ADC trade-off among accuracy, bandwidth and speed. The DNN (Deep Neural Networks) has performed the learning of patterns in photonic system defects and recover the distorted data. This has tend to provide high quality of electronic quantised data adaptively and succinctly. The digital representation of multivariate CT (Continuous Time) has found to be complex in several signal processing systems. So, the suggested study[12] has used task based ADC, to produce digital illustration of multivariate CT input method. This has been performed in order to recover the fundamental statistically related element called as task. It has deployed scalar uniform quantisation, uniform sampling and analog filtering, before recuperating the task element using linear digital recovery filter. Then the A/D filters has been optimised and close form expressions has been derived for optimised MSE (Mean Square Error). This has been done to recover task vector from a set of analog signals, when applying ADCs along with an amplitude resolution and fixed sampling rate.

The ADC along with other sensor interfaces are complex, such that it is an intensive analog structure and accelerating to produce other innovations need remodelling. This brings the partial area down-scaling when it is compared with the digital systems. Hence, the considered paper[13] has implemented fully synthesizable SAR (Successive Approximation Register) ADCs, which is applicable for low cost integrated systems. This has been introduced for both current and voltage inputs. The design has enabled voltage scaling to adjacent threshold state, silicon area reduction and low effort design. These analog-intensive designing systems has allowed compact system combination effort, although immense-in-logic ADC structure, digital area reduction across CMOS generations and design porting. From the analysis, it has identified that the system has produced typical capacity to cover direct procurement of current and voltage inputs, lowest area and high level of design automation, by supressing the need of trans-resistance amplifier in current readout. In pipelined ADCs, the switched capacitor plays a significant role. Whereas, the capacitor and finite op-amp (operational amplifier) are the main amplification errors that limits the performance of the system. On the intention of overcoming , the intimated study[14] has performed RS (Reference Swapping) and ACLS (Averaging Correlated Level Shifting) to reduce errors from finite op-amp gain and capacitor mismatch in a pipe-lined ADC. Here, the ACLS method has tend to reduce the sensitivity of ADC precision to op-amp gain, by averaging the finite op-amp gain errors under two amplifying stages. Whereas, the second amplifying stage has been developed to have conflicting polarity to the first amplifying stage. Further, the RS has used averaging operation, in order to decrease the capacitor random mismatch error and has thus integrated a simple capacitor layout structure. Thus, this system has been capable for high pipelined resolution ADCs, low complexity and calibration free ADCs.

The energy efficient wide band ADCs are significant for applications like radio receivers, portable battery powered devices and others. Based on number of bits, the power consumption is increased, thus providing low efficient systems. Hence, the considered study[15, 16] has implemented a new circuit based method to alleviate the non-linearity in open loop RO based ADCs. This system has been comprised of accelerating a CCO (Current Controlled Oscillator) along with various trans-conductors interlinked parallel to the varying bias conditions. In order to evaluate, the model has been designed with ring oscillator based ADC and simulated in 65nm. The non-linearity has been reduced and has resulted in ENOB (Effective Number of Bits) enhancement. The design has been found to be better without resorting to a compound structure and has required simple foreground digital calibration.

A hybrid MR (Memristor) complementary metal oxide semiconductor based flash ADC has been employed in the considered study[17] . In most cases, the flash ADC is the firmest type of ADC, but due to the resistor mismatch the efficiency of the system is affected. It is considered as the first tuneable MR to produce precise reference voltages. An analogue behaviour has been detected in multi-stage MR devices and the electrical constituents if the devices have been extracted by using device characterisation.

Further, to develop a correlated mathematical and SPICE (Simulation Program with Integrated Circuit Emphasis), the VTEAM (Voltage Threshold Adaptive Model) has been applied. This approach has tend to decrease the dispute of resistor mismatch resulting in encoding inaccuracies. It has also improved the area efficiency and ADC transfer function characteristic. It has also reduced the integral and differential non-linearity errors. A two-step ADC with single channel hybrid voltage time, is applied in the suggested study[18, 19] . This has been performed to attain better speed in low voltage nano-scale CMOS technology. This method has been used to solve the variations in the voltage, since the technology scaling and supply voltage reduces simultaneously. To achieve low power ADCs and high speed, the efficiency and speed of time domain converter and high accuracy of voltage domain CDAC (Capacitive DAC) are combined together. A power efficient operation has been performed by introducing RO (Ring Oscillator) based TDC (Time to Digital Converter) and a speed optimised VTC (Voltage to Time Converter).

Another method of 8-channel time interleaved VCO[20, 21] based ADC has been used in the intimated study[22] achieving 7.2 ENOB (Effective Number of Bits) at 5GS/s in 28nm CMOS. In this study, a shared tail transistor and a high speed RO with feed forward cross coupling has been combined together along with asynchronous counter. This has been done to enhance the resolution and reducing the power consumption. To provide the sampling of synchronous counter state, an asynchronous double sampling has been employed. The sampling time mismatch, non-linear distortion and channel mismatch has been compensated by applying on chip digital calibration. This has been corrected by using tunable clock delays. Similarly, a digital background calibration approach for pipelined ADC has been deployed in the considered study[23] . This study has been based on the framework of split architecture to address the non-linearity and finite dc gain of the residue amplifier. Here, the pipelined ADC has been separated into two different channels, in which each channel involves an ideal backend ADC.A 1.5 bit per stage. On the other hand, the pseudorandom sequence has been introduced before one of the channels. To rectify the errors, the difference between the digital outputs of the two channels has been used. A microchip readout chip combined with VCO based ADC has been implemented in the suggested study [24, 25] . An open loop pseudo differential structure has been involved along with ROs and a coarse fine frequency to digital converter.

From the assessment of above existing works, core concerns are emphasized as explored below,

- The SAR based ADCs are introduced in the paper, which should be extended to envelope the persistence of mostly and fully digital ADC structures[13] .
- The study has implemented ring oscillator based ADCs, to overcome the non-linearity current to frequency function. But it should also be performed in the way to reduce the area of the circuit and develop in several other high-resolution applications[15] .
- Even though, the suggested study has performed well, it lacks in detecting the faults automatically with an accuracy of 97.5%, which would make the degradation of system and finds help in detecting the fault precisely[26] .

2 Materials and Methods

Figure 1 portrays the entire procedure of the proposed framework. Initially, the real-time based input source such as wind and PV are fed into a framework, which comprises of AC-DC converter and VCO controller. AC-DC converters possess high efficiency, therefore it possess very less energy loss during the operation. And SC-DC power supply has low standby power consumption. In addition to AC-DC converter, SEPIC converter is also utilized. The SEPIC converter permits the grid to process the different input voltages and generate enhanced output. Further, ACO-PSO algorithm is proposed for determining the optimal control parameters to control the speed. Here PWM generator is employed to reduce the average power produced by the digital

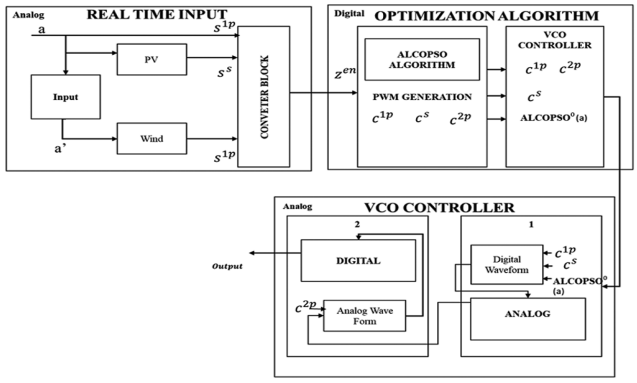

Fig. 1 — Working mechanism of the proposed framework.

signal and transforming these signals into discrete parts. Here, the signal energy is dispersed through a sequence of pulses instead of incessantly varying signal. It is used for voltage regulation and controls the amount of power delivered without dissipating any wasted power. Thus, the VCO is employed to tune the operating frequency producing an output that is directly proportional to its input voltage.

2.1 PMSG (Permanent Magnet Synchronous Generator) modelling

The voltage V_{RE_i} and current I_{RE_i} generated by the input power sources differs with the solar radiation level. The current and voltage that is accomplished from rectification is mathematically shown in terms of stator voltage/stator current as shown in equation (1) and (2),

$$V_{RE_i} = \frac{3\sqrt{6}}{\pi V_{i_{stator}}} \quad \ldots (1)$$

$$I_{RE_i} = \pi/\sqrt{6} V_{i_{stator}} \quad \ldots (2)$$

Figures 2 & 3, represents the PMSG model with steady current and battery deisgn which is based on electric ciruict is depicted.

Mathematical modelling of the wind module includes, the power rating associated with the behaviour of aerodynamic is scientifically computed using the equation (3),

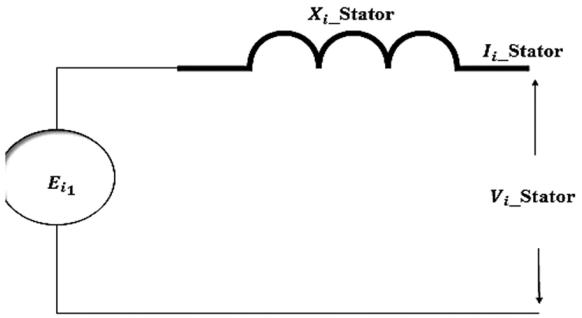

Fig. 2 — PMSG Model with steady current

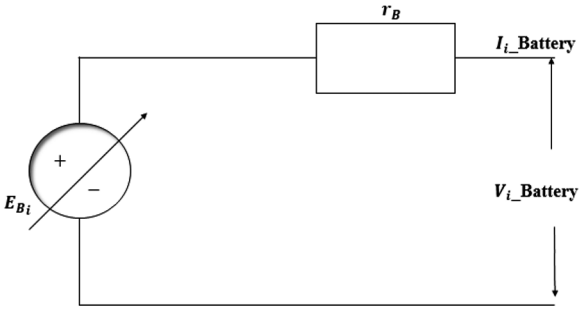

Fig. 3 — Battery model of the circuit

$$P_{i_{Turbine}} = \frac{1}{2} * C_{i_p}(\lambda_t, \beta_p) \text{pair } \pi R_{iT}^2 V_{iwind}^3 \quad \ldots (3)$$

Speed of the turbine is correlated with the velocity of the wind and the velocity of the wind turbine is computed the equation (4),

$$\frac{\Omega_{Turbine} * R_{iT}}{V_{iwind}} \quad \ldots (4)$$

Coefficient of the power is $(C_{i_p}(\lambda_t, \beta_p))$ is calculated by mathematical relation as per equation (5),

$$C_{i_p}(\lambda_t, \beta_p) = (0.34 - 0.0016) * (\beta_p - 2) * \sin K * (-184) * 10^5 (\lambda_t - 3)(\beta_p - 2) \quad \ldots (5)$$

Mechanical relationship governing the wind turbine is mathematically given by equation (6),

$$\text{Mechanical} = \frac{P_i \text{mechinical}}{\Omega_{Turbine}} \quad \ldots (6)$$

Based on the outcome generated by the PV and wind turbine, it is then fed into converter block that incorporates the SEPIC converter.

2.2 Sepic converter

2.2.1 Maximum duty cycle

Voltage-gain of SEPIC converter at steady state is represented by equation (7),

$$V_i O + V_i D = V_{iin} \frac{D_i}{1 - D_i} \quad \ldots (7)$$

In which V_i D is denoted as on state drop across diode, V_{ii} is denoted as input voltage, V_iO is represented as output voltage and D_i is represented as PWM duty ratio.

MDC (Maximum value of duty cycle) is estimated using below equation (8),

$$D_{imax} = \frac{V_i O + V_i D}{V_{iin\_max} + V_i O + V_i D_i} \quad \ldots (8)$$

2.2.2 Coupling capacitor

Depending upon the peak to peak (PTP) ripple voltage, RMS current, selection of coupling capacitor is done.

2.2.3 Induction selection

With ripple-content at 7.5% of the rated inductor current with 20 kHz of switching frequency, selecting optimal value of the inductor for CCM function is calculated by equation (9),

$$L_1 = L_2 = \frac{V_{iin}}{\text{ilf}_{sw}} D_{imax} \quad \ldots (9)$$

2.2.4 Output capacitor choice

As the DC-bus voltage regulation is the process of DC-DC bi-directional converter of battery, the output capacitor choice is not much vital in this functionality.

2.3 ACO-PSO optimization algorithm

The output from the SEPIC converter is further passed into ADC converter, which converts the analog input into digital output. It is optimised by deploying ACO-PSO meta-heuristic algorithm to efficiently generate the output. In existing methods, different metaheuristic algorithms have been used in energy analysis and estimation. Specifically, among all the approaches, ACO and PSO are considered as prominent algorithms. They are also widely used in resolving several optimisation issues showing improved outcomes. So, to improve and achieve optimised performance, hybrid form of ACO and PSO has been used in the present study.

$$v_i(s+1) = wv_i(s) + a_1u_1\left(p_{b,i} - p_i(s)\right) + a_2u_2(g_{b,i} - p_i(s) \quad \ldots (10)$$

$$p_i(s+1) = p_i(s) + v_i(s+1) \quad \ldots (11)$$

In which, i=1,2,3,…n, v_i denotes the particle velocity and p_i signifies the particle position. The number of iterations is given by 'k' with inertia weight 'w'. The random variables $u_1$and u_2, which are distributed uniformly between [0,1] and a_1, a_2 are the social and cognitive coefficients. p_b is the individual particles best position and best position g_b is the best position between entire particles individual best position. Thus, the PSO preserves the p_b as best values and endures to update, till the g_b point is predicted or achieves the objective function. However, the performance of PSO is enhanced by using hybridisation of ACO algorithm, which jointly increase the efficiency of the system.

In case of ACO, the probability based approach is employed to resolve computational issues, which is inspired by the behaviour of ants for probing shortest route starting from their colony upto the food source. Generally, the ants follow shortest route to attain their food source, in which they leave a chemical component called as pheromone trail. Moreover, the pheromone trail aids other ants to track the same route, where the members of the same species tend to react. To predict the pheromone concentration, the formula is represented by the equation (12),

$$S_{ab} = \omega S_{ab}(s-1) + \Delta S_{ab} \quad \ldots (12)$$

Where, ω is the pheromone concentration rate, S_{ab} is the revised pheromone concentration and ΔS_{ab} is the concentration variation in pheromone. With the potential benefits of hybrid ACO-PSO algorithm the proposed study implements VCO based ADC system. It enhances the ACO sequentially feature by the exploitation ratio of the PSO. The step-wise procedure for the implementation of proposed ACO-PSO is explained as follows,

1. Establishment of objective function or ACO fitness function.
2. Set optimization parameters and limits of the variables
3. Production of random population,in which the population is denoted as given in equation (13),

$$\text{Population} = \begin{bmatrix} \text{PACO}_{11} & \text{PACO}_{12} & \text{PACO}_{21} \\ \text{PACO}_{21} & \text{PACO}_{22} & \text{PACO}_{23} \\ \text{PACO}_{\text{nn}} & \text{PACO}_{\text{nn}} & \text{PACO}_{3\text{n}} \end{bmatrix} \ldots (13)$$

4. Analog Phase: The mean for the particular variable can be calculated as the following equation:

$$\text{M}*,\text{D} = [\text{m1}, \text{m2}, \ldots\ldots, \text{mD}] \quad \ldots (14)$$

5. PWM GENERATION: Best solution analog pulse generated if P_i
6.The best solution is taken into consideration, as an analog for that specific iteration:

$$\text{P}_\text{i}\text{analog} = \text{P}_\text{i}(\text{f}_\text{o}(\text{P}_\text{i}) = \min) \quad \ldots (15)$$

7. The grade point of each variable is sorted and a new mean is calculated. The difference between two means is evaluated with subsequent equation, TF is considered as 1 or 2 and D is digital phase

8. $$\text{Di f f erence}*,\text{D} = \text{r}(\text{Mnew},\text{D} - \text{TF} \times \text{M}*,\text{D}) \quad \ldots (16)$$

9. Update the values by adding the difference to the ACO- PSO solution.

10. $$\text{DA},\text{D} = \text{Xold},\text{D} + \text{Di f f erence}*,\text{D} \quad \ldots (17)$$

The each particle possesses a track on both local and the global best solution. The local best of a particle is processed depending on the minimal value of objective function. Whereas, the global best of all assessed particles is the minimum value of objective function. At the completion of each iteration, the particles move towards in the direction of local best for specific units. Then, the particle transfers to global best for equivalent units. Further, it is repeated for all iterations, until the optimal best solution is attained. However, ACO is considered as population-based heuristic algorithm, where the optimal solution is evaluated for non-linear variables. Consequently, the

nodes are arbitrarily generated at equally speeded units and the update of pheromone matrix is done to discover the optimised value.

3 Results and Discussion

3.1 Simulation results

The voltage generated in solar and wind turbine are simulated and shown in Fig.4, which shows that the voltage regulation is maintained and thus reducing the voltage drop. This transmission has provided better tendency to increase the power efficiency.

The VCO is used in converting the initial analog signal form to digital wave followed by the conversion of digital wave to analog signal. The output power spectrum of the proposed VCO using spectrum analyser is pemed in the study as shown in Fig 5.

Due to some frequency fluctuations, it is complex for a system to generate power effectively. As shown in Fig.6, it is observed that frequency range is gradually increased with variations on solar and wind inputs.

The proposed model consist of different number of gates as shown in Fig. 7 These gates are used for the purpose of converting analog to digital signals.

The internal design architecture of the proposed system is shown in Fig. 8, which denotes the functionality and connectivity among different circuit elements deployed in the proposed system.

The slice LUT of the proposed model is signified in Fig. 9, in which a slice consist of set number of LUTs.

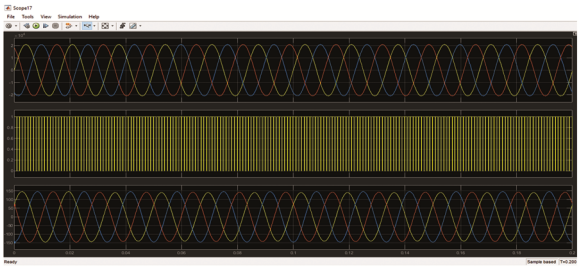

Fig. 5 — VCO using spectrum analyser.

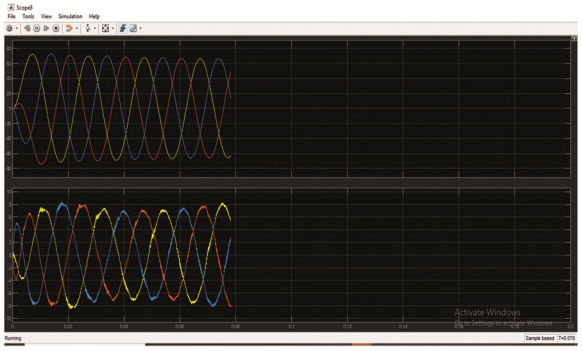

Fig. 4 — Voltage produced by Solar PV and wind turbine.

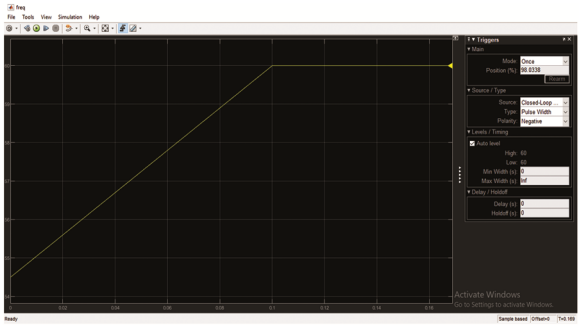

Fig. 6 — Frequency variation of solar and wind energy.

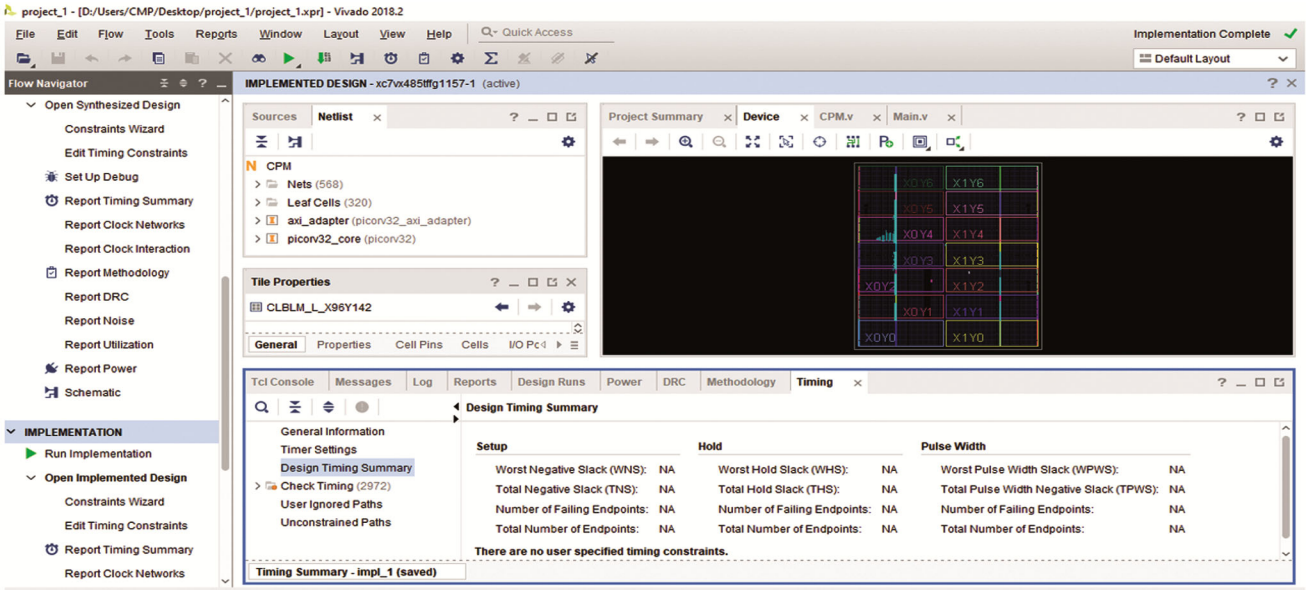

Fig. 7 — Overall gates used in proposed model.

These LUTs are the group of logic gates hard-wired on a circuit that stores a default list of outputs from every combinations of inputs. This tends to produce a fast way to recover the output from a logical operation.

The total power produced by the proposed model is illustrated in Fig.10. From analysis, it is found that the total on-chip power attained is 31.605 W, temperature of the junction obtained is 69.2ºC. The power generated is identified to be 97% denoting 30.565W. Thus, the outcomes produced by the proposed model portrays that the model tend to be efficient.

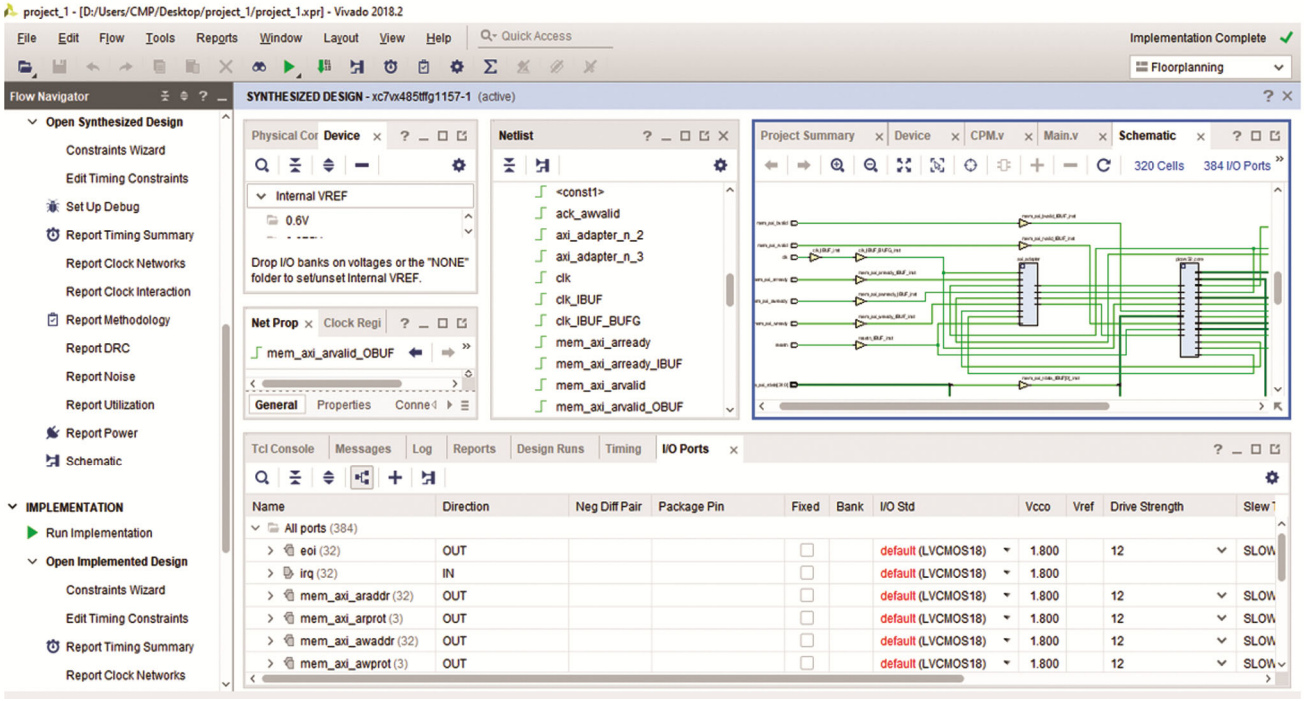

Fig. 8 — Schematic diagram of proposed model.

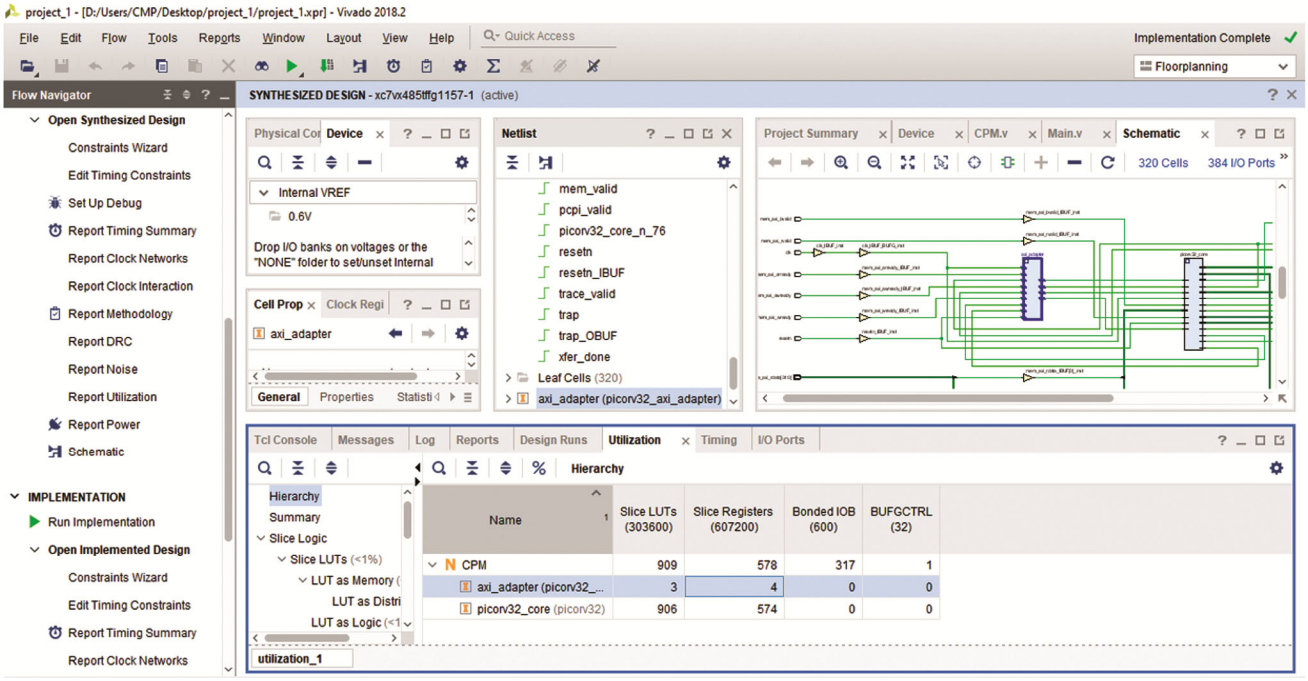

Fig. 9 — Slice LUTs representation.

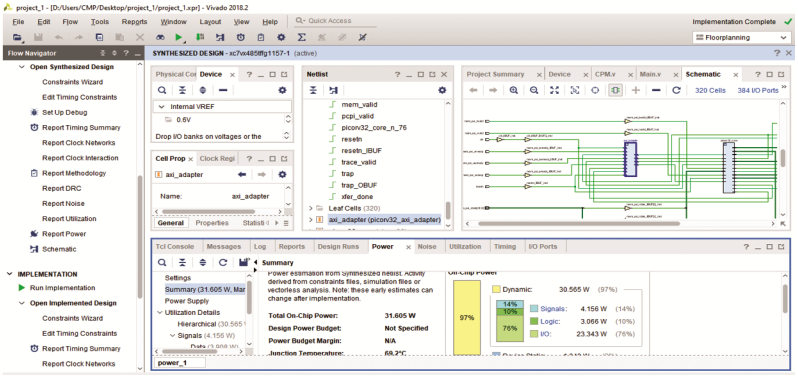

Fig. 10 — Power generated by the proposed model.

Table 1 — Comparative analysis of the prevailing method with proposed method[26].

Methods	Supply Voltage	Frequency	Area
Existing Method	3.3 V	9.37 GHz	0.22 m^2
Proposed Method	3.3 V	5.0 GHz	0.123 m^2

Table 2 — Comparative analysis of existing approaches with proposed method[28].

Methods	TE (%)	FC (s)	OA (W)
P&O	93.55	0.29	77.42
INC	94.84	0.22	64.98
FLC	96.56	0.19	42.65
Fractional VoC	94.25	0.24	65.37
HC	91.13	0.38	85.65
HWO-PS-INC	99.35	0.13	4.54
Proposed	99.41	0.11	4.25

Table 3 — Comparative analysis of PSNR model[29].

Method	PSNR	MSE
SSLAR –ADC	57	0.7
Proposed Method	52	0.2

3.2 Comparative analysis

Table 1, shows the supply voltage, frequency and area of the existing method and proposed method, in which supply voltage of the existing method is 3.3V, frequency is 9.37 Hz and area determined is 0.22. Whereas the proposed method obtained supply voltage is 3.3V, frequency of the proposed method is 5.0 GHz and area obtained by the proposed method is 0.123. Table 2 signifies the comparative analysis of existing approaches with proposed method

It is found that the tracking efficiency of the proposed method is better than the existing ones, by obtaining TE rate of 99.41%, proposed approach obtained FC with 0.11 seconds with much faster and quicker than existing methods and finally, OA obtained by the proposed method is only 4.25.

From Table 3, it can be depicted that PSNR of existing method is 57 and MSE is 0.7 whereas the PSNR of proposed method is 52 and MSE is 0.2.

Table 4 — Comparative analysis of the process[30].

Process	180nm CMOS	65nm CMOS (ADC)	65nm CMOS (ADC)	Proposed
Area (mm²)	0.0517 (incl. shared DCO)	0.096	0.013	0.04523
Sampling Rate (fs)	255kHz avg. for 1kHz sine	50kHz	4.17kHz	3.52kHz
Power (µW)	36.7 µW (9.94 µW reused from AD-PLL)	38 µW (excluding ref. gen. blocks)	0.92 µW	0.99 µW
SNDR (dB)	40.2 @ 100mV PK-PK	44.5 @ 10mV PK-PK	39.1 @ 1.6mV PK-PK	29.1 @ 1.6mV PK-PK
Efficiency (pJ/sample)	142 @ 255k-samples/sec	760	220.6	220.6

Table 4 prioritizes ultra-low power consumption (0.99 µW), achieving a level nearly 40 times lower than the first two benchmarks. While it maintains a competitive efficiency of 220.6 pJ/sample, it trades off performance in sampling rate (3.52 kHz) and SNDR (29.1 dB). With a mid-range area of 0.04523 mm², the process is best suited for energy-constrained applications where power savings are more critical than high-speed resolution.

4 Conclusion

The proposed framework aims to enhance the efficiency of a VCO-based ADC by implementing a hybrid ACO-PSO optimization algorithm. This approach addresses significant challenges such as power consumption and operating voltage, which are critical in chip design. Existing works often lack stability and efficiency, particularly at high voltages. The integration of the ACO-PSO algorithm not only optimizes the ADC's performance but also minimizes

noise and power consumption through a PWM generator. Performance evaluations focus on key metrics including area, delay, power, and gain. The results indicate that the circuit occupies an area of 0.012 μm², with a Mean Square Error (MSE) of 0.2 and a Peak Signal to Noise Ratio (PSNR) of 52 dB, demonstrating superior performance compared to existing methods.

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